

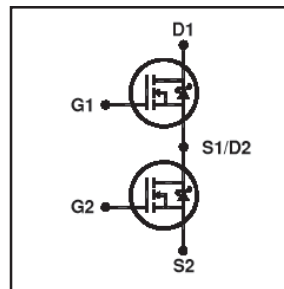
# IRFI4019HG-117P

## DIGITAL AUDIO MOSFET

### Features

- Integrated Half-Bridge Package
- Reduces the Part Count by Half
- Facilitates Better PCB Layout
- Key Parameters Optimized for Class-D Audio Amplifier Applications
- Low  $R_{DS(ON)}$  for Improved Efficiency
- Low  $Q_g$  and  $Q_{sw}$  for Better THD and Improved Efficiency
- Low  $Q_{rr}$  for Better THD and Lower EMI
- Can Delivery up to 200W per Channel into  $8\Omega$  Load in Half-Bridge Configuration Amplifier
- Lead-Free Package
- Halogen-Free

Key Parameters ⑥		
$V_{DS}$	150	V
$R_{DS(ON)}$ typ. @ 10V	80	m $\Omega$
$Q_g$ typ.	13	nC
$Q_{sw}$ typ.	4.1	nC
$R_{G(int)}$ typ.	2.5	$\Omega$
$T_J$ max	150	$^{\circ}$ C



G1, G2	D1, D2	S1, S2
Gate	Drain	Source

### Description

This Digital Audio MosFET Half-Bridge is specifically designed for Class D audio amplifier applications. It consists of two power MosFET switches connected in half-bridge configuration. The latest process is used to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery, and internal Gate resistance are optimized to improve key Class D audio amplifier performance factors such as efficiency, THD and EMI. These combine to make this Half-Bridge a highly efficient, robust and reliable device for Class D audio amplifier applications.

### Absolute Maximum Ratings ⑥

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	150	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	
$I_D$ @ $T_C = 25^{\circ}$ C	Continuous Drain Current, $V_{GS}$ @ 10V	8.7	A
$I_D$ @ $T_C = 100^{\circ}$ C	Continuous Drain Current, $V_{GS}$ @ 10V	6.2	
$I_{DM}$	Pulsed Drain Current ①	34	
$E_{AS}$	Single Pulse Avalanche Energy②	77	mJ
$P_D$ @ $T_C = 25^{\circ}$ C	Power Dissipation ④	18	W
$P_D$ @ $T_C = 100^{\circ}$ C	Power Dissipation ④	7.2	
	Linear Derating Factor	0.15	W/ $^{\circ}$ C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	$^{\circ}$ C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

### Thermal Resistance ⑥

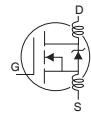
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	6.9	
$R_{\theta JA}$	Junction-to-Ambient	—	65	

Notes ① through ⑥ are on page 2

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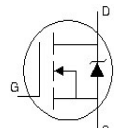
## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified) ⑥

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.19	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	80	95	$m\Omega$	$V_{GS} = 10V, I_D = 5.2A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	4.9	V	$V_{DS} = V_{GS}, I_D = 50\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-11	—	$mV/^\circ\text{C}$	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$g_{fs}$	Forward Transconductance	11	—	—	S	$V_{DS} = 50V, I_D = 5.2A$
$Q_g$	Total Gate Charge	—	13	20	nC	$V_{DS} = 75V$ $V_{GS} = 10V$ $I_D = 5.2A$ See Fig. 6 and 19
$Q_{gs1}$	Pre-Vth Gate-to-Source Charge	—	3.3	—		
$Q_{gs2}$	Post-Vth Gate-to-Source Charge	—	0.8	—		
$Q_{gd}$	Gate-to-Drain Charge	—	3.9	—		
$Q_{godr}$	Gate Charge Overdrive	—	5.0	—		
$Q_{sw}$	Switch Charge ( $Q_{gs2} + Q_{gd}$ )	—	4.1	—		
$R_{G(int)}$	Internal Gate Resistance	—	2.5	—	$\Omega$	
$t_{d(on)}$	Turn-On Delay Time	—	7.0	—	ns	$V_{DD} = 75V, V_{GS} = 10V$ ③ $I_D = 5.2A$ $R_G = 2.4\Omega$
$t_r$	Rise Time	—	6.6	—		
$t_{d(off)}$	Turn-Off Delay Time	—	13	—		
$t_f$	Fall Time	—	3.1	—		
$C_{iss}$	Input Capacitance	—	810	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ , See Fig.5 $V_{GS} = 0V, V_{DS} = 0V$ to $120V$
$C_{oss}$	Output Capacitance	—	100	—		
$C_{rfs}$	Reverse Transfer Capacitance	—	15	—		
$C_{oss}$	Effective Output Capacitance	—	97	—		
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		



## Diode Characteristics ⑥

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	8.7	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	34		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 5.2A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	57	86	ns	$T_J = 25^\circ\text{C}, I_F = 5.2A$
$Q_{rr}$	Reverse Recovery Charge	—	140	210	nC	$di/dt = 100A/\mu s$ ③



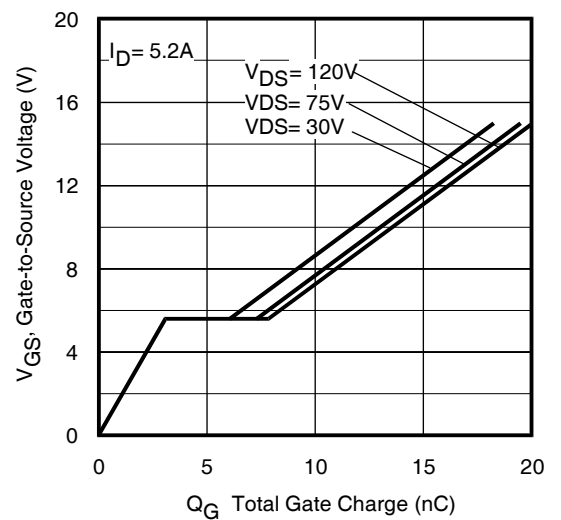
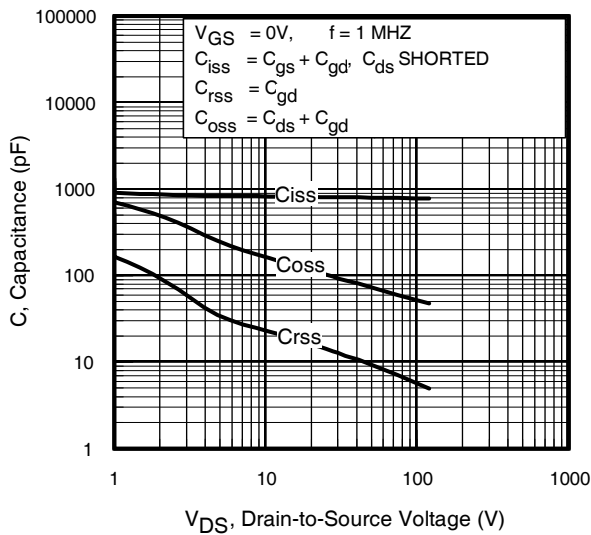
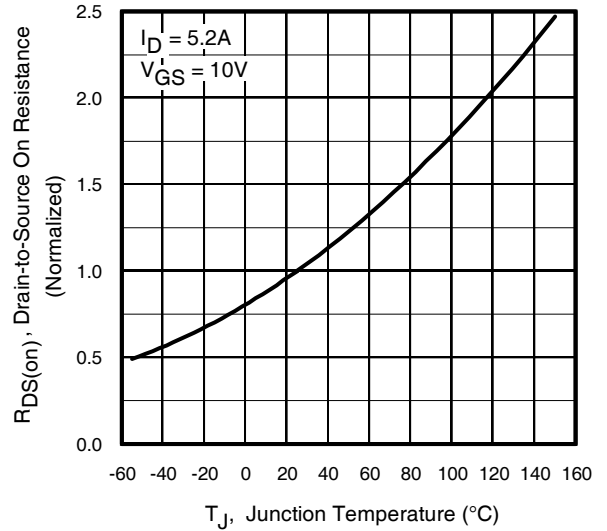
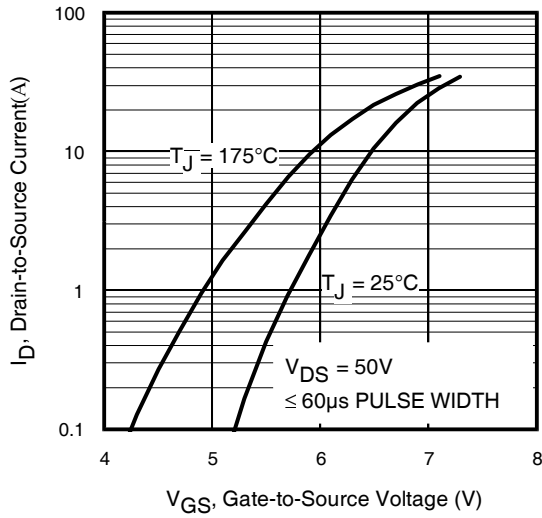
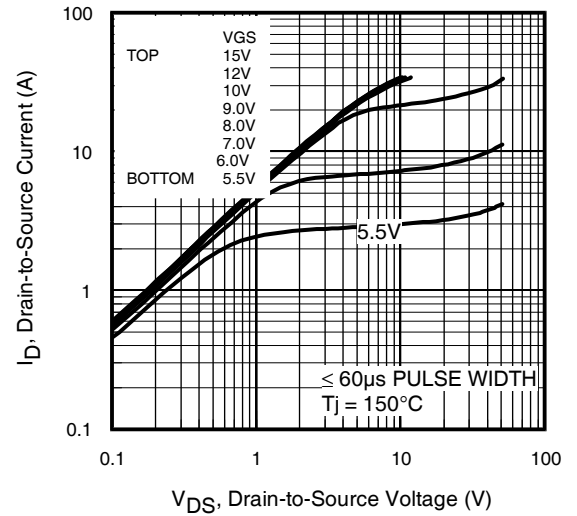
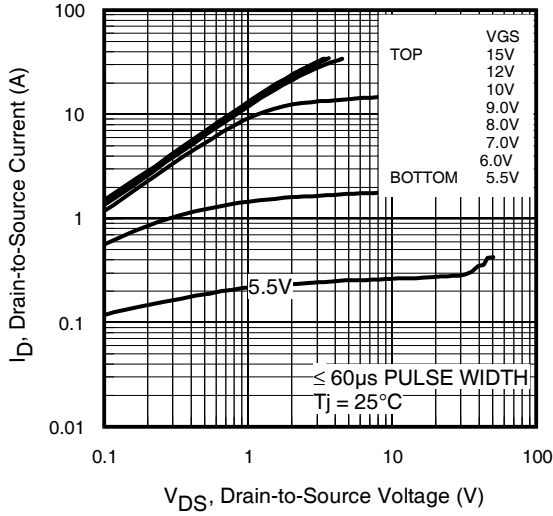
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 5.8\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 5.2A$ .
- ③ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .

④  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .

⑤ Limited by  $T_{jmax}$ . See Figs. 14, 15, 17a, 17b for repetitive avalanche information

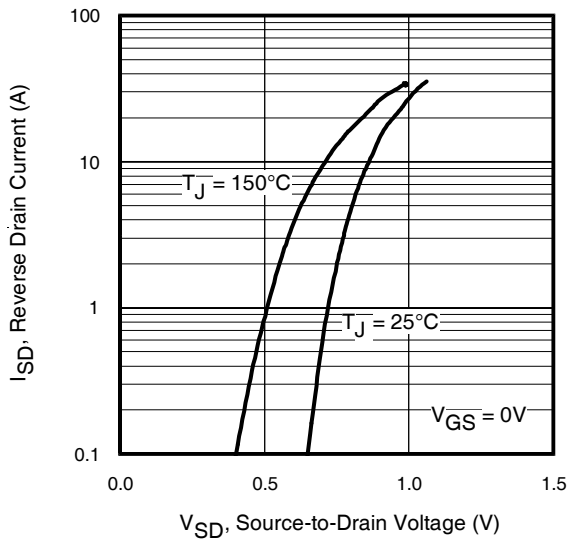
⑥ Specifications refer to single MosFET.



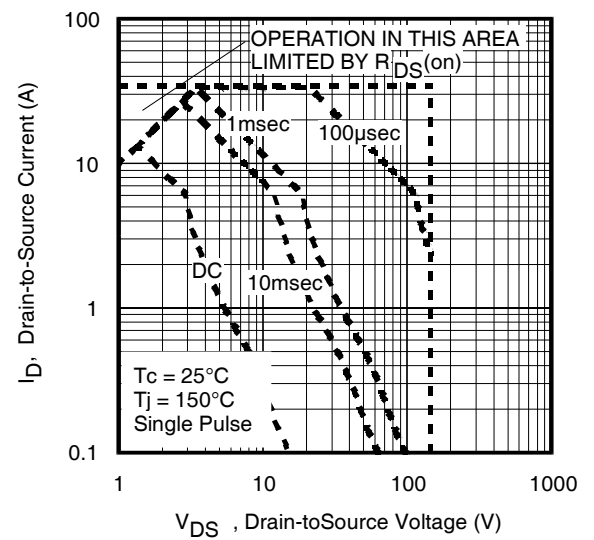
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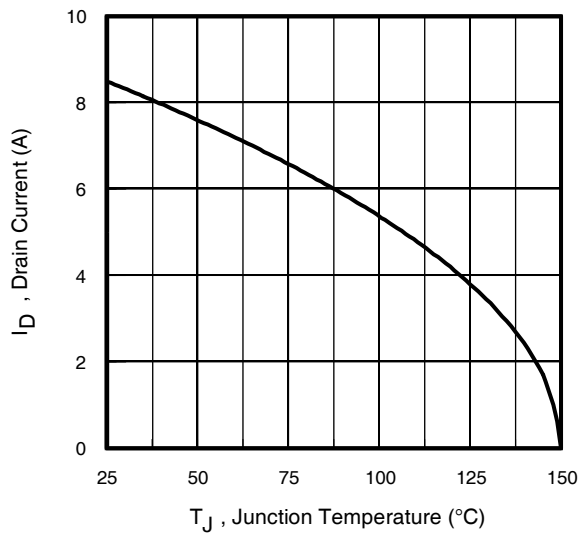
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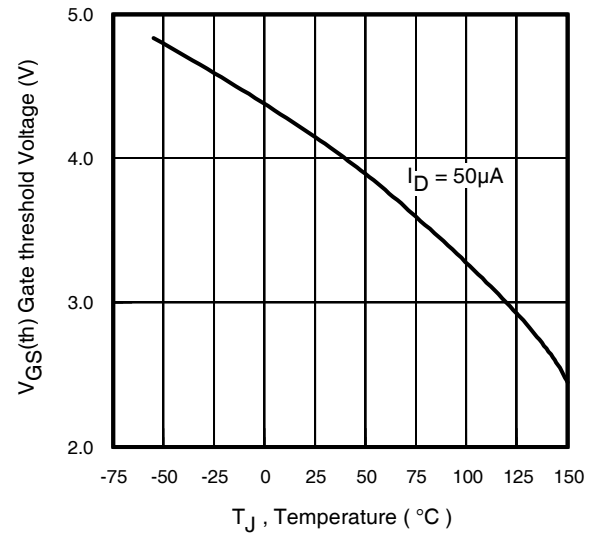
**Fig 7.** Typical Source-Drain Diode Forward Voltage



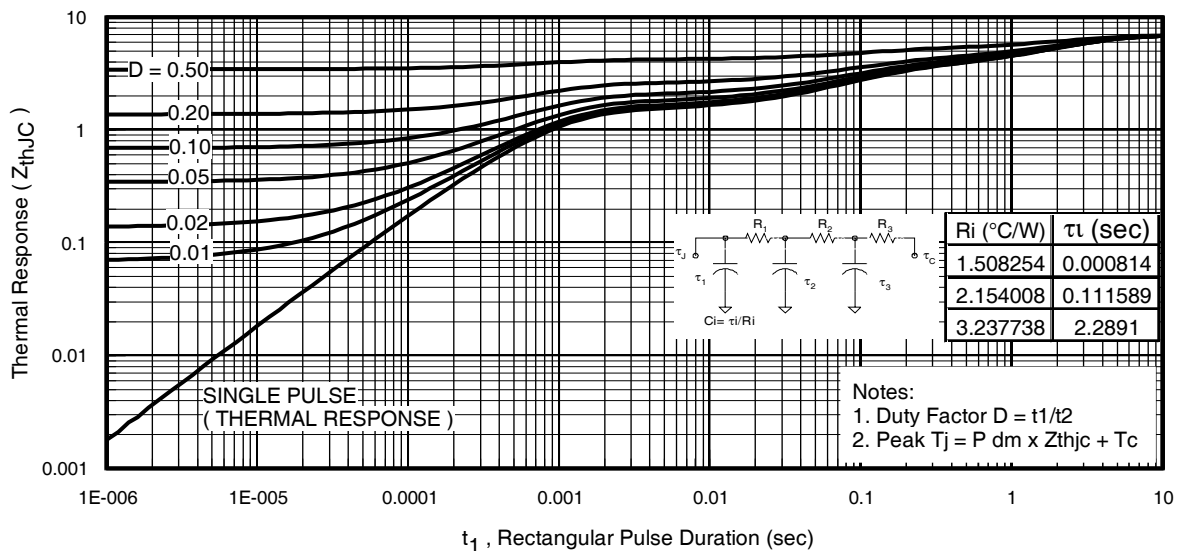
**Fig 8.** Maximum Safe Operating Area



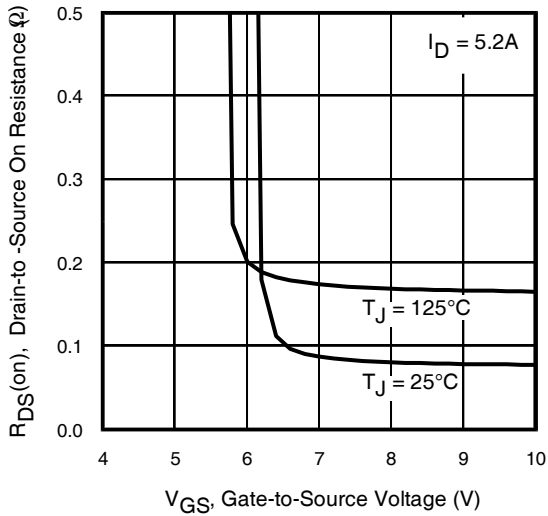
**Fig 9.** Maximum Drain Current vs. Case Temperature



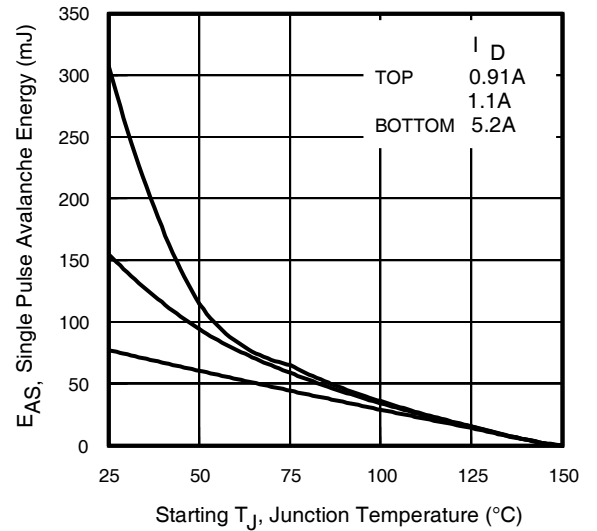
**Fig 10.** Threshold Voltage vs. Temperature



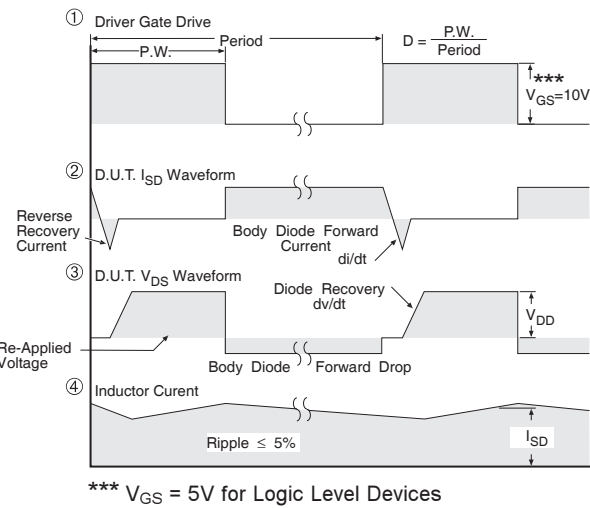
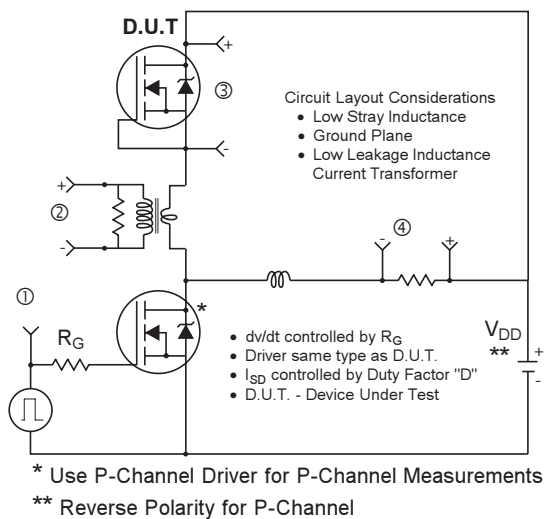
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



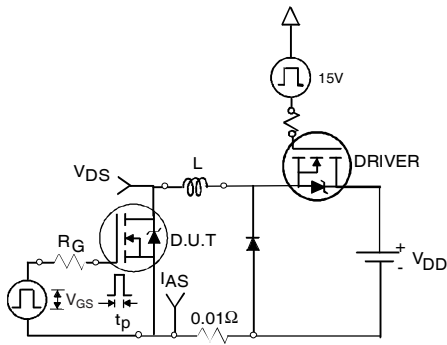
**Fig 12.** On-Resistance Vs. Gate Voltage



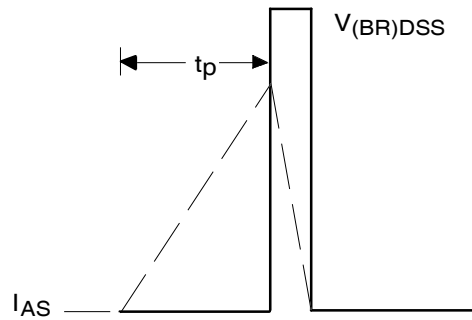
**Fig 13.** Maximum Avalanche Energy Vs. Drain Current



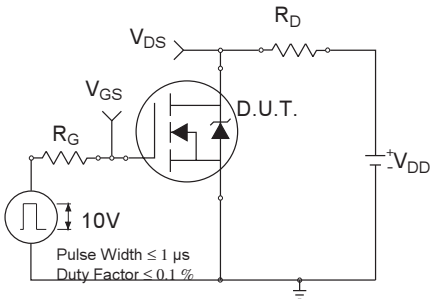
**Fig 14.** Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs



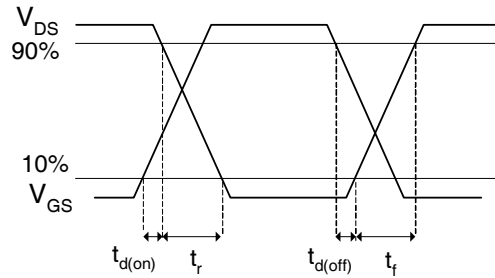
**Fig 15a.** Unclamped Inductive Test Circuit



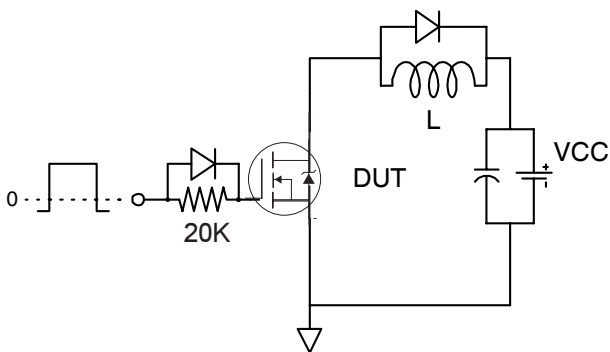
**Fig 15b.** Unclamped Inductive Waveforms



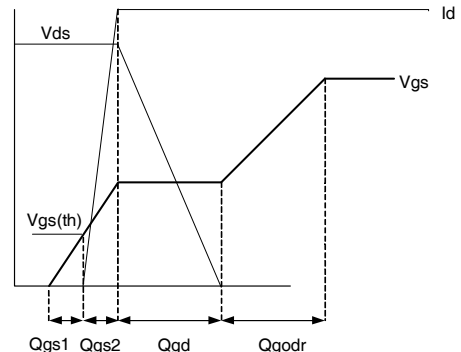
**Fig 16a.** Switching Time Test Circuit



**Fig 16b.** Switching Time Waveforms



**Fig 17a.** Gate Charge Test Circuit



**Fig 17b** Gate Charge Waveform

