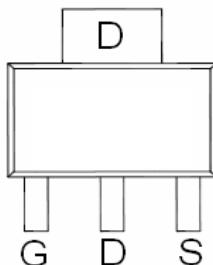
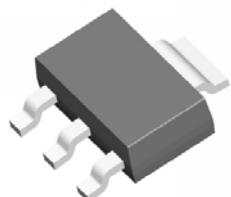
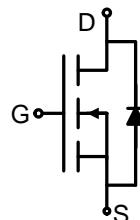


## 150V(D-S) N-Channel Enhancement Mode Power MOS FET

**General Features**

- $V_{DS} = 150V, I_D = 2A$
- $R_{DS(ON)} < 300m\Omega @ V_{GS}=10V$  (Typ:260mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

**Lead Free****Marking and pin assignment****PIN Configuration****SOT-223-3L view****Schematic diagram****Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN1502U	MSN1502U	SOT-223-3L	Ø330mm	12mm	2500 units

**Absolute Maximum Ratings ( $T_A=25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	150	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	2	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	6	A
Maximum Power Dissipation	$P_D$	2	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C

**Thermal Characteristic**

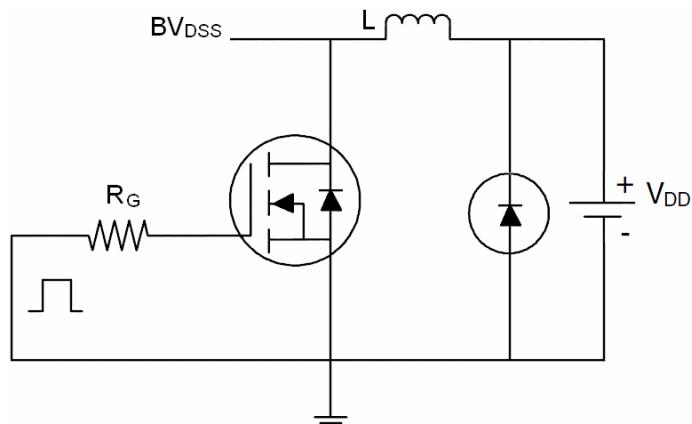
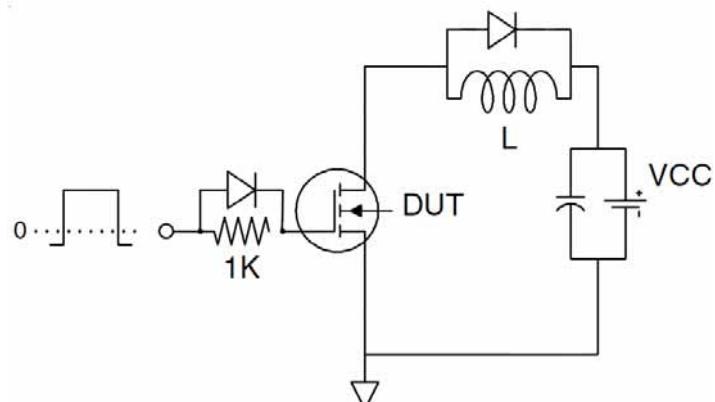
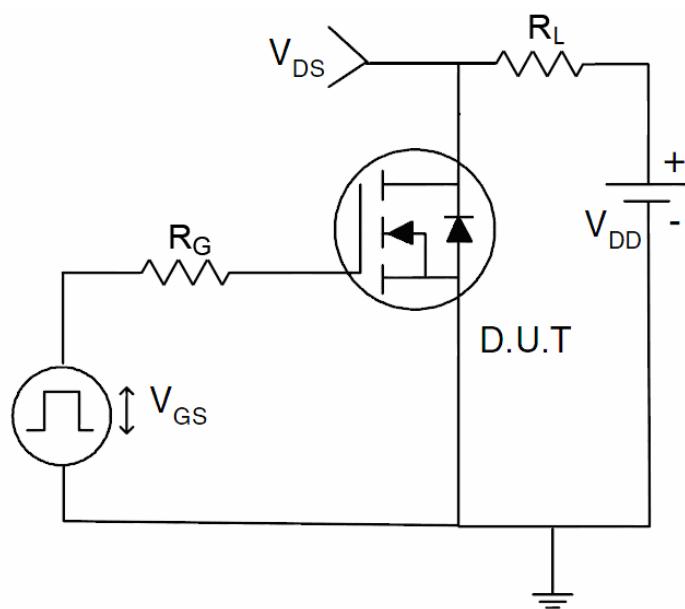
Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	62.5	°C/W
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**Electrical Characteristics ( $T_A=25^\circ\text{C}$  unless otherwise noted)**

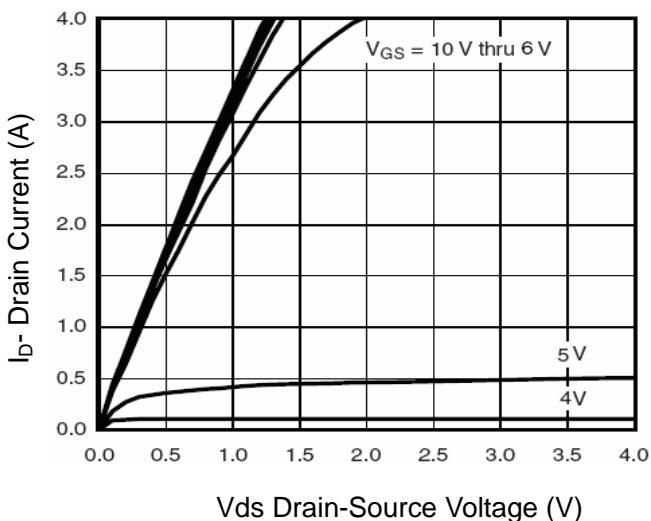
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	150	-	-	V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}}=150\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	$\mu\text{A}$
Gate-Body Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.5	2.0	2.5	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=1.5\text{A}$	-	260	300	$\text{m}\Omega$
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{DS}}=15\text{V}, I_{\text{D}}=1.5\text{A}$	-	3	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	235	-	PF
Output Capacitance	$C_{\text{oss}}$		-	36	-	PF
Reverse Transfer Capacitance	$C_{\text{rss}}$		-	20	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=75\text{V}, I_{\text{D}}=1\text{A}, R_{\text{L}}=75\Omega$ $V_{\text{GS}}=10\text{V}, R_{\text{G}}=6\Omega$	-	8	-	nS
Turn-on Rise Time	$t_{\text{r}}$		-	10	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	20	-	nS
Turn-Off Fall Time	$t_{\text{f}}$		-	15	-	nS
Total Gate Charge	$Q_{\text{g}}$	$V_{\text{DS}}=75\text{V}, I_{\text{D}}=1.5\text{A}, V_{\text{GS}}=10\text{V}$	-	8	-	nC
Gate-Source Charge	$Q_{\text{gs}}$		-	1.4	-	nC
Gate-Drain Charge	$Q_{\text{gd}}$		-	2.1	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{\text{SD}}$	$V_{\text{GS}}=0\text{V}, I_{\text{s}}=2\text{A}$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_{\text{s}}$		-	-	2	A

**Notes:**

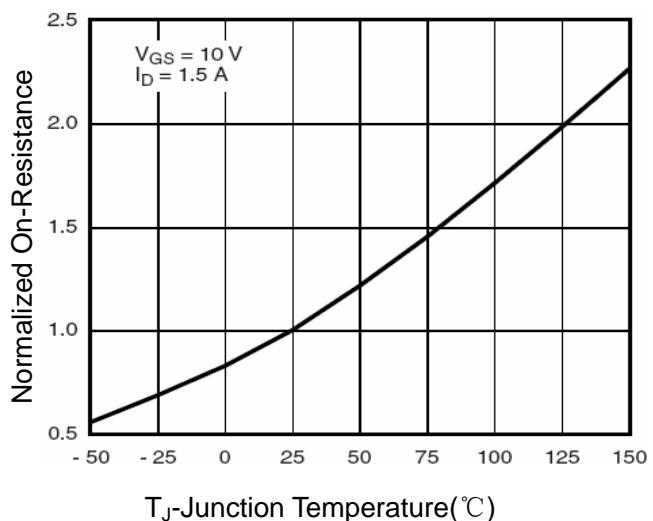
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to product

**Test Circuit****1) E<sub>AS</sub> Test Circuit****2) Gate Charge Test Circuit****3) Switch Time Test Circuit**

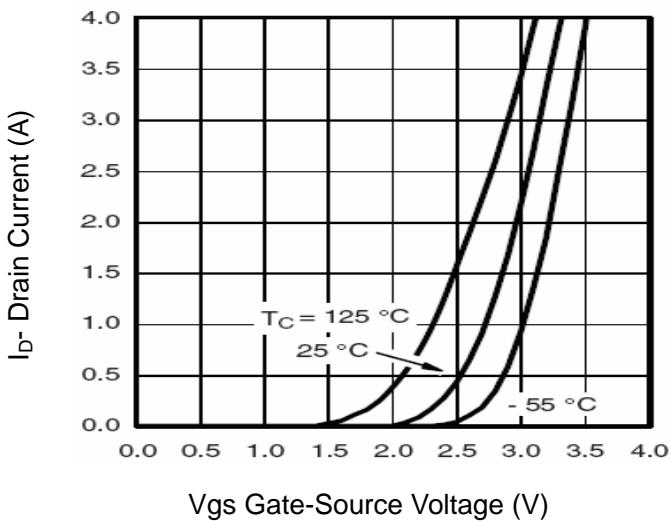
### Typical Electrical and Thermal Characteristics (Curves)



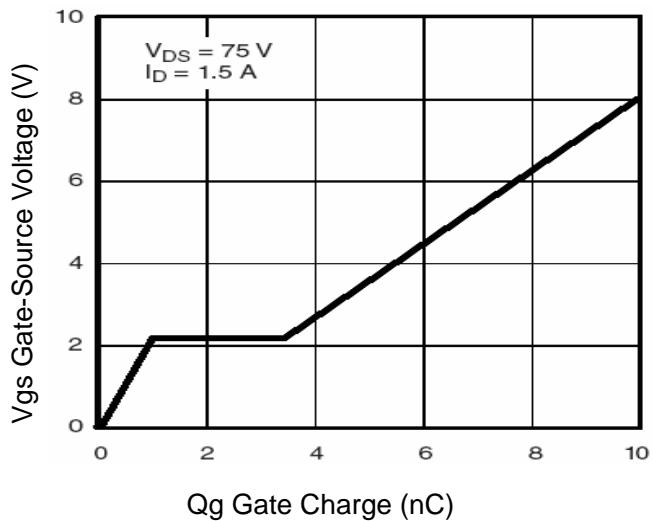
**Figure 1 Output Characteristics**



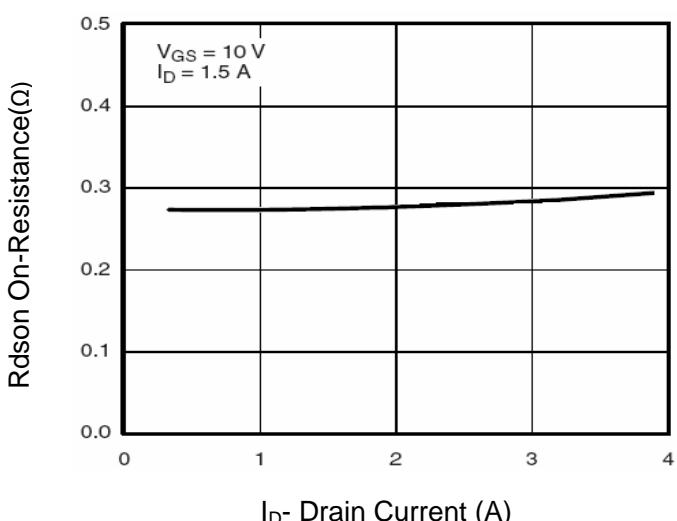
**Figure 4 Rdson- Junction Temperature**



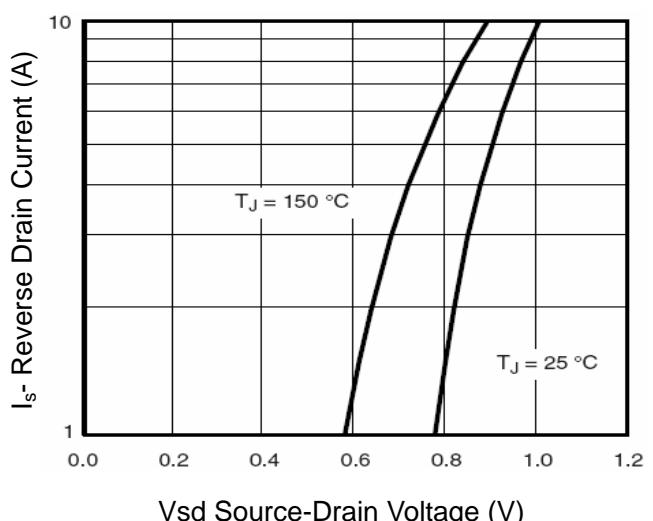
**Figure 2 Transfer Characteristics**



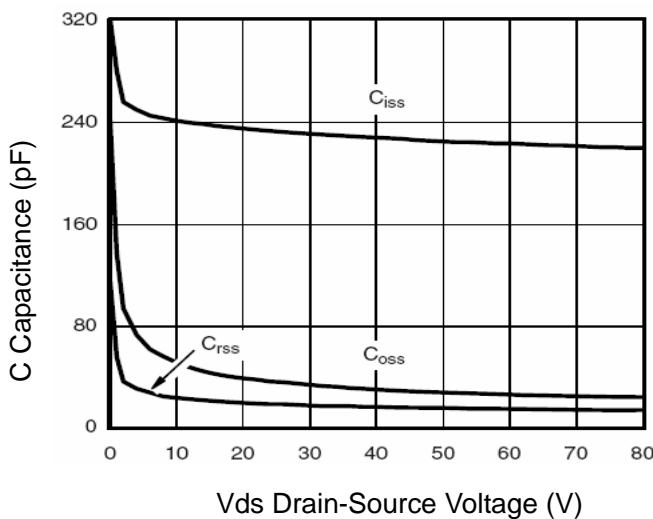
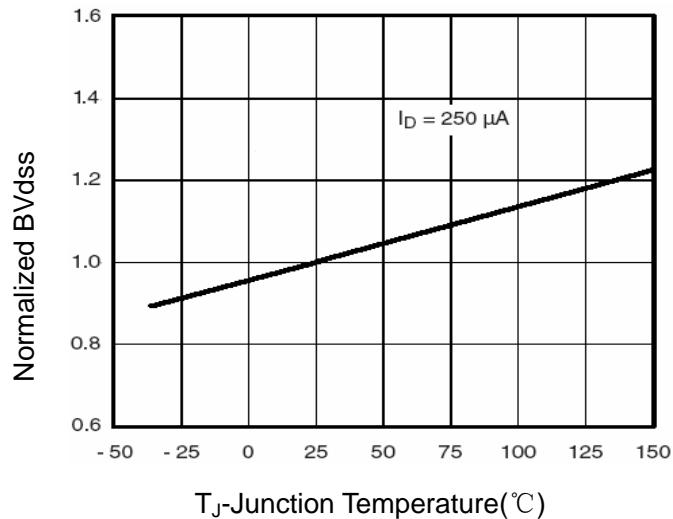
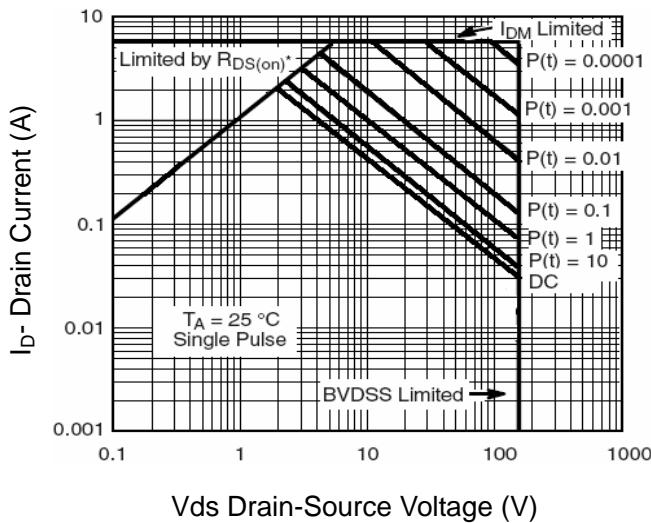
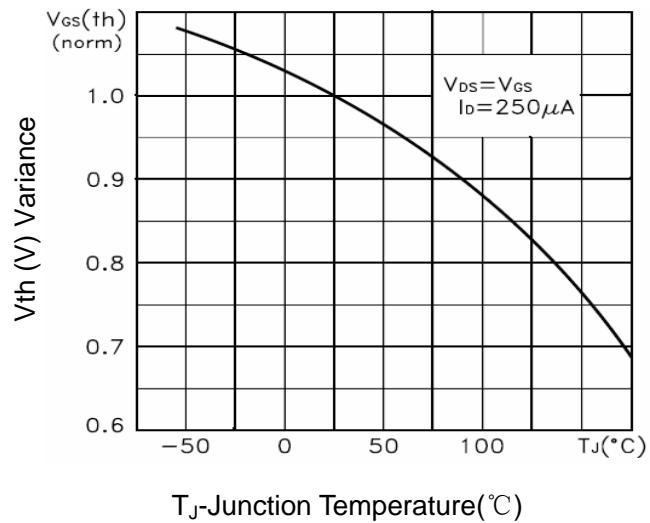
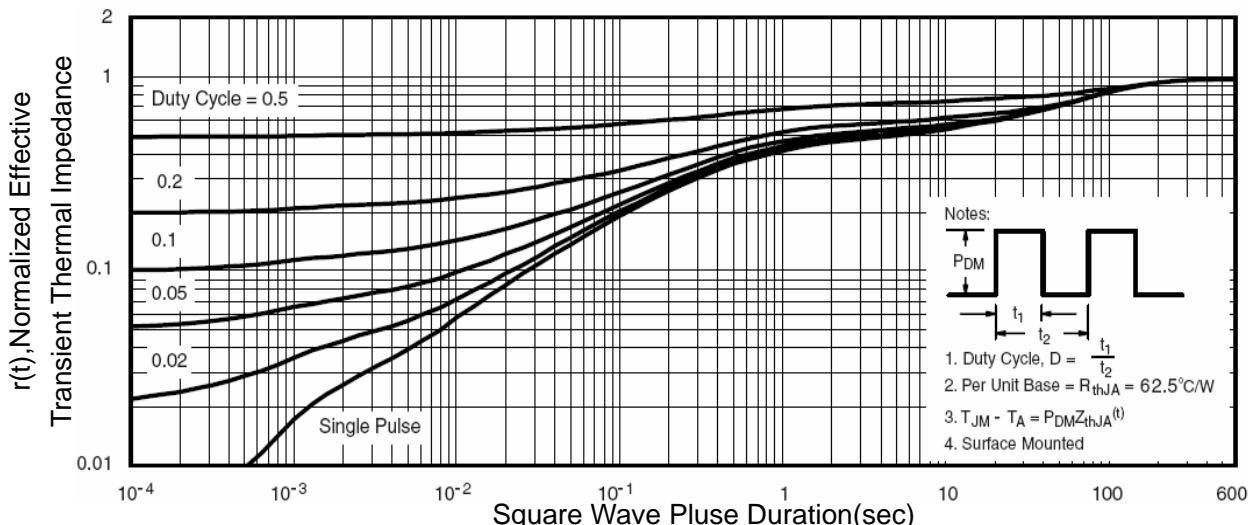
**Figure 5 Gate Charge**



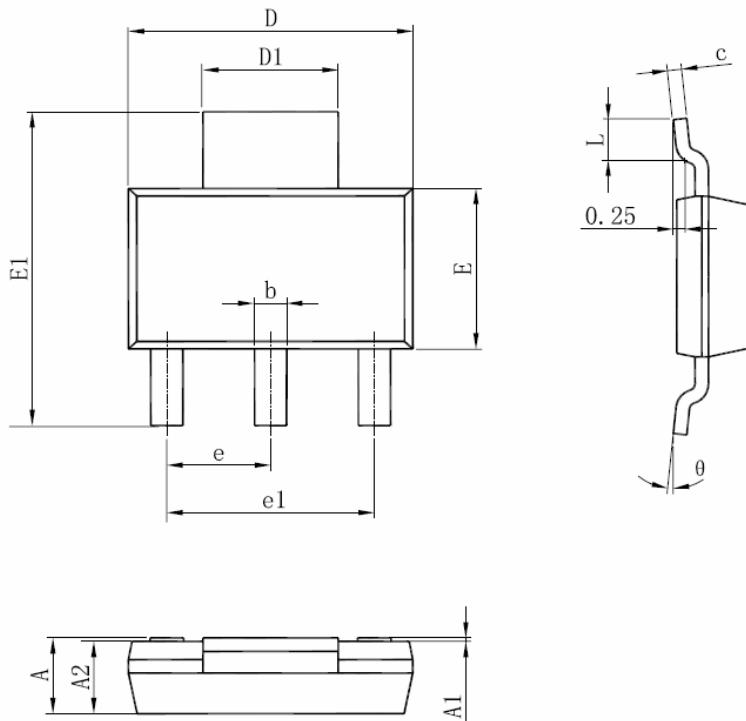
**Figure 3 Rdson- Drain Current**



**Figure 6 Source- Drain Diode Forward**

**Figure 7 Capacitance vs Vds****Figure 9  $BV_{DSS}$  vs Junction Temperature****Figure 8 Safe Operation Area****Figure 10  $V_{GS(th)}$  vs Junction Temperature****Figure 11 Normalized Maximum Transient Thermal Impedance**

## SOT-223-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.520	1.800	0.060	0.071
A1	0.000	0.100	0.000	0.004
A2	1.500	1.700	0.059	0.067
b	0.660	0.820	0.026	0.032
c	0.250	0.350	0.010	0.014
D	6.200	6.400	0.244	0.252
D1	2.900	3.100	0.114	0.122
E	3.300	3.700	0.130	0.146
E1	6.830	7.070	0.269	0.278
e	2.300(BSC)		0.091(BSC)	
e1	4.500	4.700	0.177	0.185
L	0.900	1.150	0.035	0.045
theta	0°	10°	0°	10°

## Notes

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10\text{mm}$  (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.