VND5T100LAJ-E

Double channel high-side driver with analog current sense for 24 V automotive applications

Datasheet − production data

Features

Max transient supply voltage	V_{CC}	58 V
Operating voltage range	V_{CC}	8 to 36 V
Typ on-state resistance (per ch.)	R_{ON}	100 mΩ
Current limitation (typ)	I_{LIM}	22 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected.

- General
  - Very low standby current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - Compliance with European directive 2002/95/EC
  - Fault reset standby pin (FR_Stby)
  - Optimized for LED application
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide range currents
  - Off-state open-load detection
  - Output short to V_{CC} detection
  - Overload and short to ground latch-off
  - Thermal shutdown latch-off
  - Very low current sense leakage
- Protection
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shutdown
  - Electrostatic discharge protection

PowerSSO-12

Application

All types of resistive, inductive and capacitive loads

Description

The VND5T100LAJ-E is a monolithic device made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes.

This device integrates an analog current sense which delivers a current proportional to the load current.

Fault conditions such as overload, overtemperature or short to V_{CC} are reported via the current sense pin.

Output current limitation protects the device in overload condition. The device latches off in case of overload or thermal shutdown.

The device is reset by a low level pass on the fault reset standby pin.

A permanent low level on the inputs and fault reset standby pin disables all outputs and sets the device in standby mode.

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1 Block diagram and pin description

Figure 1. Block diagram

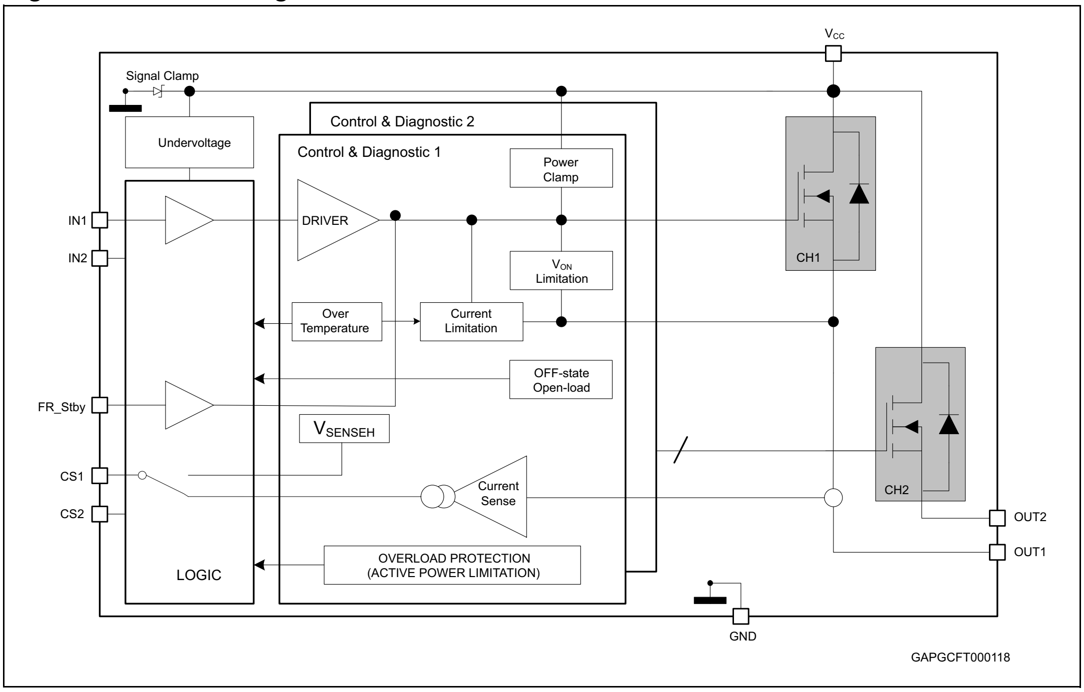


Table 1. Pin function

Name	Function
V_{CC}	Battery connection
OUTn	Power output
GND	Ground connection
INn	Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state
CSn	Analog current sense pin, it delivers a current proportional to the load current
FR_Stby	In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_Stby pin are low.

Figure 2. Configuration diagram (top view)

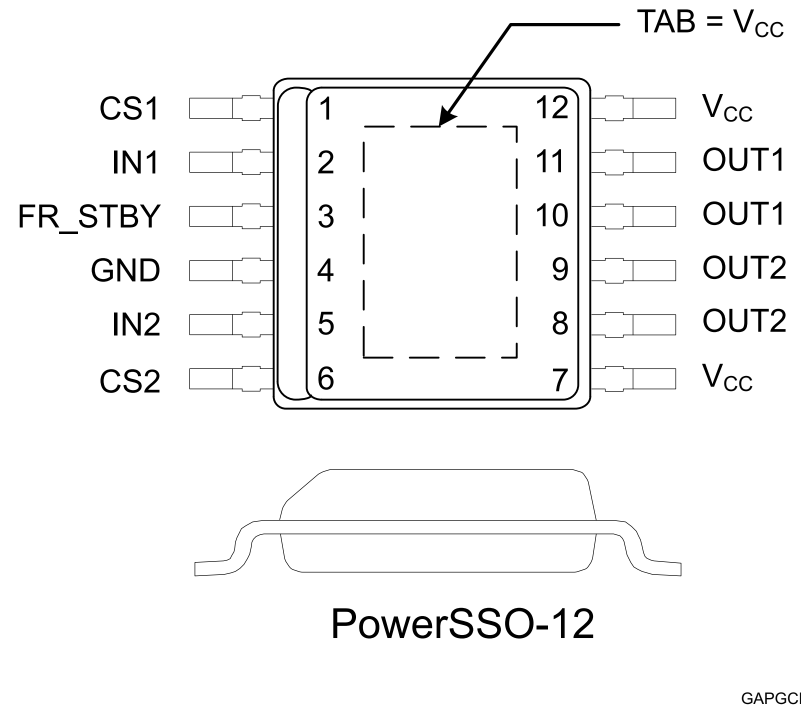


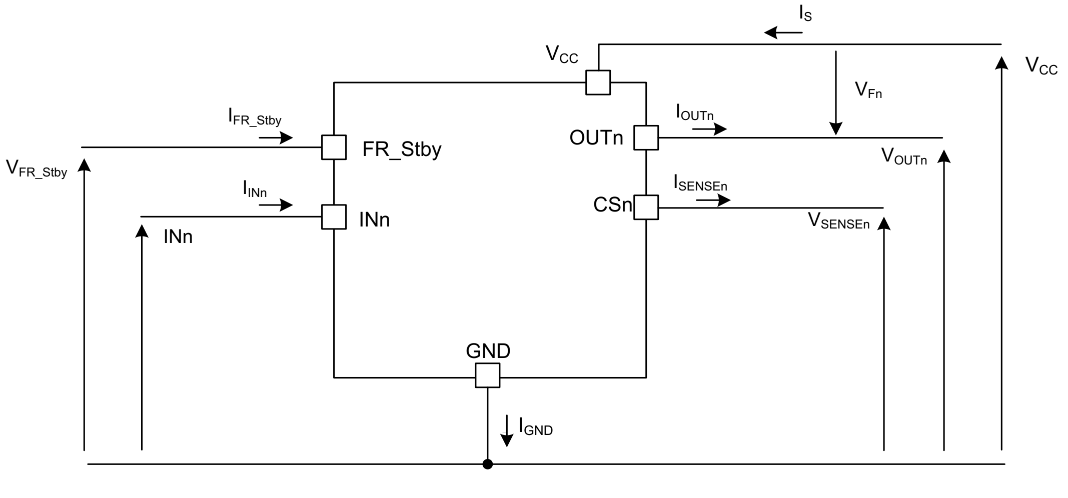
Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	FR_Stby
Floating	Not allowed	X(1)	X	X	X
To ground	Through 10 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ resistor

1. X: do not care.

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	58	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	20	A
I_{IN}	DC input current	-1 to 10	mA
I_{FR_Stby}	Fault reset standby DC input current	-1 to 1.5	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 58 to $+V_{CC}$	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (L = 1.9 mH; V_{bat} = 32 V; T_{jstart} = 150°C; I_{OUT} = I_{limL} (Typ))	70	mJ
V_{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF) – INPUT – CURRENT SENSE – FR_STBY – OUTPUT – V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C
L_{Smax}	Maximum stray inductance in short circuit R_L = 300 mΩ, V_{bat} = 32 V, T_{jstart} = 150°C, I_{OUT} = $I_{limHmax}$	40	µH

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Maximum value	Unit
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	3	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	See *Figure 27*	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 36 V; -40°C < T_j < 150°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		8	24	36	V
V_{USD}	Undervoltage shutdown			3.5	5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance(1)	I_{OUT} = 1.5 A; T_j = 25°C		100		mΩ
		I_{OUT} = 1.5 A; T_j = 150°C			200	mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA	58	64	70	V
I_S	Supply current	Off-state: V_{CC} = 24 V; T_j = 25°C; V_{IN} = V_{OUT} = V_{SENSE} = 0 V		2(2)	5(2)	µA
		On-state: V_{CC} = 24 V; V_{IN} = 5 V; I_{OUT} = 0 A		4.2	6	mA
$I_{L(off)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 24 V; T_j = 25°C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 24 V; T_j = 125°C	0		5	µA
V_F	Output - V_{CC} diode voltage	-I_{OUT} = 1.5 A; T_j = 150°C			0.7	V

1. For each channel.
2. PowerMos leakage included

Table 6. Switching(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 16 Ω		27		µs
$t_{d(off)}$	Turn-off delay time	R_L = 16 Ω		38		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 16 Ω		1		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 16 Ω		0.65		V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 16 Ω		0.23		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 16 Ω		0.26		mJ

1. Operating conditions: V_{CC} = 24 V; T_j = 25 °C

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		V
$V_{FR\_Stby\_L}$	Fault_reset_standby low level voltage				0.9	V
$I_{FR\_Stby\_L}$	Low level fault_reset_standby current	V_{FR_Stby} = 0.9 V	1			µA
$V_{FR\_Stby\_H}$	Fault_reset_standby high level voltage		2.1			V
$I_{FR\_Stby\_H}$	High level fault_reset_standby current	V_{FR_Stby} = 2.1 V			10	µA
$V_{FR\_Stby\ (hyst)}$	Fault_reset_standby hysteresis voltage		0.25			V
$V_{FR\_Stby\_CL}$	Fault_reset_standby clamp voltage	I_{FR_Stby} = 15 mA (t < 10 ms)	11		15	V
		I_{FR_Stby} = -1 mA		-0.7		V
t_{reset}	Overload latch-off reset time	See *Figure 4*	2		24	µs
t_{stby}	Standby delay	See *Figure 5*	120		1200	µs

Figure 4. $T_{standby}$ definition

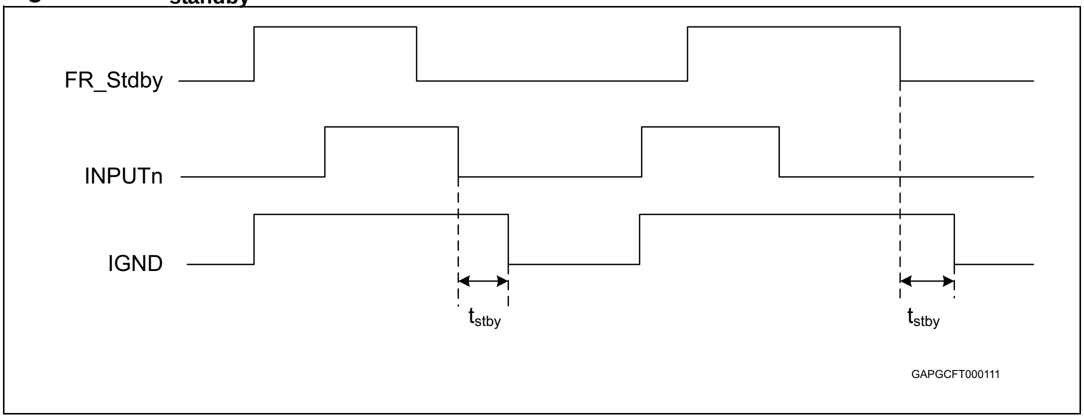


Figure 5. **T_{reset} definition**

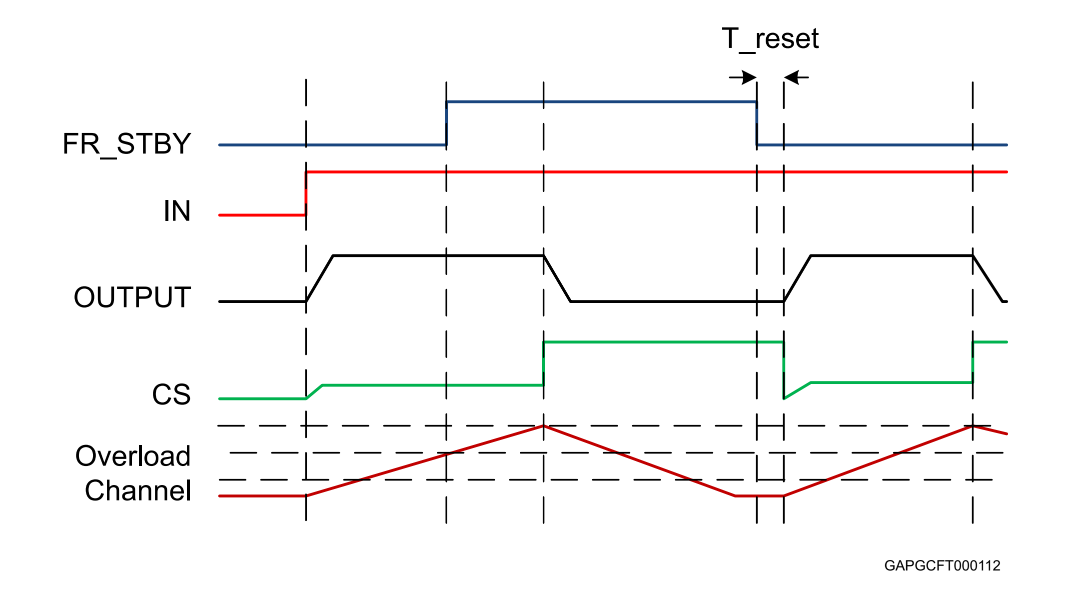


Table 8. **Protections and diagnostics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC} = 24 V	16	22	30	A
		5 V < V_{CC} < 36 V			30	A
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 24 V; $T_R < T_j < T_{TSD}$		6		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 1.5 A; V_{IN} = 0; L = 6 mH	V_{CC} - 58	V_{CC} - 64	V_{CC} - 70	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 50 mA; T_j = -40°C to 150°C		25		mV

Table 9. Current sense (8 V < V_{CC} < 36 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 12 mA; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	833			
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 50 mA; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	1328	2190	3332	
$dK_{LED}/K_{LED(TOT)}$(1)	Current sense ratio drift	I_{OUT} = 12 mA to 25 mA; I_{CAL} = 18 mA; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	-30		30	%
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 100 mA; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	1170	1950	2730	
dK_0/K_0(1)	Current sense ratio drift	I_{OUT} = 100 mA; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	-18		18	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.4 A; V_{SENSE} = 1 V; T_j = -40°C to 150°C	1259	1740	2191	
dK_1/K_1(1)	Current sense ratio drift	I_{OUT} = 0.4 A; V_{SENSE} = 1 V; T_j = -40°C to 150°C	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 0.8 A; V_{SENSE} = 2 V; T_j = -40°C to 150°C	1372	1730	2058	
dK_2/K_2(1)	Current sense ratio drift	I_{OUT} = 0.8 A; V_{SENSE} = 2 V; T_j = -40°C to 150°C	-12		12	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 1.6 A; V_{SENSE} = 2 V; T_j = -40°C to 150°C	1509	1720	1921	
dK_3/K_3(1)	Current sense ratio drift	I_{OUT} = 1.6 A; V_{SENSE} = 2 V; T_j = -40°C to 150°C	-8		8	%
K_4	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	1646	1720	1784	
dK_4/K_4(1)	Current sense ratio drift	I_{OUT} = 6 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	-4		4	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{IN} = 0 V; T_j = -40 °C to 150 °C	0		1	µA
		I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{IN} = 5 V; T_j = -40 °C to 150 °C	0		2	µA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 6 A; R_{SENSE} = 3.9 KΩ	5			V
V_{SENSEH}	Analog sense output voltage in fault condition(2)	V_{CC} = 24 V; R_{SENSE} = 3.9 KΩ	7.5	8.5	9.5	V
I_{SENSEH}	Analog sense output current in fault condition(2)	V_{CC} = 24 V; V_{SENSE} = 5 V	4.9	9	12	mA
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V; 0.07 A < I_{OUT} < 6 A; I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 6*)		100	200	µs

Table 9. Current sense (8 V < V_{CC} < 36 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V; I_{SENSE} = 90 % of $I_{SENSEMAX}$; I_{OUT} = 90 % of I_{OUTMAX}; I_{OUTMAX} = 1.5 A (see *Figure 11*)			150	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V; 0.07 A < I_{OUT} < 6 A; I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 6*)		5	20	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open-load in OFF-state condition.

Table 10. Open-load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off-state voltage detection threshold	V_{IN} = 0 V; 8 V < V_{CC} < 36 V; F_{R_STBY} = 5 V	2		4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn off	See *Figure 6*; F_{R_STBY} = 5 V	180		1800	µs
t_{DFRSTK_ON}	Output short circuit to V_{CC} detection delay at FRSTBY activation	See *Figure 9*; $Input_{1,2}$ = low			50	µs
$I_{L(off2)}$	Off-state output current at V_{OUT} = 4V	V_{IN} = 0 V; V_{SENSE} = 0 V; V_{OUT} rising from 0 V to 4 V; F_{R_STBY} = 5 V	-120		0	µA
t_{d_vol}	Delay response from output rising edge to V_{SENSE} rising edge in open-load	V_{OUT} = 4 V; V_{IN} = 0 V; V_{SENSE} = 90 % of V_{SENSEH}; R_{SENSE} = 3.9 KΩ; F_{R_STBY} = 5 V			20	µs

Figure 6. Current sense delay characteristics

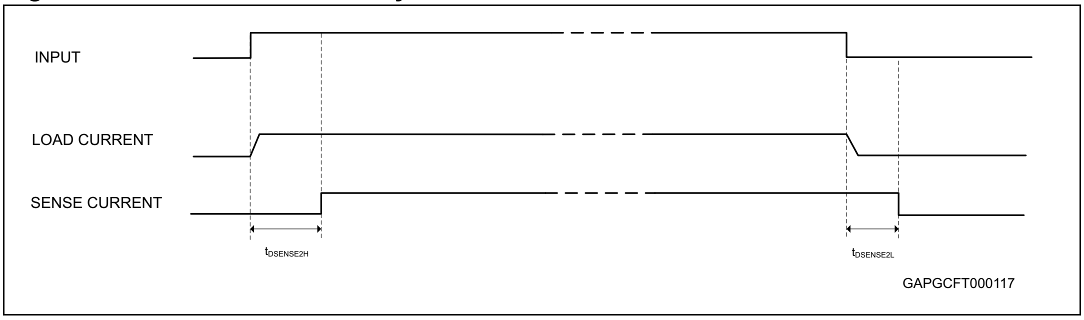


Figure 7. Open-load off-state delay timing

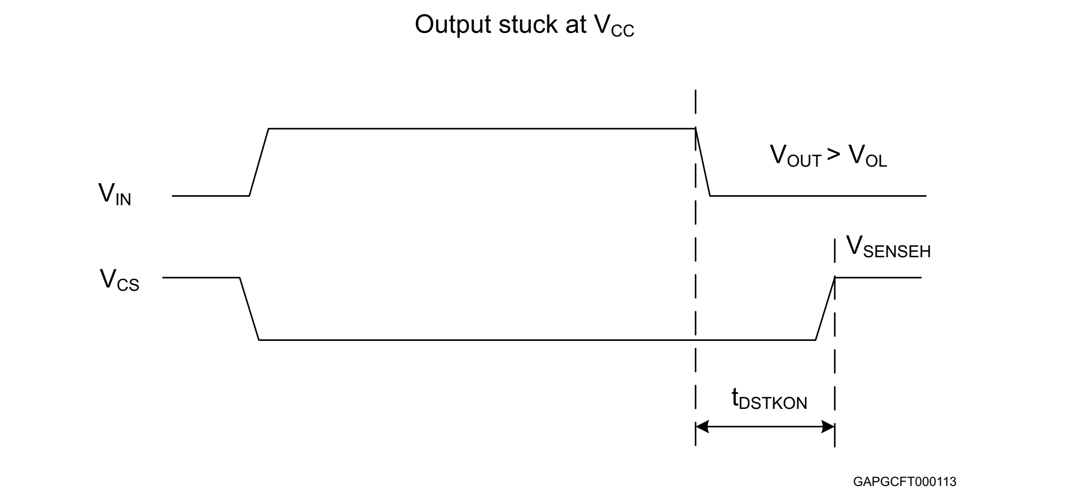


Figure 8. Switching characteristics

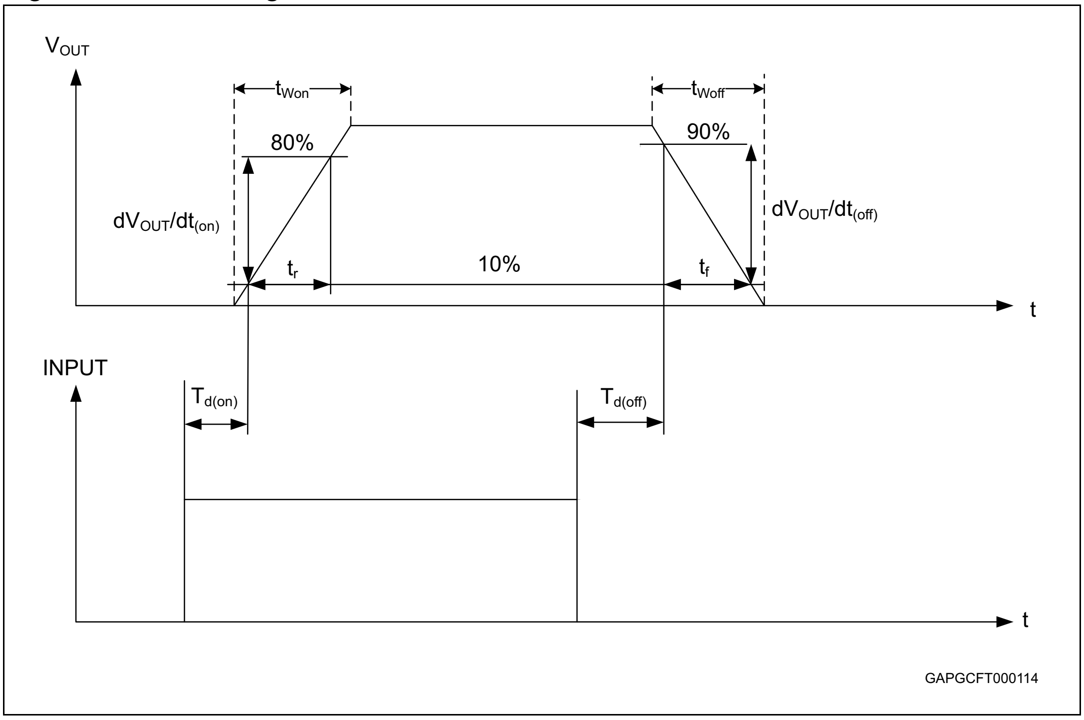


Figure 9. Output stuck to V_{CC} detection delay time at FRSTBY activation

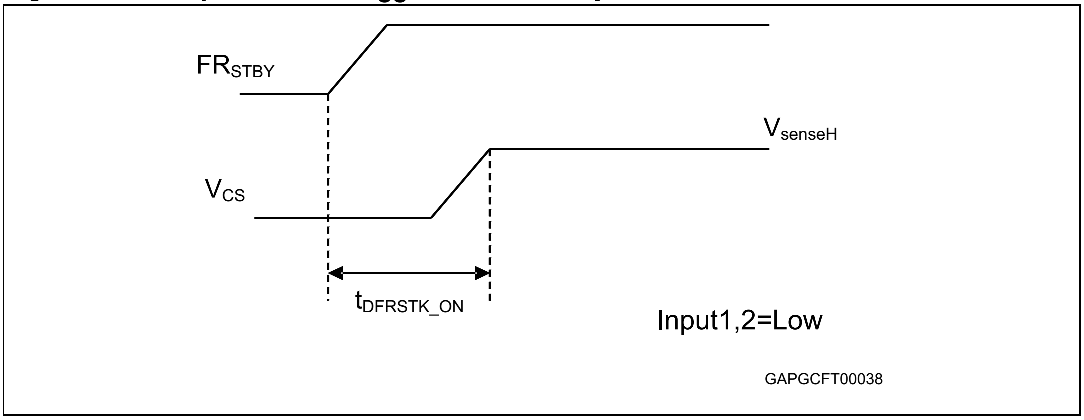


Figure 10. Delay response time between rising edge of output current and rising edge of current sense

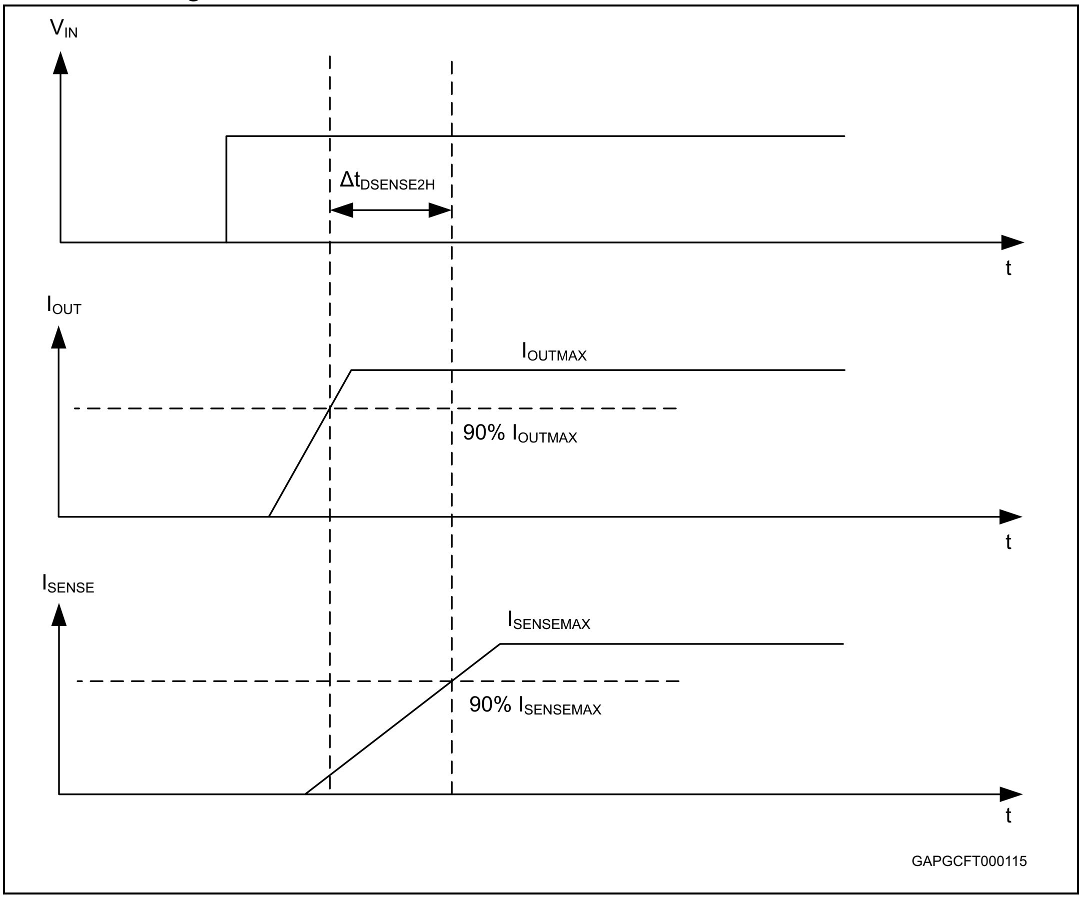


Figure 11. Output voltage drop limitation

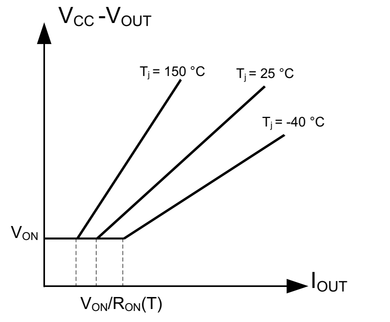
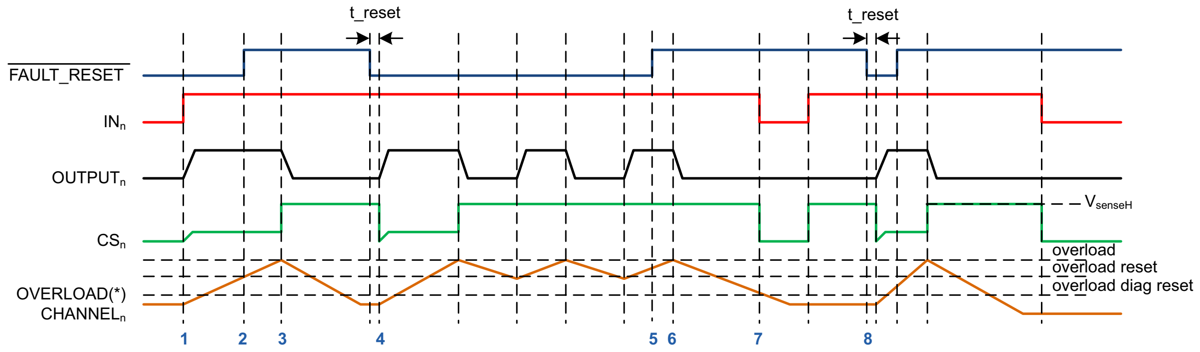


Figure 12. Device behavior in overload condition



1: $OUTPUT_n$ and CS_n controlled by INn

2: FAULT_RESET from ‘0’ to ‘1’ → no action on CS_n pin

3: overload latch-off. Inn high → CS_n high

4: FAULT_RESET low AND Temp channeln < overload_reset → overload latch reset after t_reset

4 to 5: FAULT_RESET low AND IN_n high → thermal cycling, CS_n high

5: FAULT_RESET high → latch-off reset disabled

6 to 7: overload event and FAULT_RESET high → latch-off, no thermal cycling

7 to 8: overload diagnostic disabled/enabled by the input

8: overload latch-off reset by FAULT_RESET

(*) OVERLOAD = thermal shutdown OR power limitation

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Table 11. Truth table

Conditions	Fault reset standby	Input	Output	Sense
Standby	L	L	L	0
Normal operation	X X	L H	L H	0 Nominal
Overload	X X	L H	L H	0 > Nominal
Overtemperature / short to ground	X L H	L H H	L Cycling Latched	0 V_{SENSEH} V_{SENSEH}
Undervoltage	X	X	L	0
Short to V_{BAT}	L H X	L L H	H H H	0 V_{SENSEH} < Nominal
Open-load off-state (with pull-up)	L H X	L L H	H H H	0 V_{SENSEH} 0
Negative output voltage clamp	X	L	Negative	0

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels (1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	- 450 V	- 600 V	5000 pulses	0.5 s	5 s	1 ms, 50 Ω
2a	+ 37 V	+ 50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	- 150 V	- 200 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+ 150 V	+ 200 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	- 12 V	- 16 V	1 pulse			100 ms, 0.01 Ω
5b (2)	+ 123 V	+ 174 V	1 pulse			350 ms, 1 Ω

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b(1)	E	E
3b(2)	C	C
4	C	C
5b (3)	C	C

1. Without capacitor between V_{CC} and GND.
2. With 10 nF between V_{CC} and GND.
3. External load dump clamp, 58 V maximum, referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Electrical characteristics curves

Figure 13. Off-state output current

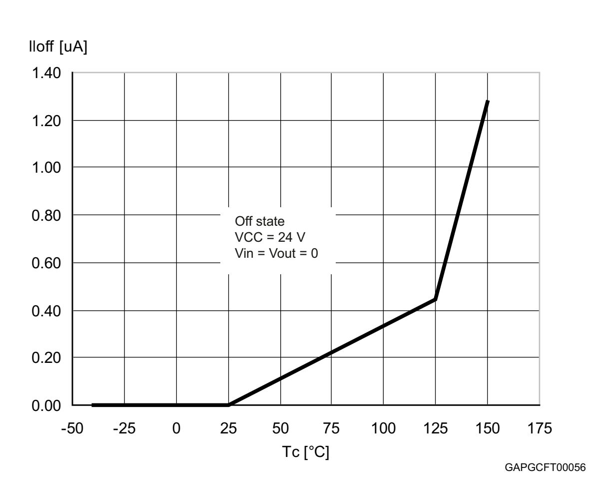


Figure 14. High level input current

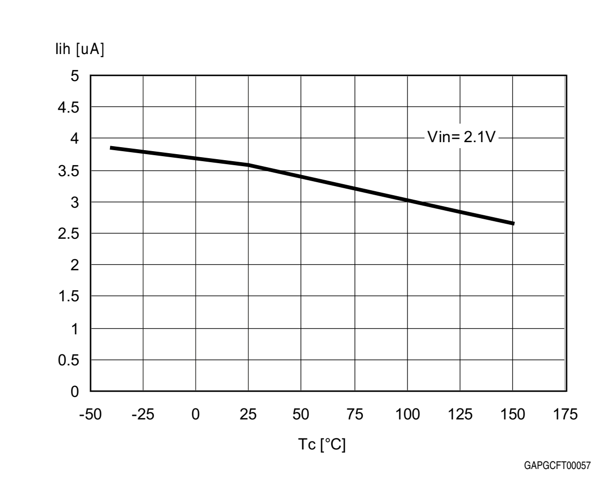


Figure 15. Input clamp voltage

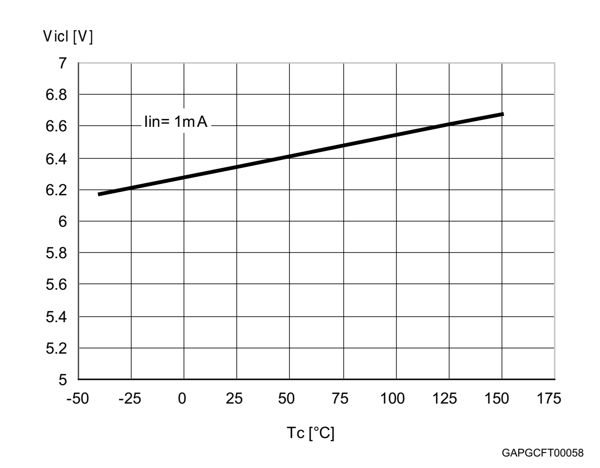


Figure 16. Input high level voltage

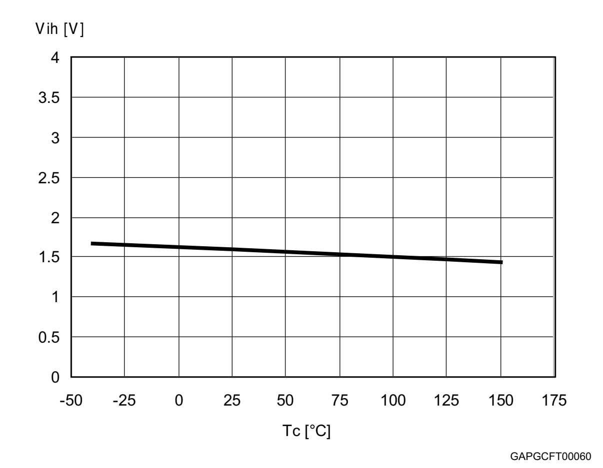


Figure 17. Input low level voltage

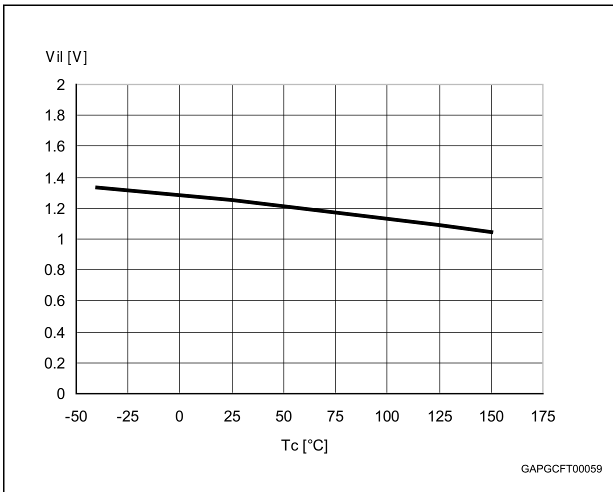


Figure 18. Input hysteresis voltage

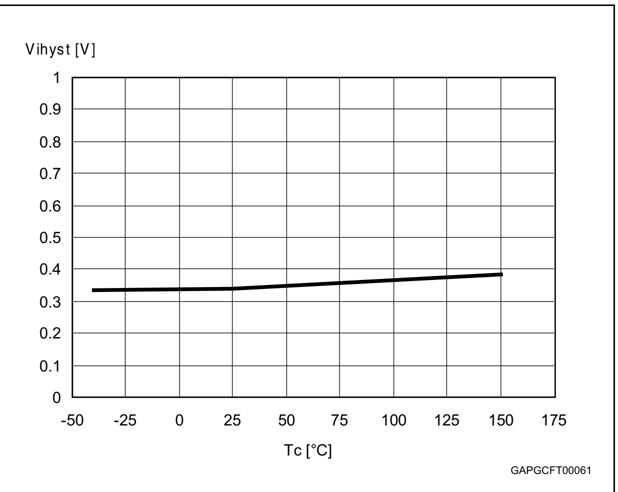


Figure 19. On-state resistance vs T_{case}

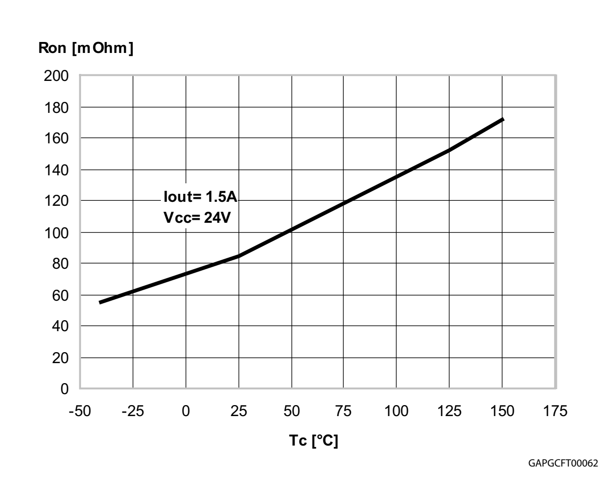


Figure 20. On-state resistance vs V_{CC}

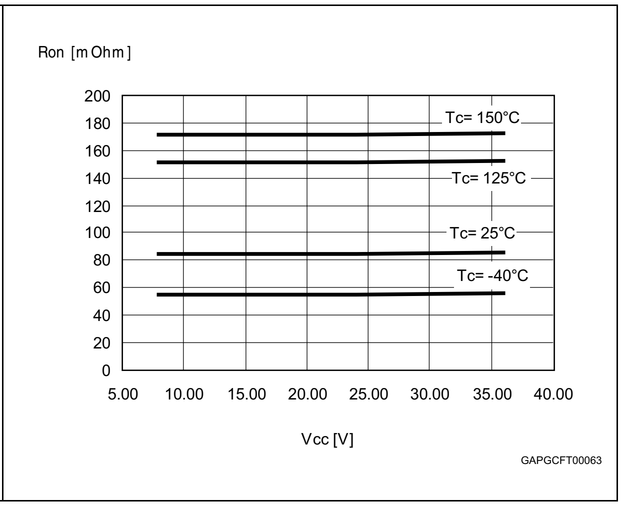


Figure 21. I_{LIMH} vs T_{case}

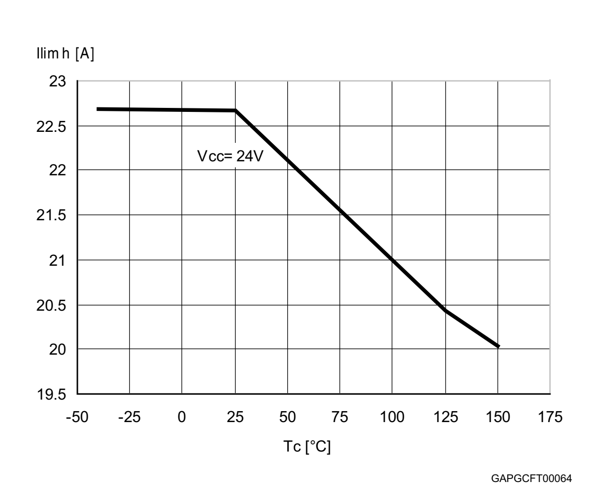


Figure 22. Turn-on voltage slope

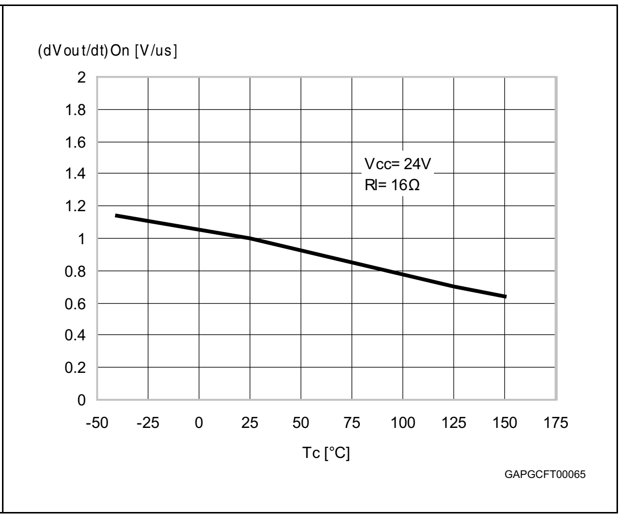
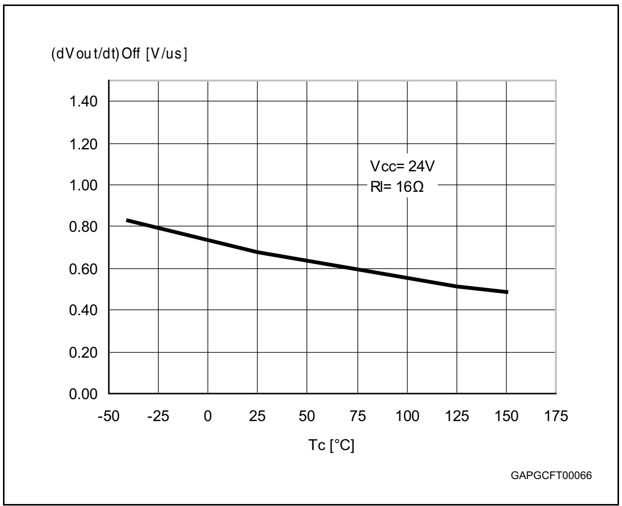
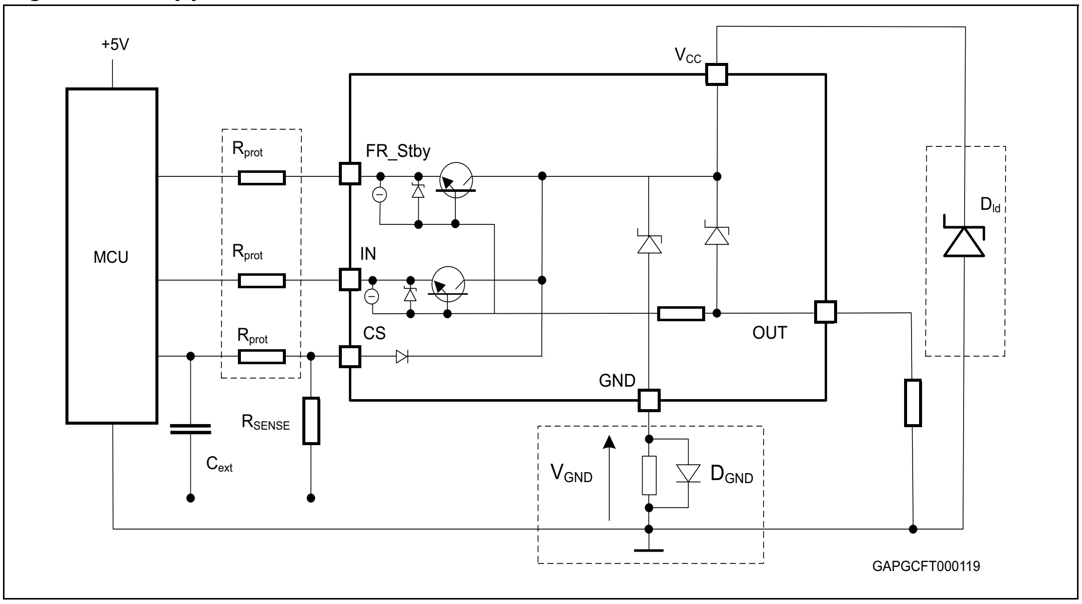


Figure 23. Turn-off voltage slope



3 Application information

Figure 24. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This solution can be used with any type of load.

The following is an indication on how to select the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$P_D = (-V_{CC})^2 / R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests Solution 2 is used (see below).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND} = 4.7 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values, if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds to V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/2 table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins are pulled negative. ST suggests that a resistor (R_{prot}) be inserted in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

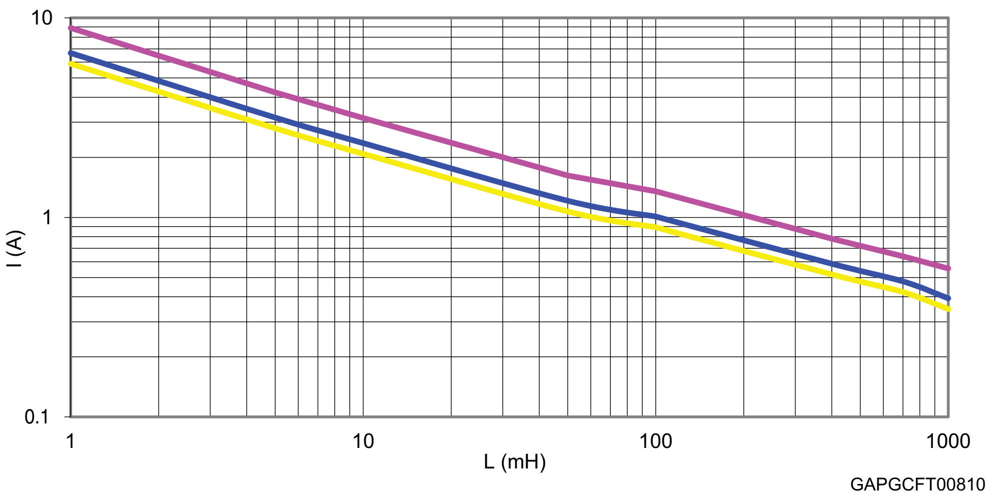
For V_{CCpeak}= -600 V and $I_{latchup} \geq 20$ mA; $V_{OH\mu C} \geq 4.5$ V

30 kΩ ≤ R_{prot} ≤ 180 kΩ.

Recommended R_{prot} value is 60 kΩ.

3.4 Maximum demagnetization energy (V_{CC} = 24 V)

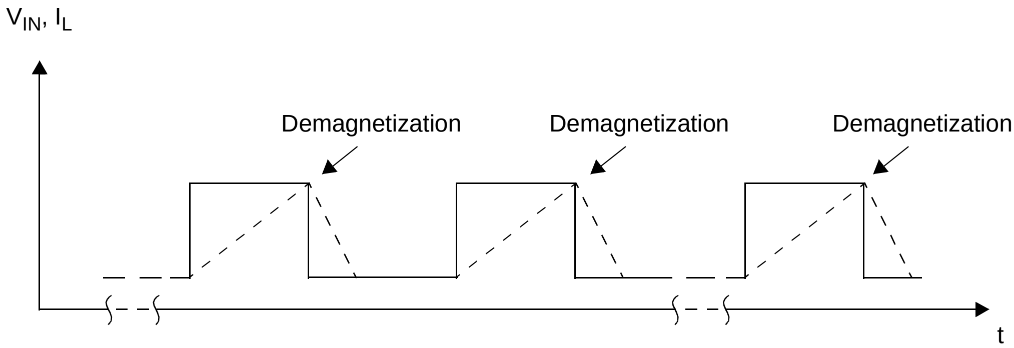
Figure 25. Maximum turn-off current versus inductance



A: T_{jstart} = 150°C single pulse

B: T_{jstart} = 100°C repetitive pulse

C: T_{jstart} = 125°C repetitive pulse

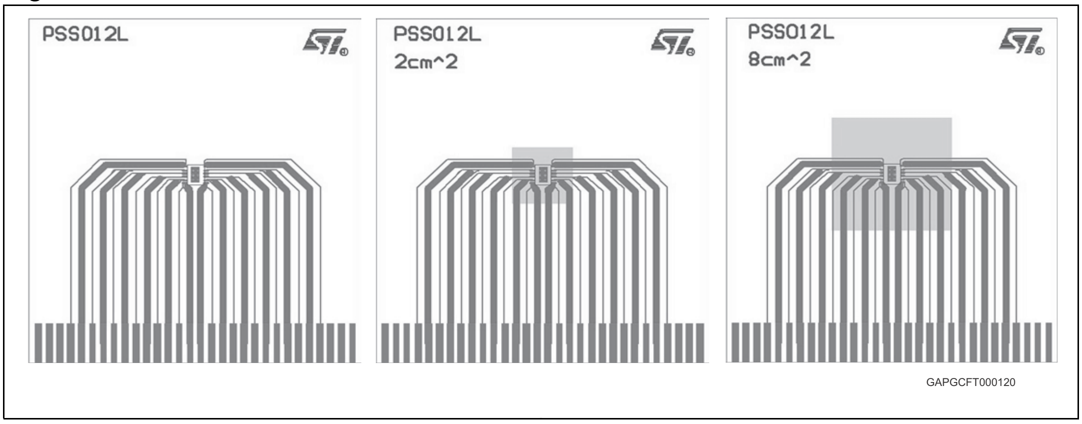


1. Values are generated with R_L =0 Ω.
In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-12 thermal data

Figure 26. PowerSSO-12 PC board



1. Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm +/- 10 %; Board double layer; Board dimension 77 mm x 86 mm; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm; Footprint dimension 4.1 mm x 6.5 mm)

Figure 27. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel ON)

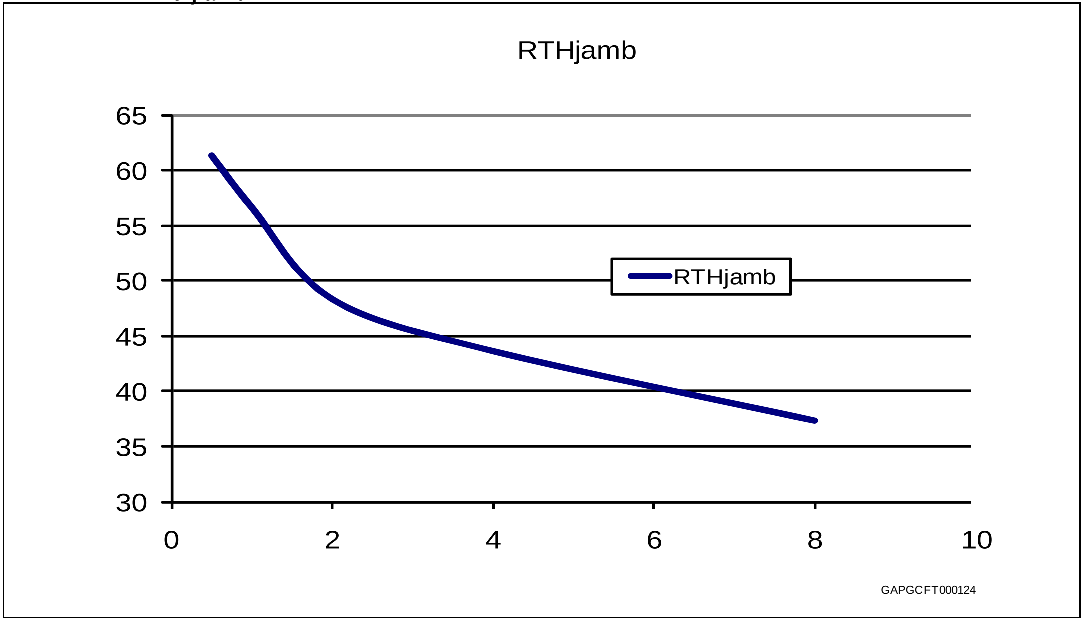


Figure 28. PowerSSO-12 thermal impedance junction ambient single pulse (one channel ON)

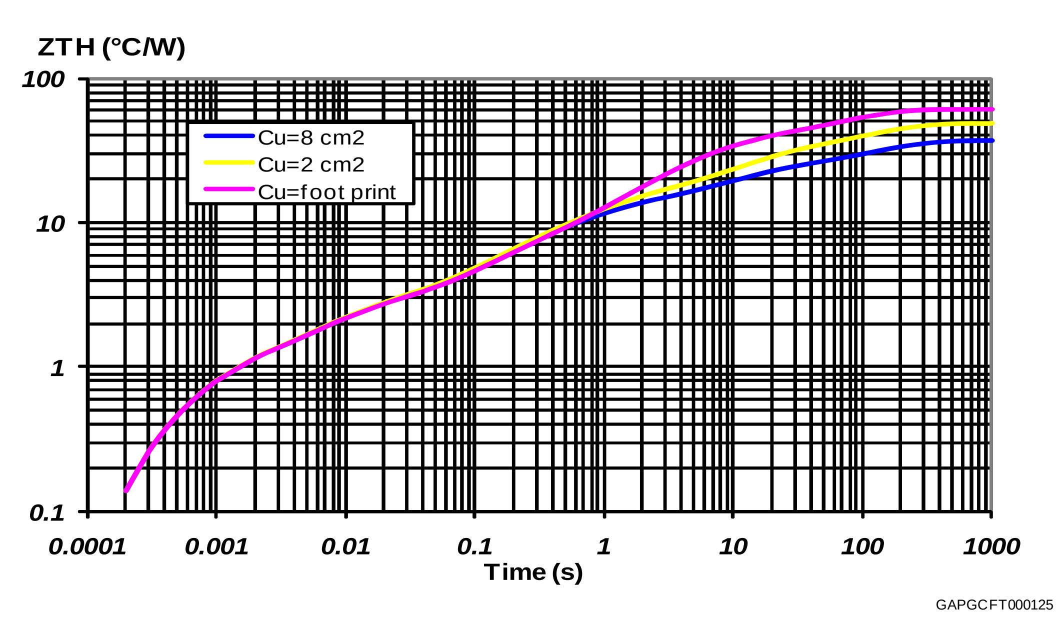
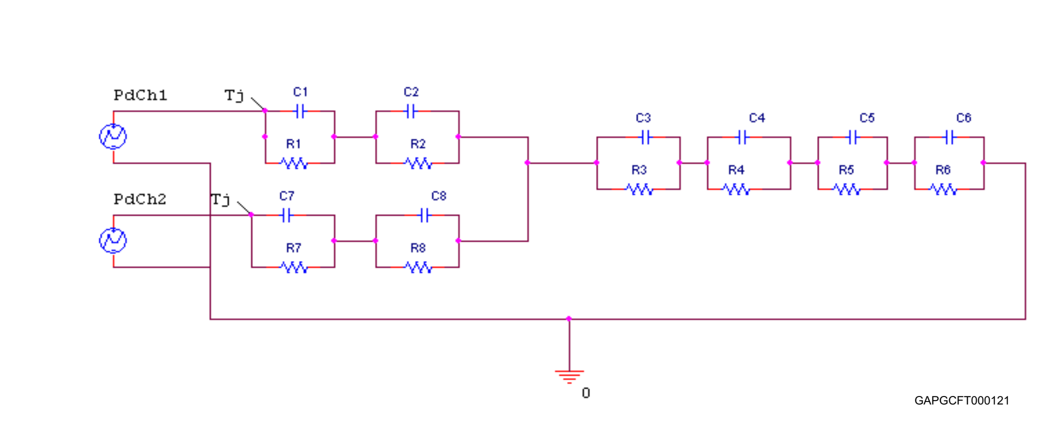


Figure 29. Thermal fitting model of a double channel HSD in PowerSSO-12



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 15. Thermal parameters

Area/island (cm^2)	Footprint	2	8
R1 = R7 (°C/W)	0.8		
R2 = R8 (°C/W)	1.5		
R3 (°C/W)	3		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 = C7 (W.s/°C)	0.0008		
C2 = C8 (W.s/°C)	0.005		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 PowerSSO-12 mechanical data

Figure 30. PowerSSO-12 package dimensions

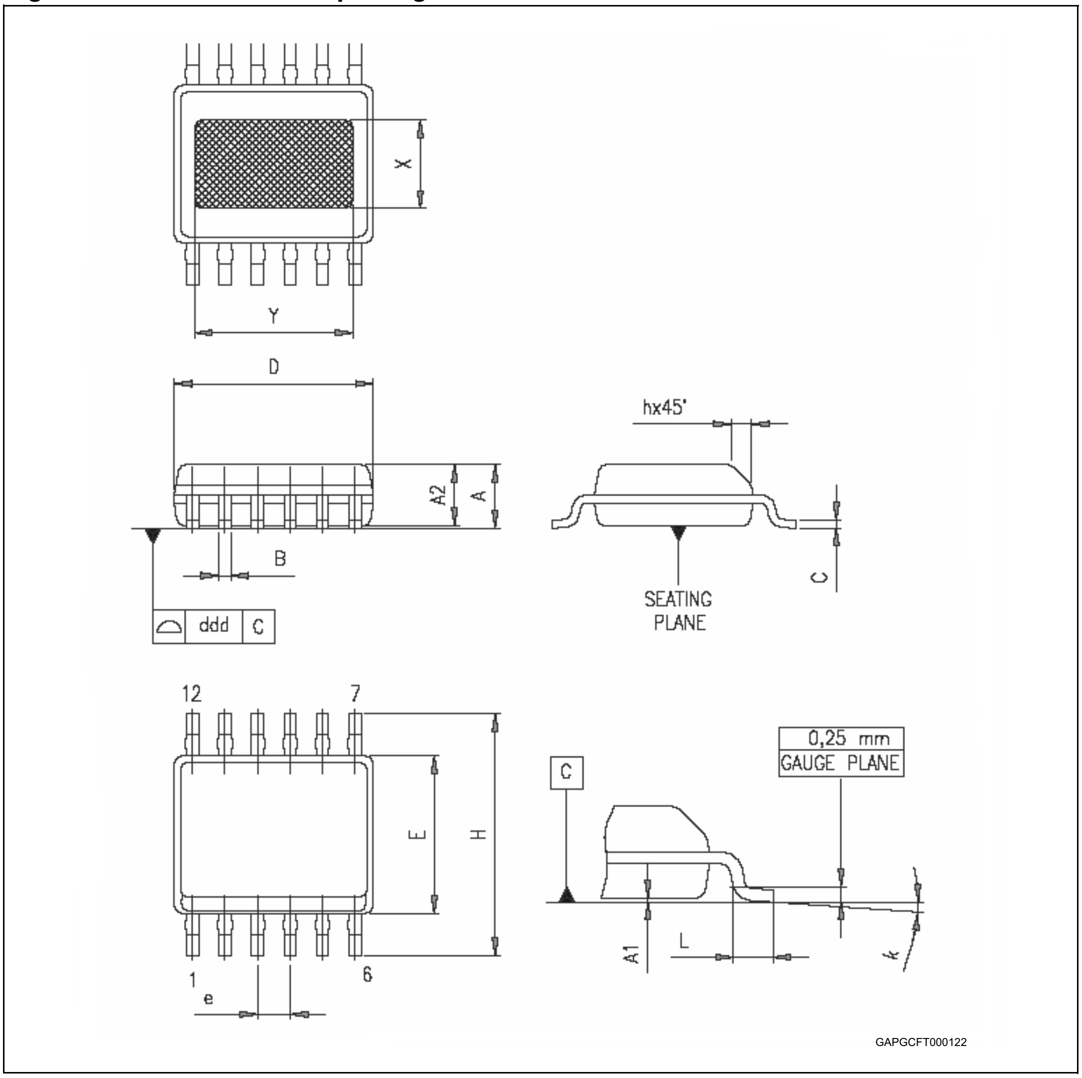
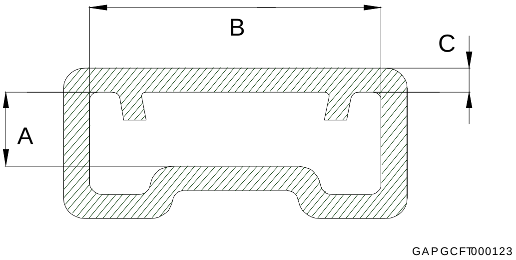


Table 16. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250	-	1.620
A1	0.000	-	0.100
A2	1.100	-	1.650
B	0.230	-	0.410
C	0.190	-	0.250
D	4.800	-	5.000
E	3.800	-	4.000
e	-	0.800	-
H	5.800	-	6.200
h	0.250	-	0.500
L	0.400	-	1.270
k	0°	-	8°
X	2.200	-	2.800
Y	2.900	-	3.500
ddd	-	-	0.100

5.3 Packing information

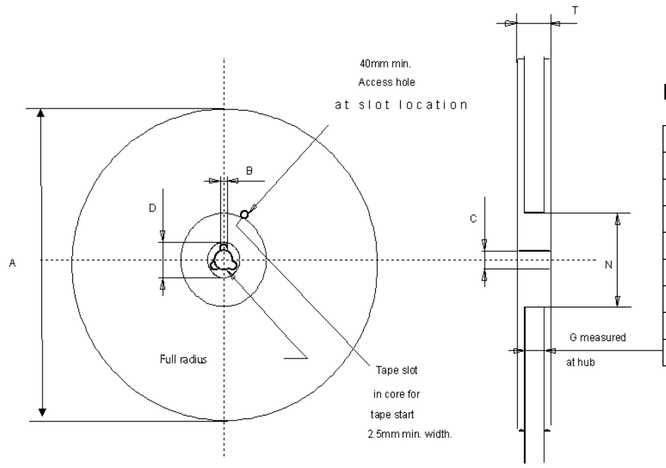
Figure 31. PowerSSO-12 tube shipment (no suffix)



All dimensions are in mm.

Base q.ty	100
Bulk q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

Figure 32. PowerSSO-12 tape and reel shipment (suffix “TR”)



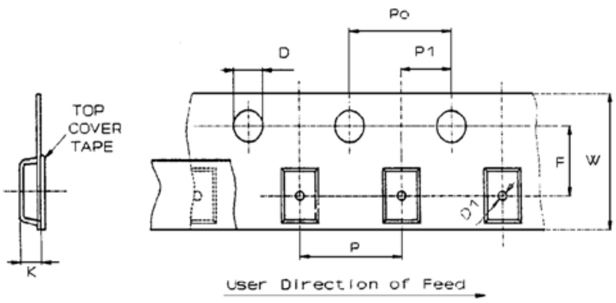
Reel dimensions

Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

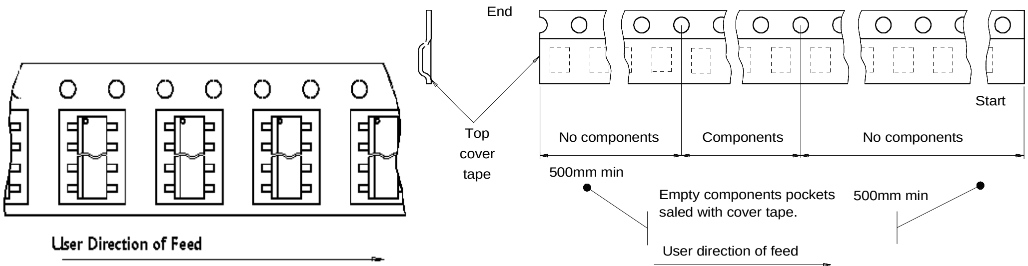
Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	8
Hole diameter	D (± 0.05)	1.5
Hole diameter	D1 (min)	1.5
Hole position	F (± 0.1)	5.5
Compartment depth	K (max)	4.5
Hole spacing	P1 (± 0.1)	2



All dimensions are in mm.



6 Order code

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-12	VND5T100LAJ-E	VND5T100LAJTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
25-Jun-2012	1	Initial release.
18-Sep-2013	2	Updated disclaimer.