LCD Driver for 160 Display Units BL55087

The BL55087 is a general COG LCD driver IC for 160 units LCD panel. It features a wide operating supply voltage range, incorporates simple communication interface with microcomputer and is suitable for multiple application.

1. Features

- Advanced low power CMOS Technology
- Selection of 1/2 or 1/3 bias, selection of 1/2 or 1/3 or 1/4 duty.
- Operation voltage: 2.5~5.5V
- I^2C data interface
- 160(40x4) Display Units
- Low power dissipation design: Power saving mode: Idd=14uA at 5V and Idd=9uA at 3.3V; Sleeping mode: Idd<2uA
- Maybe cascaded up to 2PCs for large LCD applications
- On-chip RC oscillator
- VLCD for adjusting LCD operating voltage
- Excellent EMC immunity
- Compatible with general microcomputer
- Package: COG

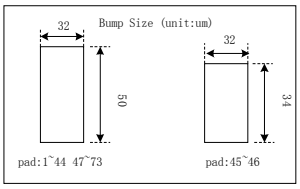
2. Pin Description

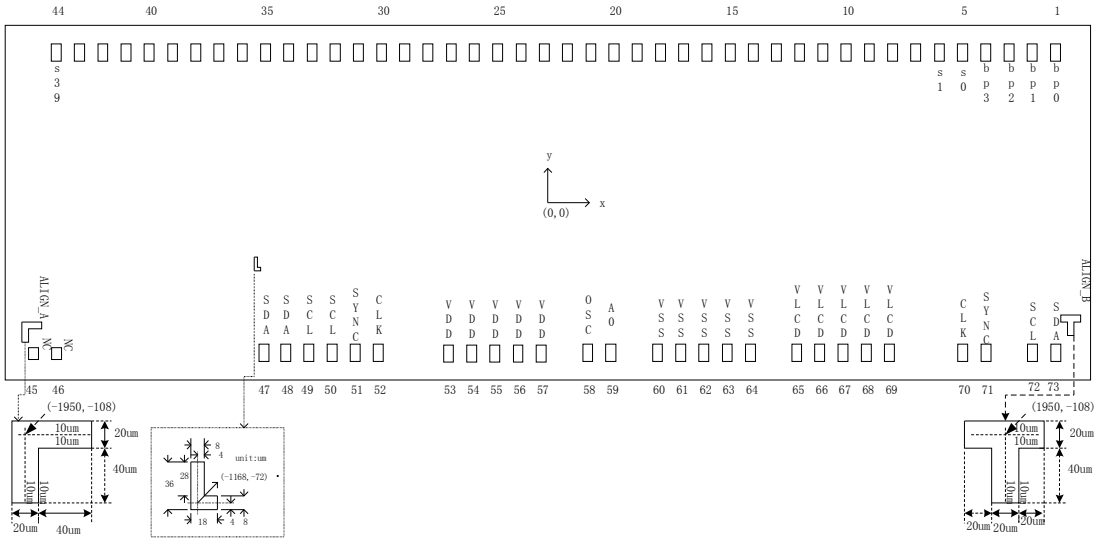
Pin No.	Pin name	Function
1~4	BP0~BP3	BP terminal driving output
5~44	S0~S39	Segment terminal driving output
45, 46	NC	
47, 48	SDA	Serial data input/output
49, 50	SCL	Serial clock input
51	SYNC	Cascade synchronization clock
52	CLK	External clock input （OSC=0:output；OSC=1:input）
53~57	Vdd	Supply voltage
58	OSC	internal oscillator enable input
59	A0	Subaddress inputs
60~64	Vss	ground
65~69	Vlcd	LCD supply voltage
70	CLK	External clock input （OSC=0:output；OSC=1:input）
71	SYNC	Cascade synchronization clock
72	SCL	Serial clock input
73	SDA	Serial data input/output

Dice Size: 4110um*680um Bump Height: 15~20um Chip Thickness: 525um
Bump Pitch: 90um(min.)

ITEM	NUMBER		SIZE		UNIT
			X	Y	
Chip Thickness			500um (暂定)		um
Pad pitch	All Pad		90		um
Bump size	Output pad	1~44	32	50	um
	In/out pad	47~52,70~73	32	50	um
	Input pad	58, 59	32	50	um
	Power/GND pad	53~57, 60~69	32	50	um
	NC	45, 46	32	34	um
Bump height	All pad		15~20		um

PIN CONFIGURATION:





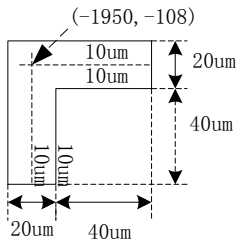
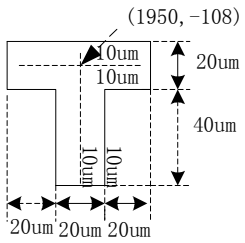
Package COG

Pad Coordinates

SYMBOL	PAD	COORDINATES	
		X	Y
BP0	1	1935	224.62
BP1	2	1845	224.62
BP2	3	1755	224.62
BP3	4	1665	224.62
S0	5	1575	224.62
S1	6	1485	224.62
S2	7	1395	224.62
S3	8	1305	224.62
S4	9	1215	224.62
S5	10	1125	224.62
S6	11	1035	224.62
S7	12	945	224.62
S8	13	855	224.62
S9	14	765	224.62
S10	15	675	224.62
S11	16	585	224.62
S12	17	495	224.62
S13	18	405	224.62
S14	19	315	224.62
S15	20	225	224.62
S16	21	135	224.62
S17	22	45	224.62
S18	23	-45	224.62
S19	24	-135	224.62
S20	25	-225	224.62
S21	26	-315	224.62
S22	27	-405	224.62
S23	28	-495	224.62
S24	29	-585	224.62
S25	30	-675	224.62
S26	31	-765	224.62
S27	32	-855	224.62
S28	33	-945	224.62
S29	34	-1035	224.62
S30	35	-1125	224.62
S31	36	-1215	224.62
S32	37	-1305	224.62
S33	38	-1395	224.62
S34	39	-1485	224.62
S35	40	-1575	224.62
S36	41	-1665	224.62
S37	42	-1755	224.62
S38	43	-1845	224.62
S39	44	-1935	224.62
NC	45	-1952.53	-202.17
NC	46	-1862.53	-202.17
SDA	47	-1145.93	-194.17
SDA	48	-1055.93	-194.17
SCL	49	-965.93	-194.17
SCL	50	-875.93	-194.17
SYNC	51	-785.93	-194.17

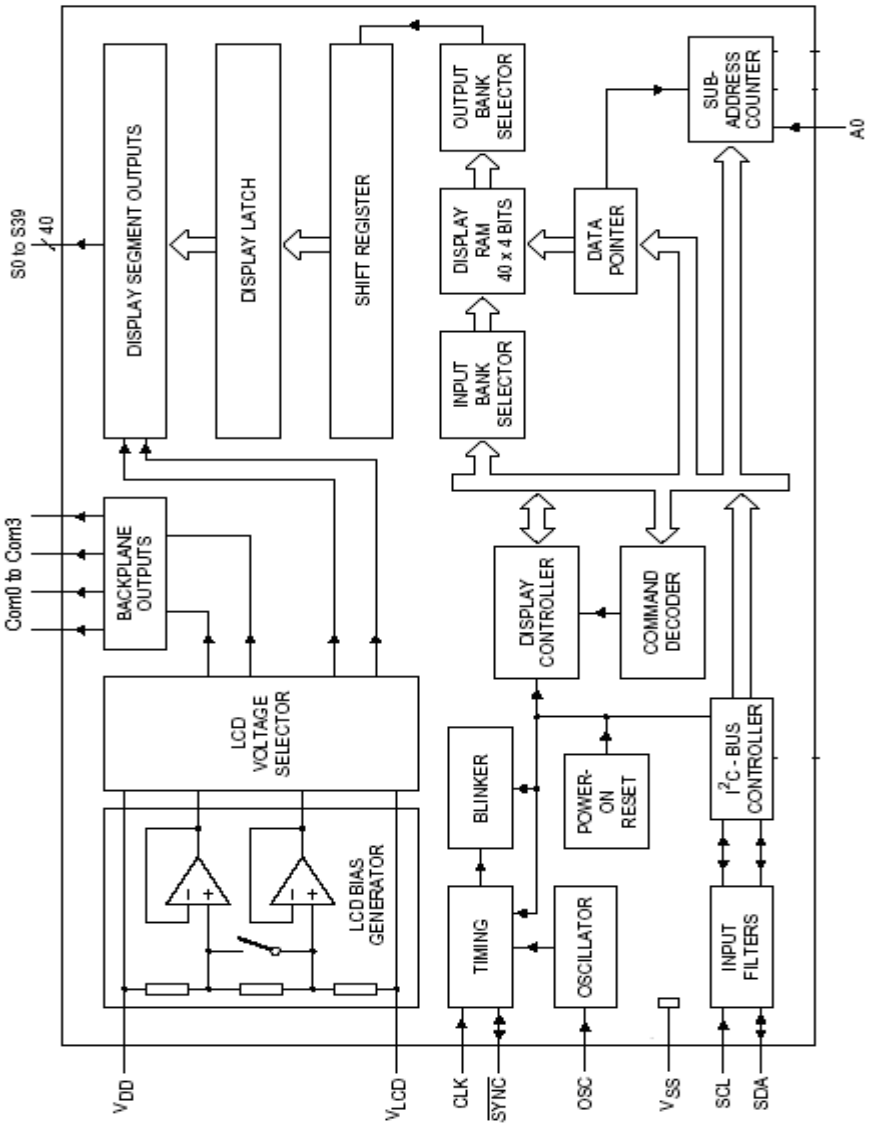
CLK	52	-695.93	-194.17
VDD	53	-425.93	-194.17
VDD	54	-335.93	-194.17
VDD	55	-245.93	-194.17
VDD	56	-155.93	-194.17
VDD	57	-65.93	-194.17
OSC	58	114.07	-194.17
A0	59	204.07	-194.17
VSS	60	384.07	-194.17
VSS	61	474.07	-194.17
VSS	62	564.07	-194.17
VSS	63	654.07	-194.17
VSS	64	744.07	-194.17
VLCD	65	924.07	-194.17
VLCD	66	1014.07	-194.17
VLCD	67	1104.07	-194.17
VLCD	68	1194.07	-194.17
VLCD	69	1284.07	-194.17
CLK	70	1554.07	-194.17
SYNC	71	1644.07	-194.17
SCL	72	1824.07	-194.17
SDA	73	1914.07	-194.17

Alignment Marks

ITEM	SIZE
ALIGN A	
ALIGN B	

Note Alignment marksare on metal2, under passi ation.

3. BLOCK DIAGRAM



4. Function Description

1. function circuit

The BL55087 has all function circuits that can directly drive any static or multiplexed LCD containing up to four commons and up to 40 segments. The function circuits include:Power-on reset, LCD bias generator, LCD voltage selector, Oscillator, display RAM, Timing, Display latch, Shift register, Common/segment outputs, input/output bank selector, Blinker, Data pointer, Subaddress counter,etc.

2. display function description

The display RAM is a static 40x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the common outputs. (see Fig.2).

Display RAM address and SEGMENT（S0~S39）output													
COM (Com0~ Com3)		0	1	2	3					36	37	38	39
	0												
	1												
	2												
	3												

Fig2

When display data is transmitted to the BL55087, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.3; the RAM filling organization depicted applies equally to other LCD types.

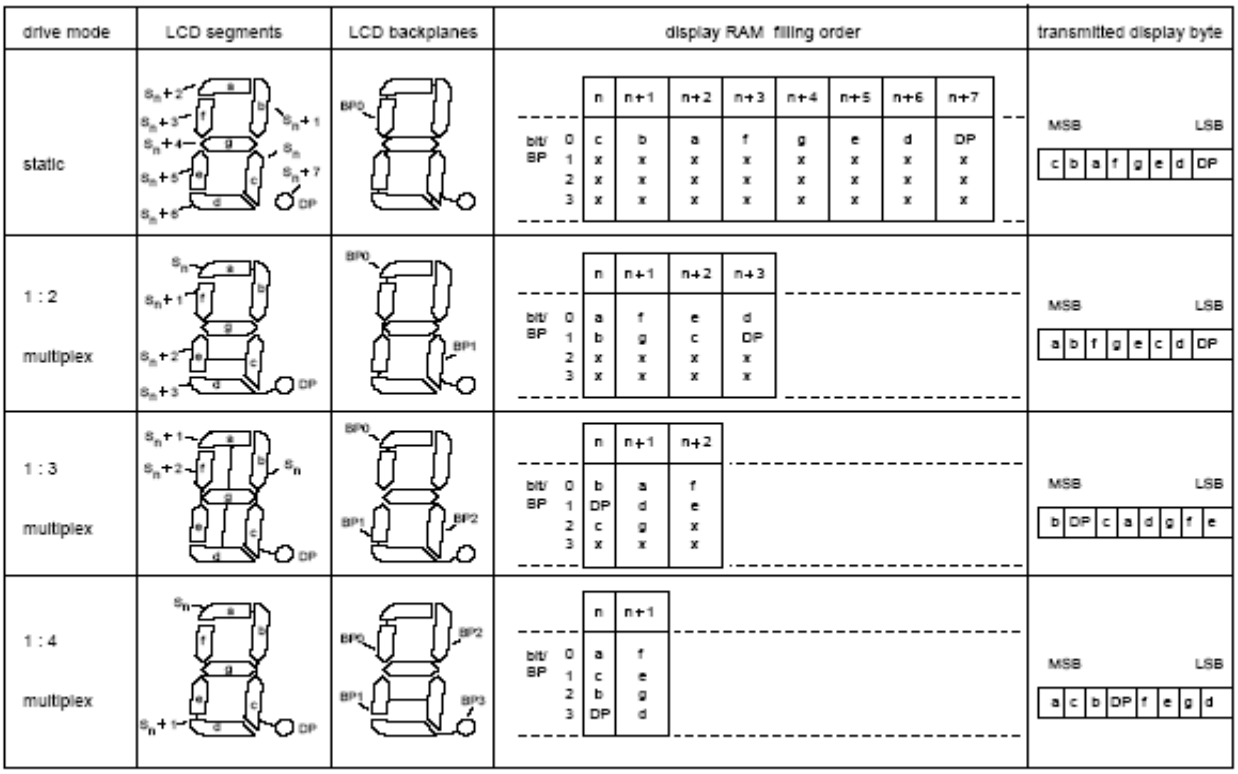


Fig 3

3. I²C-bus protocol

Two I²C-bus slave addresses (0111000) are reserved for the BL55087. The least significant bit of the slave address that a BL55087 will respond to is defined by the level tied at its input SA0. Therefore, two types of BL55087 can be distinguished on the same I²C-bus which allows:

1. Up to 2 BL55087 on the same I2C-bus for very large LCD applications.
2. The use of two types of LCD multiplex on the same I2C-bus.

The I2C-bus protocol is shown in Fig.4. The sequence is initiated with a START condition (S) from the I2C-bus master which is followed by one of the two BL55087 slave addresses available. Two BL55087s with the corresponding SA0 level acknowledge in parallel with the slave address but two BL55087s with the alternative SA0 level ignore the whole I2C-bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed BL55087s. The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed BL55087s on the bus. After the last command byte, a series of display data bytes(n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended BL55087 device. The acknowledgement after each byte is made only by the A0 addressed BL55087. After the last display byte, the I2C-bus master issues a STOP condition (P).

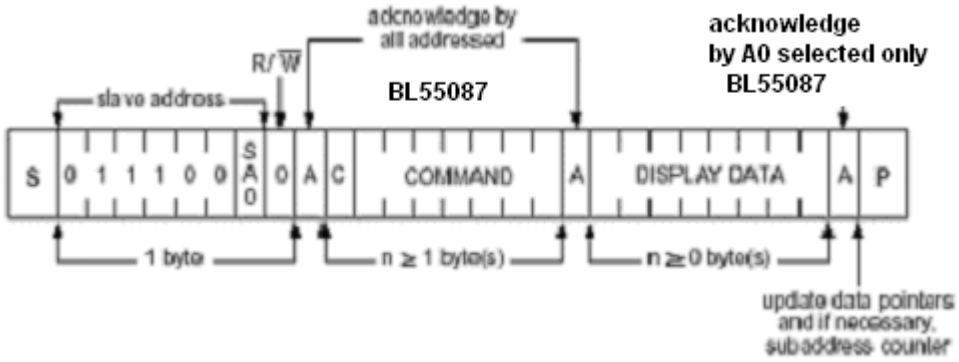
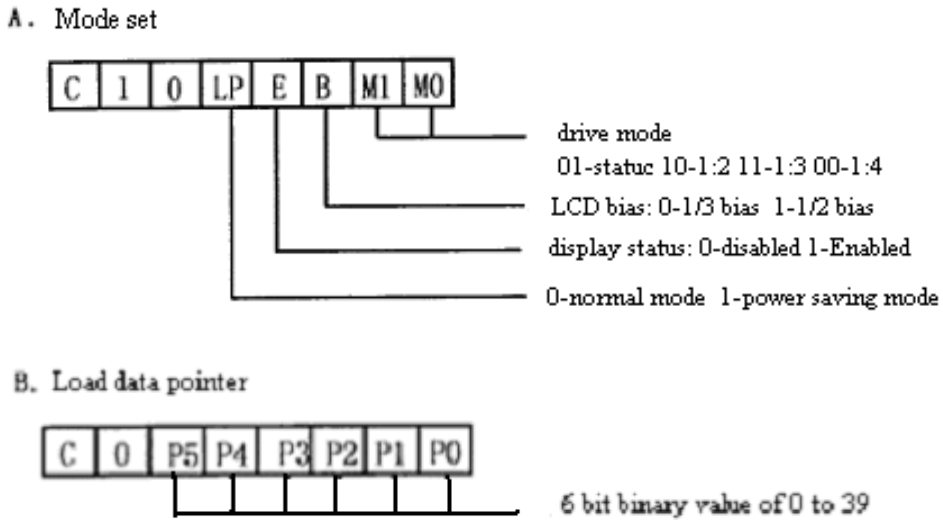


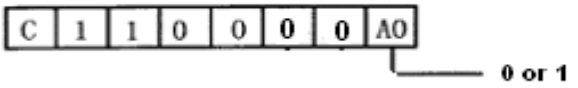
Fig 4

4. command decoder

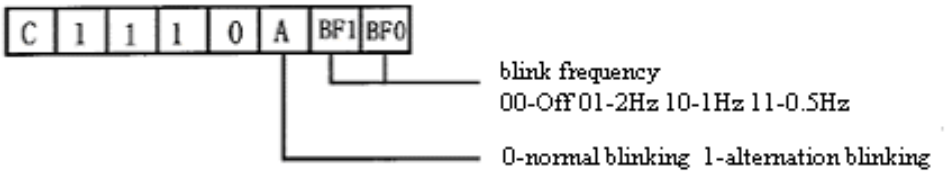
The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most significant bit position. The five commands available to the BL55077 are defined in Fig 5.



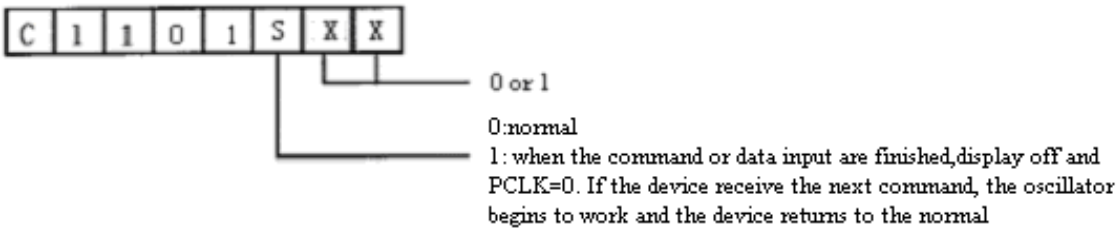
C: Device select



D. Blink control



E. Sleep control



F. BANK

The BANK SELECT command has no effect in 1:3 and 1:4 multiplex drive modes.

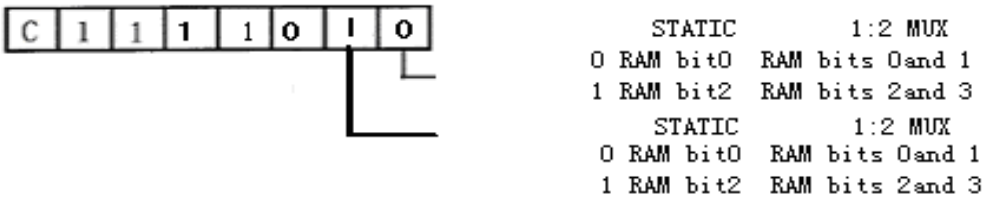


Fig 5

Note 1 In power-saving mode，the frequency of SCL must be less than 20kHz

2 At the bias of 1/3，Vdd – Vlcd must be more than 2.9V

Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Supply voltage	Vdd	-0.5 +6.0	V
LCD operating voltage	Vlcd	0 Vdd	V
Input voltage	Vi	Vss-0.5 Vdd+0.5	V
Output voltage	Vo	Vlcd-0.5 Vdd+0.5	V
Vdd,Vss,Vlcd current	Idd,Iss,Ilcd	-50 +50	mA
Maximum power consumption	Ptot	400	mW
Operating temperature	Topr	-40 +75	°C
Storage temperature	Tstg	-65 +150	°C

Tab 6

DC Characteristic

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Vdd	IC Operating voltage		2.5	-	5.5	V
Vlcd	LCD operating voltage		0	-	Vdd-2	V
Idd1	Supply current	Vdd 5V, VLCD 0V, Normal mode, internal oscillator	-	25	50	uA
Idd2	Supply current	Vdd 5V, VLCD 0V, power sa ing mode, internal oscillator	-	14	30	uA
Idd3	Supply current	Vdd 3.3V, VLCD 0V, Normal mode, internal oscillator	-	16	30	uA
Idd4	Supply current	Vdd 3.3V, VLCD 0V, power sa ing mode, internal oscillator	-	9	15	uA
I_{SL}	Sleep current	Vdd=5V,VLCD=0V	-	1.5	2	uA
ViL	Low voltage input	SDA,SCL	Vss	-	0.3Vdd	V
ViH	High voltage input	SDA,SCL	0.7Vdd	-	6.0	V
Rph	Pull high resister	SYNC	30	60	100	k

Tab 7

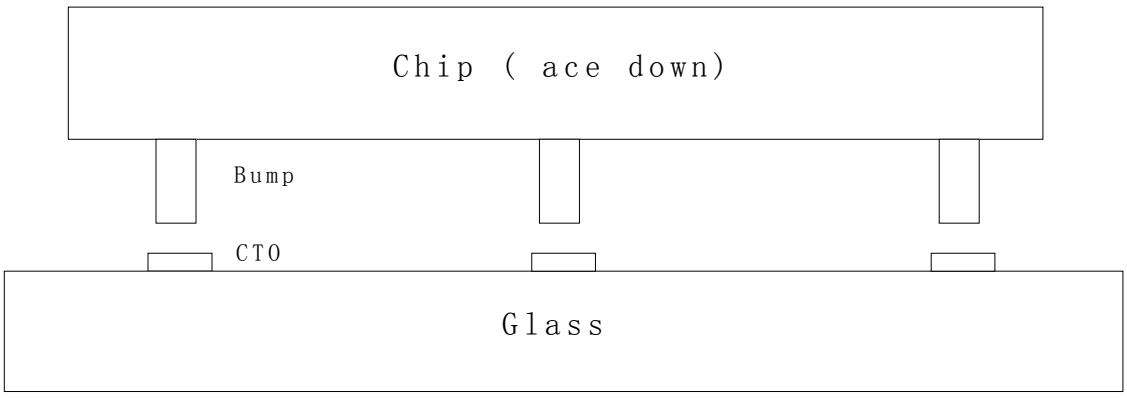
AC Characteristic

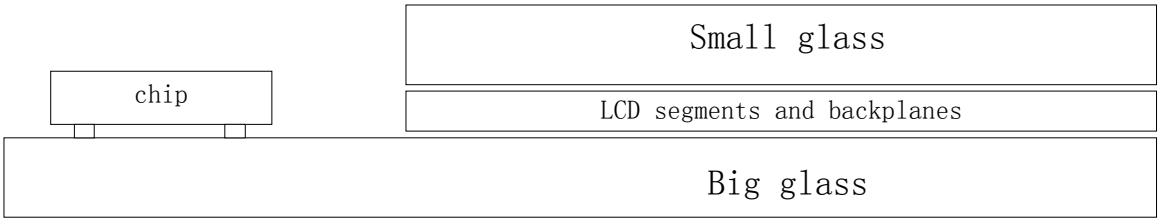
Ta=25°C

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Fclk	Oscillator frequency	Vdd=5V,normal mode	125	180	300	KHz
Fclklp	Oscillator frequency	Vdd=3.3V, power saving mode	21	31	48	KHz
Tclkh/L	CLK time		1	-	3	us
Tsh	Set-up delay time		5	-	-	us
Tlow	SCL LOW time		5	-	-	us
Thigh	SCL HIGH time		4	-	-	us
Thd	Pulse delay time		250	-	-	ns

Tab 8

5. COG Package





6. timing wa e orms

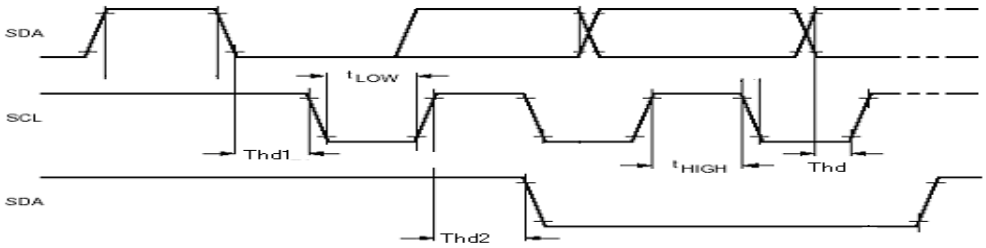
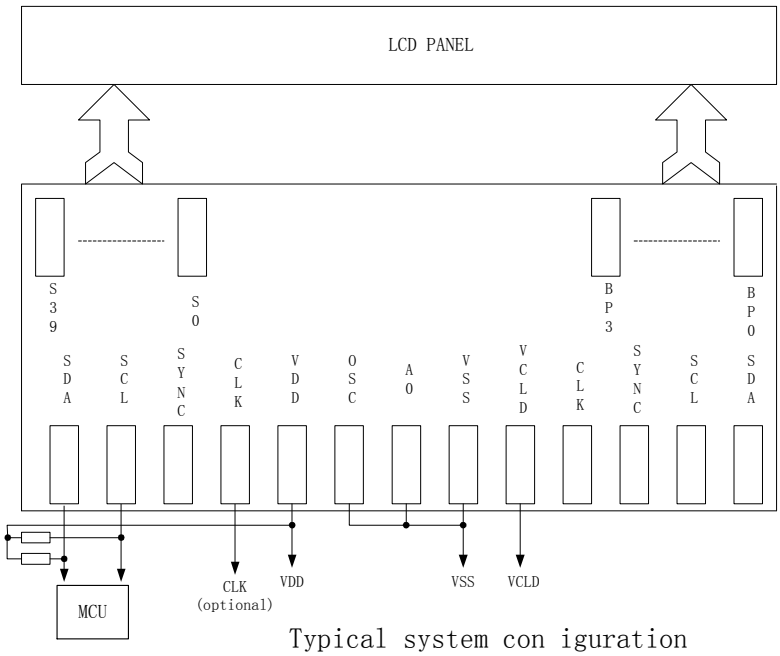


Fig 6

7. Typical Application Circuit

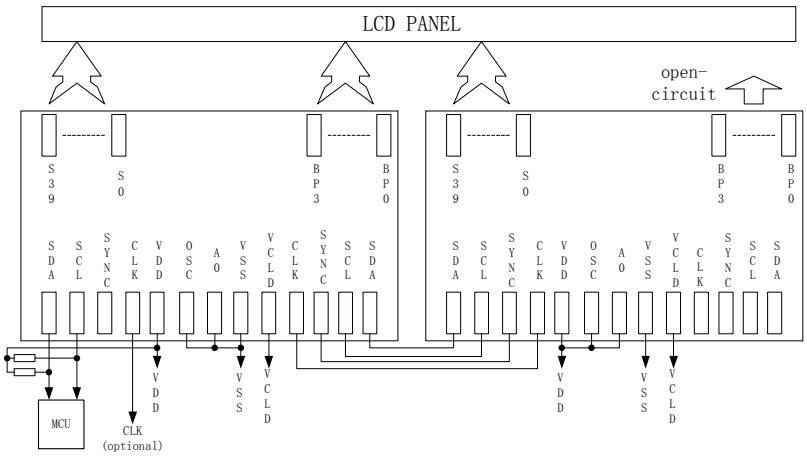
Note:1/ when I²C are idle mode,SDA and SCL must be connect to high level(by pull up resistor),otherwise the device maybe can not go into power saving mode.

1/ single application



Typical system con iguration

2/ cascade application



Cascaded con iguration

N