

# NCV7344

## High Speed Low Power CAN, CAN FD Transceiver

### Description

The NCV7344 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7344 is an addition to the CAN high-speed transceiver family complementing NCV734x CAN stand-alone transceivers and previous generations such as AMIS42665, AMIS3066x, etc.

The NCV7344 guarantees additional timing parameters to ensure robust communication at data rates beyond 1 Mbps to cope with CAN flexible data rate requirements (CAN FD). These features make the NCV7344 an excellent choice for all types of HS-CAN networks, in nodes that require a low-power mode with wake-up capability via the CAN bus.

### Features

- Compatible with ISO 11898-2:2016
- Specification for Loop Delay Symmetry up to 5 Mbps
- V<sub>IO</sub> pin on NCV7344-3 Version Allowing Direct Interfacing with 3 V to 5 V Microcontrollers
- Very Low Current Standby Mode with Wake-up via the Bus
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity
- Very Low EME without Common-mode (CM) Choke
- No Disturbance of the Bus Lines with an Un-powered Node
- Transmit Data (TxD) Dominant Timeout Function
- Under All Supply Conditions the Chip Behaves Predictably
- Very High ESD Robustness of Bus Pins, >8 kV System ESD Pulses
- Thermal Protection
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- Bus Pins Protected Against Transients in an Automotive Environment
- These are Pb-free Devices

### Quality

- Wettable Flank Package for Enhanced Optical Inspection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

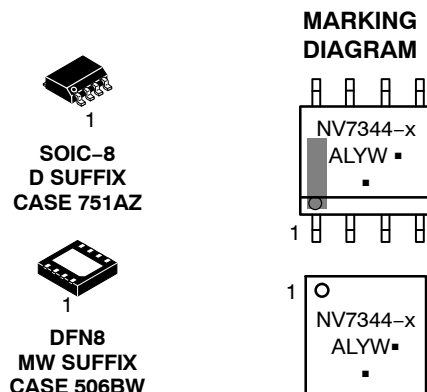
### Typical Applications

- Automotive
- Industrial Networks



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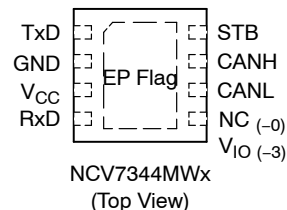
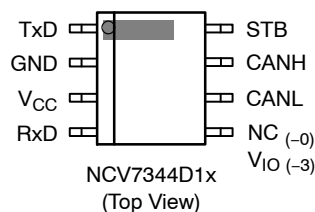
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NV7344-x = Specific Device Code  
x = 0 or 3  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

# NCV7344

## BLOCK DIAGRAM

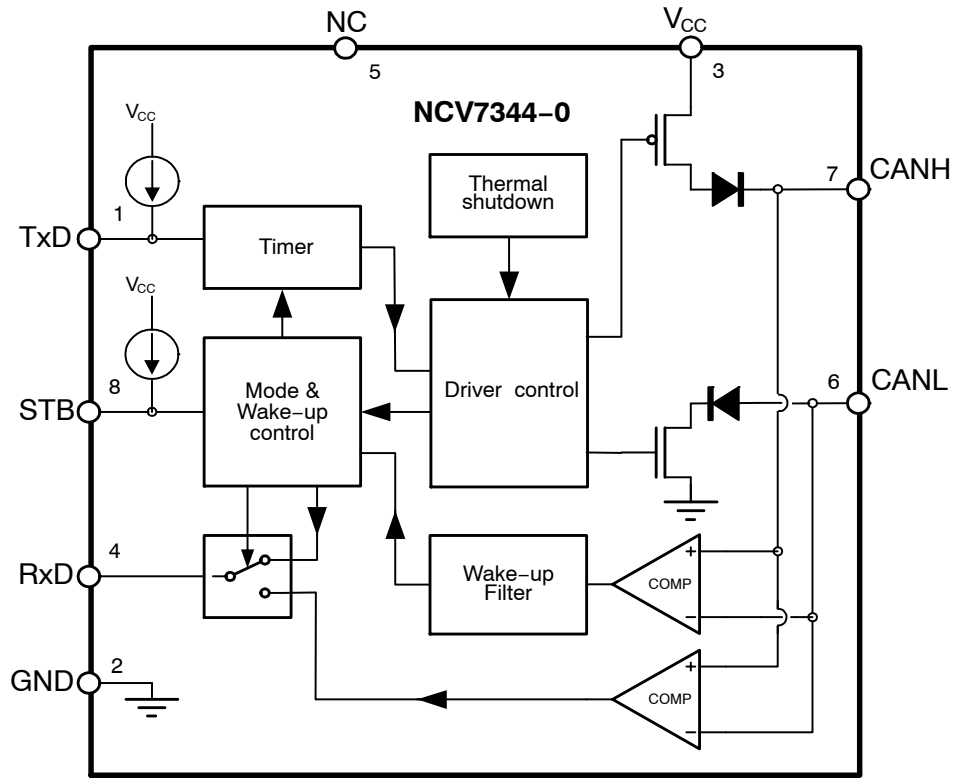


Figure 1. NCV7344-0 Block Diagram

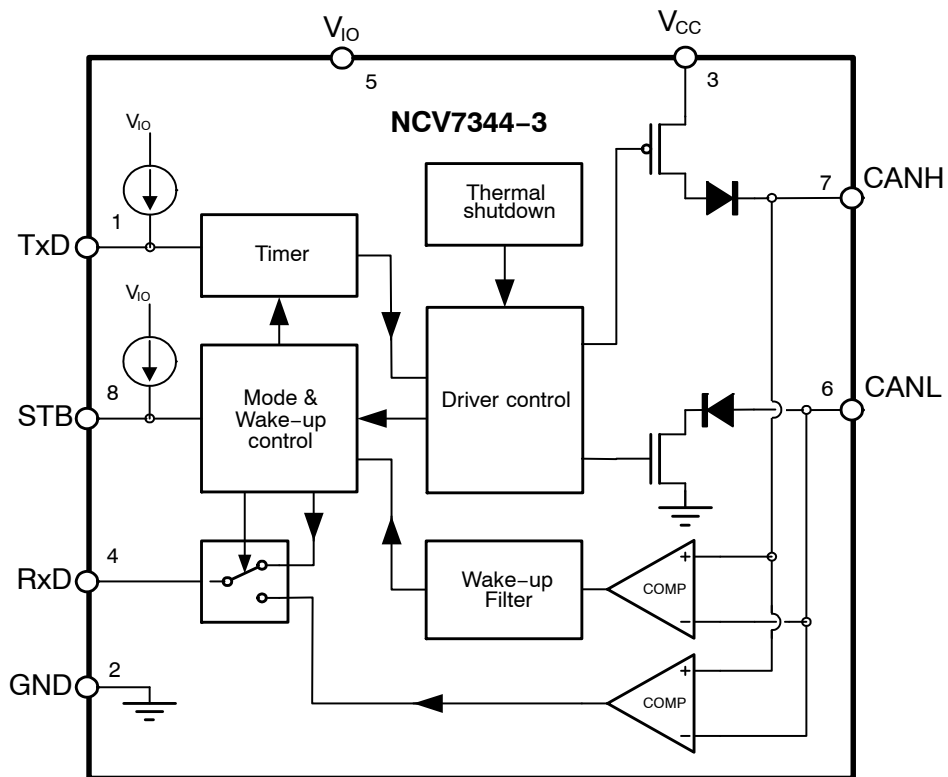


Figure 2. NCV7344-3 Block Diagram

# NCV7344

## TYPICAL APPLICATION

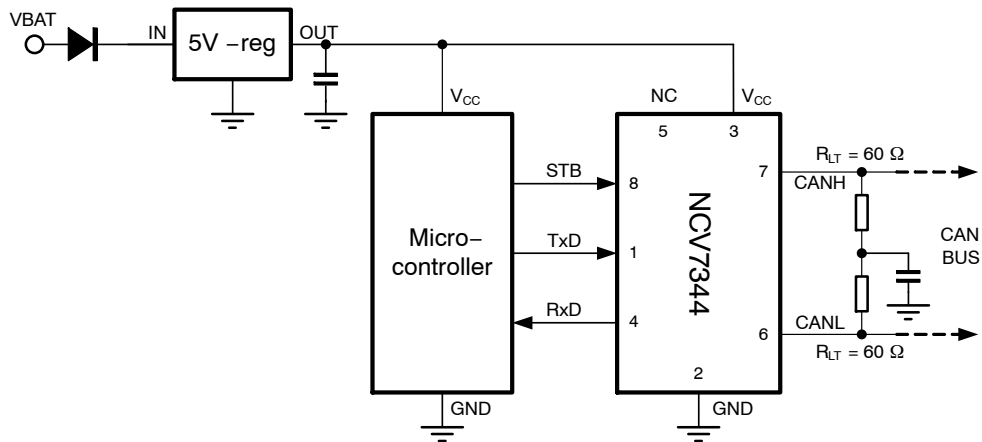


Figure 3. Application Diagram NCV7344-0

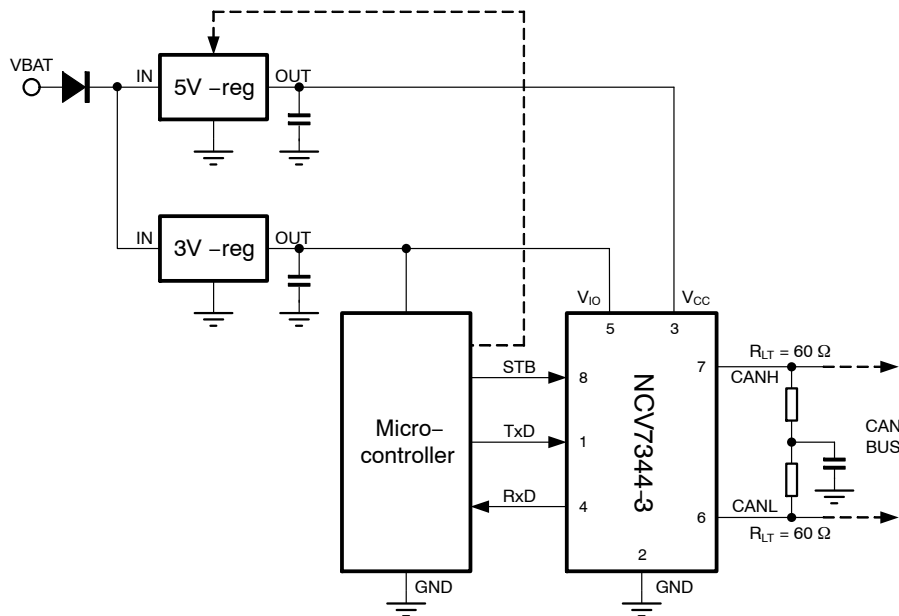


Figure 4. Application Diagram NCV7344-3

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	TxD	Transmit data input; low input → dominant driver; internal pull-up current
2	GND	Ground
3	V <sub>CC</sub>	Supply voltage
4	RxD	Receive data output; dominant transmitter → low output
5	NC	Not connected. On NCV7344-0 only
5	V <sub>IO</sub>	Digital Input / Output pins and other functions supply voltage. On NCV7344-3 only
6	CANL	Low-level CAN bus line (low in dominant mode)
7	CANH	High-level CAN bus line (high in dominant mode)
8	STB	Standby mode control input; internal pull-up current

FUNCTIONAL DESCRIPTION

**Operating Modes**

NCV7344 provides two modes of operation as illustrated in Table 2. These modes are selectable through pin STB.

**Table 2. OPERATING MODES**

Pin STB	Mode	Pin RxD	
Low	Normal	Low when bus dominant	High when bus recessive
High	Standby	Follows the bus when wake-up detected	High when no wake-up request detected

**Normal Mode**

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give low EME.

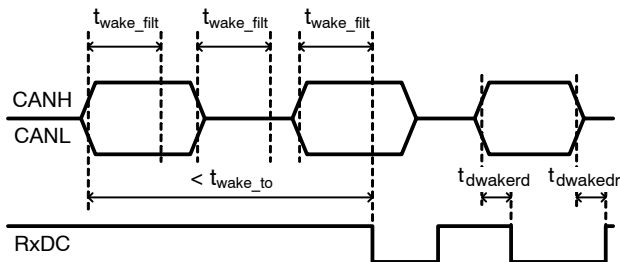
**Standby Mode**

In standby mode both the transmitter and receiver are disabled and a very low-power differential receiver monitors the bus lines for CAN bus activity. The bus lines are biased to ground and supply current is reduced to a minimum, typically 10  $\mu$ A. When a wake-up request is detected by the low-power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of  $t_{wake\_filt}$ , the RxD pin is driven low by the transceiver (following the bus) to inform the controller of the wake-up request.

**Wake-up**

When a valid wake-up pattern (phase in order dominant – recessive – dominant) is detected during the standby mode the RxD pin follows the bus. Minimum length of each phase is  $t_{wake\_filt}$  – see Figure 5.

Pattern must be received within  $t_{wake\_to}$  to be recognized as valid wake-up otherwise internal logic is reset.



**Figure 5. NCV7344 Wake-up Behavior**

**Overtemperature Detection**

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 170°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off-state resets when the temperature decreases below the shutdown threshold and pin TxD goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

**TxD Dominant Timeout Function**

A TxD dominant timeout timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low-level on pin TxD exceeds the internal timer value  $t_{dom(TxD)}$ , the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

This TxD dominant timeout time  $t_{dom(TxD)}$  defines the minimum possible bit rate to 12 kbps.

**Fail Safe Features**

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

Undervoltage on VCC pin prevents the chip sending data on the bus when there is not enough VCC supply voltage. After supply is recovered TxD pin must be first released to high to allow sending dominant bits again. Recovery time from undervoltage detection is equal to  $t_{d(stb-nm)}$  time.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 7). Pins TxD and STB are pulled high internally should the input become disconnected. Pins TxD, STB and RxD will be floating, preventing reverse supply should the VCC supply be removed.

**V<sub>IO</sub> Supply Pin**

The V<sub>IO</sub> pin (available only on NCV7344-3 version) should be connected to microcontroller supply pin. By using V<sub>IO</sub> supply pin shared with microcontroller the I/O levels between microcontroller and transceiver are properly adjusted. See Figure 4. Pin V<sub>IO</sub> also provides the internal supply voltage for low-power differential receiver of the transceiver. This allows detection of wake-up request even when there is no supply voltage on pin V<sub>CC</sub>.

**ELECTRICAL CHARACTERISTICS**

**Definitions**

All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

**ABSOLUTE MAXIMUM RATINGS**

**Table 3. ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>SUP</sub>	Supply voltage V <sub>CC</sub> , V <sub>IO</sub>		-0.3	+6	V
V <sub>CANH</sub>	DC voltage at pin CANH	0 < V <sub>CC</sub> < 5.25 V; no time limit	-42	+42	V
V <sub>CANL</sub>	DC voltage at pin CANL	0 < V <sub>CC</sub> < 5.25 V; no time limit	-42	+42	V
V <sub>CANH-CANL</sub>	DC voltage between CANH and CANL		-42	+42	V
V <sub>I/O</sub>	DC voltage at pin TxD, RxD, STB		-0.3	+6	V
V <sub>esdHBM</sub>	Electrostatic discharge voltage at all pins, Component HBM	(Note 1)	-8	+8	kV
V <sub>esdCDM</sub>	Electrostatic discharge voltage at all pins, Component CDM	(Note 2)	-750	+750	V
V <sub>esdIEC</sub>	Electrostatic discharge voltage at pins CANH and CANL, System HBM (Note 4)	(Note 3)	-8	+8	kV
V <sub>schaff</sub>	Voltage transients, pins CANH, CANL. According to ISO7637-3, Class C (Note 4)	test pulses 1	-100		V
		test pulses 2a		+75	V
		test pulses 3a	-150		V
		test pulses 3b		+100	V
Latch-up	Static latch-up at all pins	(Note 5)		150	mA
T <sub>stg</sub>	Storage temperature		-55	+150	°C
T <sub>J</sub>	Maximum junction temperature		-40	+170	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA-JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Standardized charged device model ESD pulses when tested according to AEC-Q100-011
3. System human body model electrostatic discharge (ESD) pulses in accordance to IEC 61000-4-2. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor referenced to GND.
4. Results were verified by external test house.
5. Static latch-up immunity: Static latch-up protection level when tested according to EIA/JESD78.

**Table 4. THERMAL CHARACTERISTICS**

Parameter	Symbol	Value	Unit
Thermal characteristics, SOIC-8 (Note 6)			
Thermal Resistance Junction-to-Air, Free air, 1S0P PCB (Note 7)	R <sub>θJA</sub>	131	°C/W
Thermal Resistance Junction-to-Air, Free air, 2S2P PCB (Note 8)	R <sub>θJA</sub>	81	°C/W
Thermal characteristics, DFN8 (Note 6)			
Thermal Resistance Junction-to-Air, Free air, 1S0P PCB (Note 7)	R <sub>θJA</sub>	125	°C/W
Thermal Resistance Junction-to-Air, Free air, 2S2P PCB (Note 8)	R <sub>θJA</sub>	58	°C/W

6. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
7. Values based on test board according to EIA/JEDEC Standard JESD51-3, signal layer with 10% trace coverage.
8. Values based on test board according to EIA/JEDEC Standard JESD51-7, signal layers with 10% trace coverage.

ELECTRICAL CHARACTERISTICS

**Table 5. ELECTRICAL CHARACTERISTICS**

$V_{CC} = 4.75\text{ V to } 5.25\text{ V}$ ;  $V_{IO} = 2.8\text{ to } 5.25\text{ V}$ ;  $T_J = -40\text{ to } +150^\circ\text{C}$ ;  $R_{LT} = 60\ \Omega$ ,  $C_{LT} = 100\text{ pF}$ ,  $C_1$  not used unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>SUPPLY (Pin <math>V_{CC}</math>)</b>						
$V_{CC}$	Power supply voltage	(Note 9)	4.75	5	5.25	V
$I_{CC}$	Supply current	Dominant; $V_{TxD} = \text{Low}$	20	45	70	mA
		Recessive; $V_{TxD} = \text{High}$	2	5	10	mA
$I_{CCS}$	Supply current in standby mode	$T_J \leq 100^\circ\text{C}$ , (Note 10)	–	10	15	$\mu\text{A}$
$V_{UVD(VCC)(stby)}$	Standby undervoltage detection $V_{CC}$ pin		3.5	4	4.3	V
$V_{UVD(VCC)(swoff)}$	Switch-off undervoltage detection $V_{CC}$ pin		2.0	2.3	2.6	V
<b><math>V_{IO}</math> SUPPLY VOLTAGE (Pin <math>V_{IO}</math>) Only for NCV7344–3 version</b>						
$V_{IO}$	Supply voltage on pin $V_{IO}$		2.8	–	5.5	V
$I_{IOS}$	Supply current on pin $V_{IO}$ in standby mode	$T_J \leq 100^\circ\text{C}$ , (Note 10)	–	–	11	$\mu\text{A}$
$I_{CCS}$	Supply current on pin $V_{CC}$ in standby mode	$T_J \leq 100^\circ\text{C}$ , (Note 10)	–	0	4.0	$\mu\text{A}$
$I_{IONM}$	Supply current on pin $V_{IO}$ during normal mode	Dominant; $V_{TxD} = \text{Low}$	0.45	0.65	0.9	mA
		Recessive; $V_{TxD} = \text{Low}$	0.32	0.43	0.58	
$V_{UVDVIO}$	Undervoltage detection voltage on $V_{IO}$ pin		2.0	2.3	2.6	V
<b>TRANSMITTER DATA INPUT (Pin <math>TxD</math>)</b>						
$V_{IH}$	High-level input voltage	Output recessive	2.0	–	–	V
$V_{IL}$	Low-level input voltage	Output dominant	–	–	0.8	V
$I_{IH}$	High-level input current	$V_{TxD} = V_{CC}/V_{IO}$	–5	0	+5	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{TxD} = 0\text{ V}$	–300	–150	–75	$\mu\text{A}$
$C_i$	Input capacitance	(Note 10)	–	5	10	pF
<b>TRANSMITTER MODE SELECT (Pin <math>STB</math>)</b>						
$V_{IH}$	High-level input voltage	Standby mode	2.0	–	–	V
$V_{IL}$	Low-level input voltage	Normal mode	–	–	0.8	V
$I_{IH}$	High-level input current	$V_{STB} = V_{CC}/V_{IO}$	–1	0	+1	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{STB} = 0\text{ V}$	–15	–	–1	$\mu\text{A}$
$C_i$	Input capacitance	(Note 10)	–	5	10	pF
<b>RECEIVER DATA OUTPUT (Pin <math>RxD</math>)</b>						
$I_{OH}$	High-level output current	Normal mode $V_{RxD} = V_{CC}/V_{IO} - 0.4\text{ V}$	–8	–3	–1	mA
$I_{OL}$	Low-level output current	$V_{RxD} = 0.4\text{ V}$	1	6	12	mA
<b>BUS LINES (Pins <math>CANH</math> and <math>CANL</math>)</b>						
$I_{o(rec)}$	Recessive output current at pins $CANH$ and $CANL$	$-27\text{ V} < V_{CANH}$ , $V_{CANL} < +32\text{ V}$ ; Normal mode	–5	–	+5	mA
$I_{LI}$	Input leakage current	$0\ \Omega < R(V_{CC}\text{ to GND}) < 1\ \text{M}\Omega$ $V_{CANL} = V_{CANH} = 5\text{ V}$	–5	0	+5	$\mu\text{A}$
$V_{o(rec)}(CANH)$	Recessive output voltage at pin $CANH$	Normal mode, $V_{TxD} = \text{High}$	2.0	2.5	3.0	V
$V_{o(rec)}(CANL)$	Recessive output voltage at pin $CANL$	Normal mode, $V_{TxD} = \text{High}$	2.0	2.5	3.0	V
$V_{o(off)}(CANH)$	Recessive output voltage at pin $CANH$	Standby mode	–0.1	0	0.1	V
$V_{o(off)}(CANL)$	Recessive output voltage at pin $CANL$	Standby mode	–0.1	0	0.1	V
$V_{o(off)}(diff)$	Differential bus output voltage ( $V_{CANH} - V_{CANL}$ )	Standby mode	–0.2	0	0.2	V
$V_{o(dom)}(CANH)$	Dominant output voltage at pin $CANH$	$V_{TxD} = 0\text{ V}$ ; $t < t_{dom}(TxD)$ ; $50\ \Omega < R_{LT} < 65\ \Omega$	2.75	3.5	4.5	V
$V_{o(dom)}(CANL)$	Dominant output voltage at pin $CANL$	$V_{TxD} = 0\text{ V}$ ; $t < t_{dom}(TxD)$ ; $50\ \Omega < R_{LT} < 65\ \Omega$	0.5	1.5	2.25	V
$V_{o(dom)}(diff)$	Differential bus output voltage ( $V_{CANH} - V_{CANL}$ )	$V_{TxD} = 0\text{ V}$ ; dominant; $45\ \Omega < R_{LT} < 65\ \Omega$	1.5	2.25	3.0	V

9. In the range of 4.5 V to 4.75V and from 5.25 V to 5.5 V the chip is fully functional; some parameters may be outside of the specification.

10. Values based on design and characterization, not tested in production

# NCV7344

**Table 5. ELECTRICAL CHARACTERISTICS**

$V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.8\text{ to }5.25\text{ V}$ ;  $T_J = -40\text{ to }+150^\circ\text{C}$ ;  $R_{LT} = 60\ \Omega$ ,  $C_{LT} = 100\text{ pF}$ ,  $C_1$  not used unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>BUS LINES (Pins CANH and CANL)</b>						
$V_{o(dom)}(diff)_{arb}$	Differential bus output voltage during arbitration ( $V_{CANH} + V_{CANL}$ )	$R_{LT} = 2.24\text{ k}\Omega$ (Note 10)	1.5	–	5.0	V
$V_{o(rec)}(diff)$	Differential bus output voltage ( $V_{CANH} - V_{CANL}$ )	$V_{TxD} = \text{High}$ ; recessive; no load	–50	0	+50	mV
$V_{o(dom)}(sym)$	Dominant output voltage driver symmetry ( $V_{CANH} + V_{CANL}$ )	$R_{LT} = 60\ \Omega$ ; $C_1 = 4.7\text{ nF}$ ; $TxD = \text{square wave up to }1\text{ MHz}$	0.9	1.0	1.1	$V_{CC}$
$I_{o(sc)}(CANH)$	Short circuit output current at pin CANH	$V_{CANH} = -3\text{ V}$ ; $V_{TxD} = \text{Low}$ $-3\text{ V} < V_{CANH} < +18\text{ V}$	–100 –115	–70	–40 115	mA
$I_{o(sc)}(CANL)$	Short circuit output current at pin CANL	$V_{CANL} = 36\text{ V}$ ; $V_{TxD} = \text{Low}$ $-3\text{ V} < V_{CANL} < +18\text{ V}$	40 –115	70	100 115	mA
$V_{i(diff)}(th)_{NORM}$	Differential receiver threshold voltage in normal mode	$-12\text{ V} < V_{CANL} < +12\text{ V}$ ; $-12\text{ V} < V_{CANH} < +12\text{ V}$	0.5	–	0.9	V
$V_{i(diff)}(th)_{STDBY}$	Differential receiver threshold voltage in standby mode	$-12\text{ V} < V_{CANL} < +12\text{ V}$ ; $-12\text{ V} < V_{CANH} < +12\text{ V}$	0.4	–	1.05	V
$R_{i(cm)}(CANH)$	Common-mode input resistance at pin CANH	$-2\text{ V} < V_{CANH} < +7\text{ V}$ ; $-2\text{ V} < V_{CANL} < +7\text{ V}$	15	26	37	k $\Omega$
$R_{i(cm)}(CANL)$	Common-mode input resistance at pin CANL	$-2\text{ V} < V_{CANH} < +7\text{ V}$ ; $-2\text{ V} < V_{CANL} < +7\text{ V}$	15	26	37	k $\Omega$
$R_{i(cm)}(m)$	Matching between pin CANH and pin CANL common mode input resistance	$V_{CANH} = V_{CANL} = +5\text{ V}$	–1	0	+1	%
$R_{i(diff)}$	Differential input resistance		25	50	75	k $\Omega$
$C_{i(CANH)}$	Input capacitance at pin CANH	$V_{TxD} = \text{High}$ ; (Note 10)	–	7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	$V_{TxD} = \text{High}$ ; (Note 10)	–	7.5	20	pF
$C_{i(diff)}$	Differential input capacitance	$V_{TxD} = \text{High}$ ; (Note 10)	–	3.75	10	pF

### TIMING CHARACTERISTICS (see Figures 6 and 8)

$t_{d(TxD-BUSon)}$	Delay TxD to bus active		–	75	–	ns
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive		–	85	–	ns
$t_{d(BUSon-RxD)}$	Delay bus active to RxD		–	24	–	ns
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxD		–	32	–	ns
$t_{pd\_dr}$	Propagation delay TxD to RxD dominant to recessive transition		50	100	210	ns
$t_{pd\_rd}$	Propagation delay TxD to RxD recessive to dominant transition		50	120	210	ns
$t_{d(stb-nm)}$	Delay standby mode to normal mode		5	11	20	$\mu\text{s}$
$t_{wake\_filt}$	Filter time for wake-up via bus		0.5	–	5	$\mu\text{s}$
$t_{dwakerd}$	Delay to flag wake event (recessive to dominant transitions)	Valid bus wake-up event	0.5	2.6	6	$\mu\text{s}$
$t_{dwakedr}$	Delay to flag wake event (dominant to recessive transitions)	Valid bus wake-up event	0.5	2.6	6	$\mu\text{s}$
$t_{wake\_to}$	Bus time for wake-up timeout	Standby mode	1	–	10	ms
$t_{dom(TxD)}$	TxD dominant time for timeout	$V_{TxD} = \text{Low}$ ; Normal mode	1	–	10	ms
$t_{Bit(RxD)}$	Bit time on RxD pin	$t_{Bit(TxD)} = 500\text{ ns}$	400	–	550	ns
		$t_{Bit(TxD)} = 200\text{ ns}$	120	–	220	ns
$t_{Bit}(V_i(diff))$	Bit time on bus (CANH – CANL pin)	$t_{Bit(TxD)} = 500\text{ ns}$	435	–	530	ns
		$t_{Bit(TxD)} = 200\text{ ns}$	155	–	210	ns
$\Delta t_{Rec}$	Receiver timing symmetry $\Delta t_{Rec} = t_{Bit(RxD)} - t_{Bit}(V_i(diff))$	$t_{Bit(TxD)} = 500\text{ ns}$	–65	–	+40	ns
		$t_{Bit(TxD)} = 200\text{ ns}$	–45	–	+15	ns

### THERMAL SHUTDOWN

$T_{J(sd)}$	Shutdown junction temperature	Junction temperature rising	160	180	200	$^\circ\text{C}$
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9. In the range of 4.5 V to 4.75V and from 5.25 V to 5.5 V the chip is fully functional; some parameters may be outside of the specification.

10. Values based on design and characterization, not tested in production

# NCV7344

## MEASUREMENT SETUPS AND DEFINITIONS

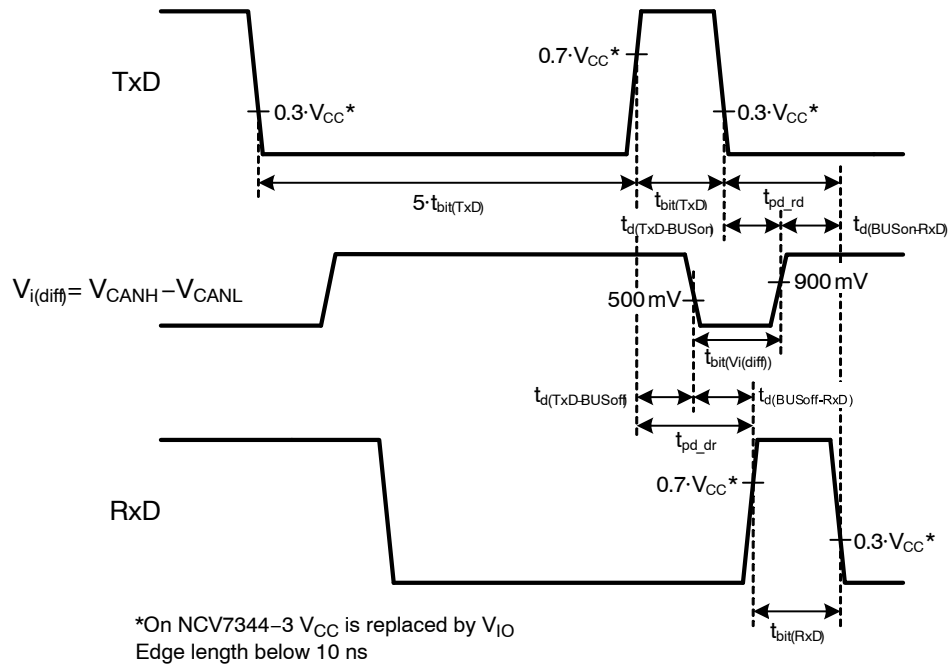


Figure 6. Transceiver Timing Diagram

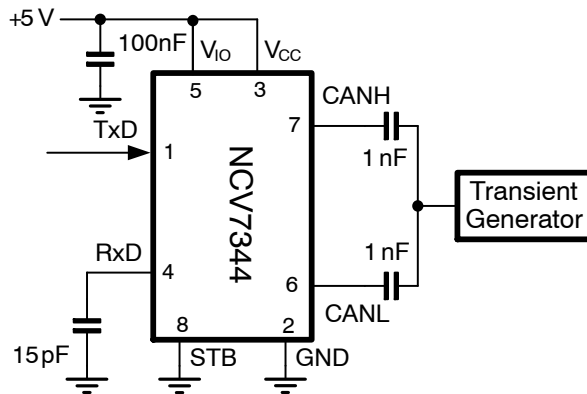


Figure 7. Test Circuit for Automotive Transients

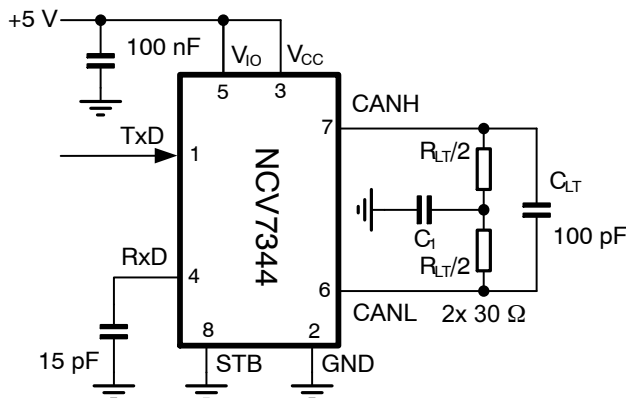


Figure 8. Test Circuit for Timing Characteristics



Table 6. ISO 11898–2:2016 Parameter Cross–Reference Table

ISO 11898–2:2016 Specification		NCV7344 Datasheet	
Parameter	Notation	Symbol	
<b>Dominant output characteristics</b>			
Single ended voltage on CAN_H	$V_{CAN\_H}$	$V_{o(dom)}(CANH)$	
Single ended voltage on CAN_L	$V_{CAN\_L}$	$V_{o(dom)}(CANL)$	
Differential voltage on normal bus load	$V_{Diff}$	$V_{o(dom)}(diff)$	
Differential voltage on effective resistance during arbitration	$V_{Diff}$	$V_{o(dom)}(diff\_arb)$	
Differential voltage on extended bus load range (optional)	$V_{Diff}$	$V_{o(dom)}(diff)$	
<b>Driver symmetry</b>			
Driver symmetry	$V_{SYM}$	$V_{o(dom)}(sym)$	
<b>Driver output current</b>			
Absolute current on CAN_H	$I_{CAN\_H}$	$I_o(SC)(CANH)$	
Absolute current on CAN_L	$I_{CAN\_L}$	$I_o(SC)(CANL)$	
<b>Receiver output characteristics, bus biasing active</b>			
Single ended output voltage on CAN_H	$V_{CAN\_H}$	$V_{o(rec)}(CANH)$	
Single ended output voltage on CAN_L	$V_{CAN\_L}$	$V_{o(rec)}(CANL)$	
Differential output voltage	$V_{Diff}$	$V_{o(rec)}(diff)$	
<b>Receiver output characteristics, bus biasing inactive</b>			
Single ended output voltage on CAN_H	$V_{CAN\_H}$	$V_{o(off)}(CANH)$	
Single ended output voltage on CAN_L	$V_{CAN\_L}$	$V_{o(off)}(CANL)$	
Differential output voltage	$V_{Diff}$	$V_{o(off)}(diff)$	
<b>Optional transmit dominant timeout</b>			
Transmit dominant timeout, long	$t_{dom}$	$T_{dom}(TxD)$	
Transmit dominant timeout, short	$t_{dom}$	NA	
<b>Static receiver input characteristics, bus biasing active</b>			
Recessive state differential input voltage range	$V_{Diff}$	$V_{i(diff)}(th)_{NORM}$	
Dominant state differential input voltage range	$V_{Diff}$	$V_{i(diff)}(th)_{NORM}$	
<b>Static receiver input characteristics, bus biasing inactive</b>			
Recessive state differential input voltage range	$V_{Diff}$	$V_{i(diff)}(th)_{STDBY}$	
Dominant state differential input voltage range	$V_{Diff}$	$V_{i(diff)}(th)_{STDBY}$	
<b>Receiver input resistance</b>			
Differential internal resistance	$R_{Diff}$	$R_{i(diff)}$	
Single ended internal resistance	$R_{CAN\_H}$ $R_{CAN\_L}$	$R_{i(cm)}(CANH)$ $R_{i(cm)}(CANL)$	
<b>Receiver input resistance matching</b>			
Matching a of internal resistance	$m_R$	$R_{i(cm)}(m)$	
<b>Implementation loop delay requirement</b>			
Loop delay	$t_{Loop}$	$t_{pd\_rd}$ $t_{pd\_dr}$	
<b>Optional implementation data signal timing requirements for use with bit rates above 1 Mbit/s and up to 2 Mbit/s</b>			
Transmitted recessive bit width @ 2 Mbit/s	$t_{Bit}(Bus)$	$t_{Bit}(Vi(diff))$	
Received recessive bit width @ 2 Mbit/s	$t_{Bit}(RXD)$	$t_{Bit}(RxD)$	

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**Table 6. ISO 11898–2:2016 Parameter Cross–Reference Table**

Parameter	Notation	Symbol
Receiver timing symmetry @ 2 Mbit/s	$\Delta t_{Rec}$	$\Delta t_{Rec}$
<b>Optional implementation data signal timing requirements for use with bit rates above 2 Mbit/s and up to 5 Mbit/s</b>		
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(Bus)}$	$t_{Bit(Vi(diff))}$
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(RxD)}$	$t_{Bit(RxD)}$
Received recessive bit width @ 5 Mbit/s	$\Delta t_{Rec}$	$\Delta t_{Rec}$
<b>Maximum ratings of <math>V_{CAN\_H}</math>, <math>V_{CAN\_L}</math> and <math>V_{Diff}</math></b>		
Maximum rating $V_{Diff}$	$V_{Diff}$	$V_{CANH-CANL}$
General maximum rating $V_{CAN\_H}$ and $V_{CAN\_L}$	$V_{CAN\_H}$ $V_{CAN\_L}$	$V_{CANH}$ $V_{CANL}$
Optional: Extended maximum rating $V_{CAN\_H}$ and $V_{CAN\_L}$	$V_{CAN\_H}$ $V_{CAN\_L}$	NA
<b>Maximum leakage currents on CAN_H and CAN_L, unpowered</b>		
Leakage current on CAN_H, CAN_L	$I_{CAN\_H}$ $I_{CAN\_L}$	$I_{LI}$
<b>Bus biasing control timings</b>		
CAN activity filter time, long	$t_{Filter}$	$t_{wake\_filt}$
CAN activity filter time, short	$t_{Filter}$	NA
Wake–up timeout, short	$t_{Wake}$	$t_{wake\_to}$
Wake–up timeout, long	$t_{Wake}$	$t_{wake\_to}$
Timeout for bus inactivity (Required for selective wake–up implementation only)	$t_{Silence}$	NA
Bus Bias reaction time (Required for selective wake–up implementation only)	$t_{Bias}$	NA

## DEVICE ORDERING INFORMATION

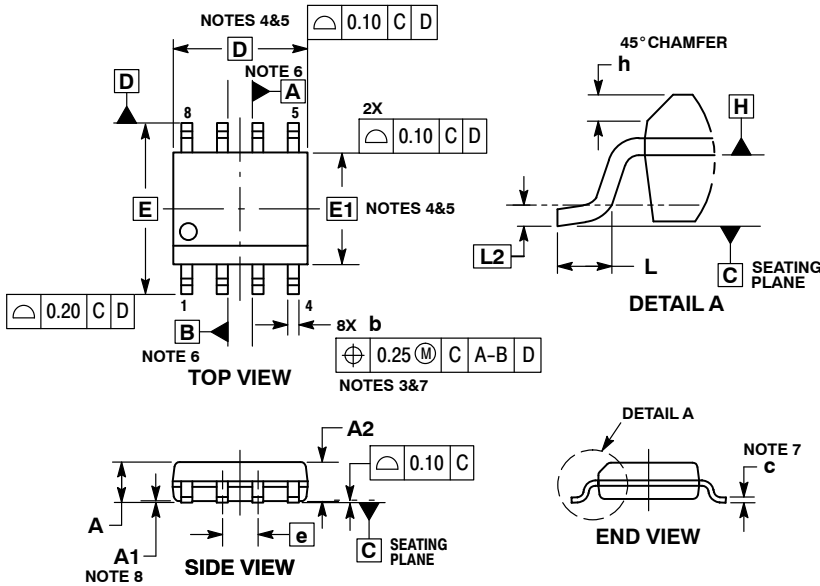
Part Number	Description	Temperature Range	Package	Shipping†
NCV7344D10R2G	High Speed Low Power CAN, CANFD Transceiver	–40°C to +125°C	SOIC 150 8 GREEN (Matte Sn, JEDEC MS–012) (Pb–Free)	3000 / Tape & Reel
NCV7344D13R2G	High Speed Low Power CAN, CANFD Transceiver with $V_{IO}$ pin			
NCV7344MW0R2G	High Speed Low Power CAN, CANFD Transceiver	–40°C to +150°C	DFN 8 Wettable Flank (Pb–Free)	3000 / Tape & Reel
NCV7344MW3R2G	High Speed Low Power CAN, CANFD Transceiver with $V_{IO}$ pin			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCV7344

## PACKAGE DIMENSIONS

### SOIC-8 CASE 751AZ ISSUE B

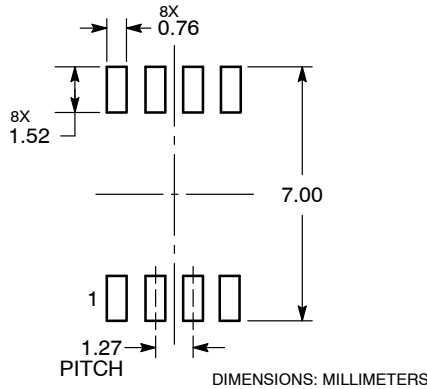


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

### RECOMMENDED SOLDERING FOOTPRINT\*

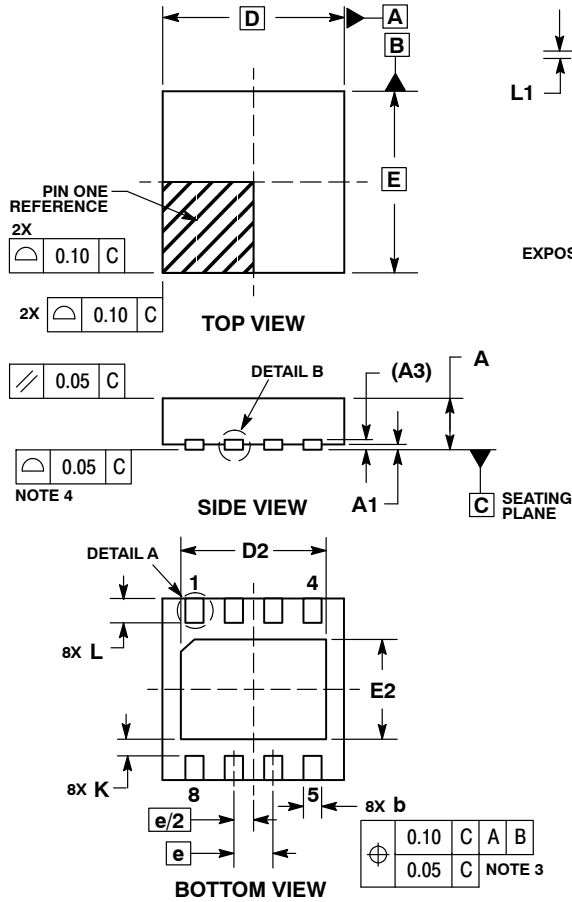


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NCV7344

## PACKAGE DIMENSIONS

### DFN8, 3x3, 0.65P CASE 506BW ISSUE O

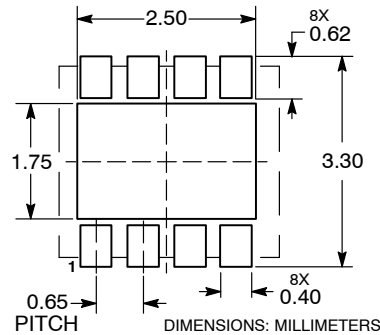


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.25	0.35
D	3.00	BSC
D2	2.30	2.50
E	3.00	BSC
E2	1.55	1.75
e	0.65	BSC
K	0.20	---
L	0.35	0.45
L1	0.00	0.15

#### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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