TOPAZ SEMICONDUCTOR

T-29-27

# TZ5911

# N-CHANNEL DEPLETION-MODE DUAL D-MOS FET

## ORDERING INFORMATION

| | |
|---|---|
| TO-78 Hermetic Package | TZ5911HD |
| SO-8 Surface Mount Package | TZ5911CY |

## FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- Available in surface mount package
- Pin and Function Compatible to Industry Standard Dual J-FETs with addition of Substrate Bias Pin

## APPLICATIONS

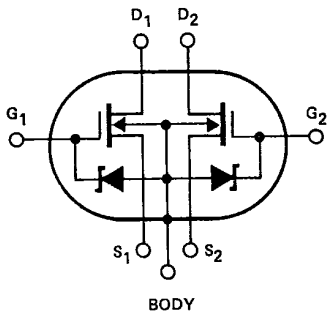
- High-Speed Analog Comparators
- Wide-Band Differential Amplifiers
- Cascode Amplifiers
- High Intercept Point Balanced Mixers

## ABSOLUTE MAXIMUM RATINGS (per side, $T_A$ = +25°C unless otherwise noted)

$V_{DS}$ Drain-Source Voltage ..... +20V
$V_{SD}$ Source-Drain Voltage ..... +10V
$V_{DB}$ Drain-Body Voltage ..... +25V
$V_{SB}$ Source-Body Voltage ..... +15V
$V_{GD}$ Gate-Drain Voltage ..... +25V
$V_{GS}$ Gate-Source Voltage ..... +25V
$V_{GB}$ Gate-Body Voltage ..... +25V
$V_{G1G2}$ Gate-to-Gate Voltage ..... +25V
$V_{D1D2}$ Drain-to-Drain Voltage ..... +25V
$V_{S1S2}$ Source-to-Source Voltage ..... +15V

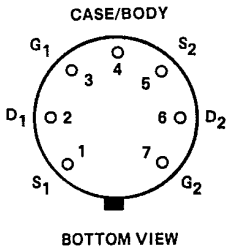
$I_D$ Continuous Drain Current ..... +50 mA
$P_D$ Device Dissipation (each side) ..... 360 mW
Derating Factor ..... 2.88 mW/°C
$P_D$ Total Device Dissipation ..... 500 mW
Derating Factor ..... 4 mW/°C
Operating Junction and Storage Temperature Range ..... -55 to +150°C
$T_L$ Lead Temperature (1/16" from mounting surface for 10 sec.) ..... +260°C

## SCHEMATIC DIAGRAM




## PIN CONFIGURATIONS

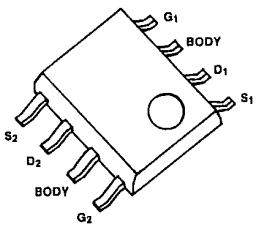
TO-78




BOTTOM VIEW

(See Package 4)

SO-8




(See Package 19)

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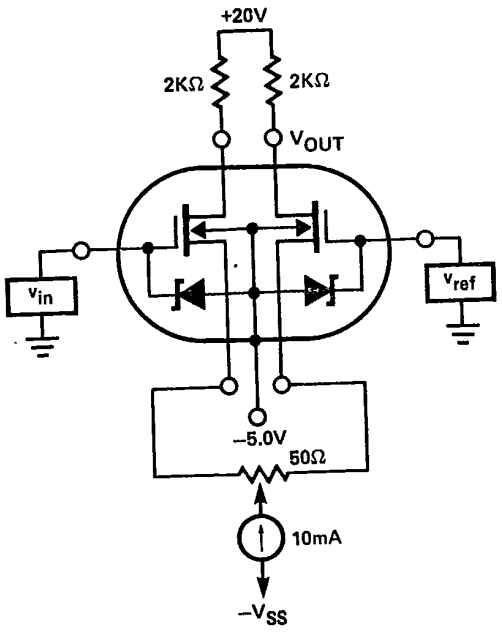
**TZ5911**

**ELECTRICAL CHARACTERISTICS** ($T_A$ = +25°C, per side, unless otherwise noted)

| # | | CHARACTERISTIC | | MIN | TYP | MAX | UNITS | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | STATIC | $BV_{DS}$ | Drain-Source Breakdown Voltage | 20 | | | V | $I_D$ = 10nA, $V_{GS}$ = $V_{BS}$ = -5V | |
| 2 | | $BV_{SD}$ | Source-Drain Breakdown Voltage | 10 | | | | $I_S$ = 10nA, $V_{GD}$ = $V_{BD}$ = -5V | |
| 3 | | $BV_{DB}$ | Drain-Body Breakdown Voltage | 25 | | | | $I_D$ = 10nA, $V_{GB}$ = 0 Source Open | |
| 4 | | $BV_{SB}$ | Source-Body Breakdown Voltage | 15 | | | | $I_S$ = 10μA, $V_{GB}$ = 0 Drain open | |
| 5 | | $I_{GSS(fwd)}$ | Forward Gate Leakage Current | | | 1.0 | nA | $V_{GS}$ = 25V, $V_{DS}$ = $V_{BS}$ = 0 | |
| 6 | | $I_G$ | Gate Operating Current | | -3.0 | -100 | pA | $V_{DG}$ = 20V, $I_D$ = 5.0 mA, $V_{BS}$ = -5.6V | |
| 7 | | | | | -0.7 | -10 | nA | $V_{DG}$ = 20V, $I_D$ = 5.0 mA, $V_{BS}$ = -5.6V | $T_A$ = +125°C |
| 8 | | $V_{GS(off)}$ | Gate-Source Cutoff Voltage | -1.0 | | -5.0 | V | $V_{DS}$ = 10V, $I_D$ = 1.0nA, $V_{BS}$ = -5.6V | |
| 9 | | $V_{GS(on)}$ | Gate-Source ON Voltage | -0.3 | | -3.0 | | $V_{DG}$ = 10V, $I_D$ = 5mA, $V_{BS}$ = -5.6V | |
| 10 | | $I_{DSX}$ | Zero Gate Voltage[1] Drain Current | 7.0 | | 40 | mA | $V_{DS}$ = 10V, $V_{GS}$ = 0, $V_{BS}$ = -5.6V | |
| 11 | | | | 5.0 | | | | $V_{DS}$ = 10V, $V_{GS}$ = 0, $V_{BS}$ = -5.6V | $T_A$ = +125°C |
| 12 | | $r_{DS(ON)}$ | Drain-Source ON Resistance | | 100 | 150 | ohms | $I_D$ = 1.0mA, $V_{GS}$ = 0, $V_{BS}$ = -5.6V | |
| 13 | DYNAMIC | $g_{fs}$ | Common-Source[1] Forward Transcond. | 5.0 | 7.5 | 10 | mmhos | $V_{DG}$ = 10V, $I_D$ = 5.0 mA, $V_{BS}$ = -5.6V | f = 1 KHz |
| 14 | | $g_{os}$ | Common-Source Output Conductance | | 200 | | μmhos | | |
| 15 | | $C_{iss}$ | Common-Source Input Capacitance | | 3.5 | | pF | | f = 1 MHz |
| 16 | | $C_{oss}$ | Common-Source Output Capacitance | | 1.2 | | | | |
| 17 | | $C_{rss}$ | Common Source Reverse Transfer Capacitance | | 0.3 | | | | |
| 18 | | $C_{(gs + sb)}$ | Source Node Capacitance | | 4.5 | | | | |
| 19 | MATCHING | $\lvert V_{GS1}-V_{GS2}\rvert$ | Differential Gate Source Voltage | | 20 | | mV | $V_{DG}$ = 10V, $I_D$ = 5.0 mA, $V_{BS}$ = -5.6V | |
| 20 | | $\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$ | Differential Drift | | 20 | | μV/°C | | $T_A$ = -55°C to +125°C |
| 21 | | $I_{DSX\ 1/2}$ | Zero Gate Voltage[1,2] Drain Current Ratio | 0.90 | | 1.0 | | | |
| 22 | | $g_{fs\ 1/2}$ | Transcond. Ratio[1,2] | 0.90 | | 1.0 | | | f = 1 KHz |

**Note 1:** Pulse Test, 80μsec, 1% Duty Cycle
**Note 2:** The lower value is side 1.

## DIFFERENTIAL AMPLIFIER/COMPARATOR




PERFORMANCE CHARACTERISTICS ($T_A$ = +25°C)

Low Frequency Differential Voltage Gain—6.2 min., 11.8 typ.

$V_{in}$, $V_{ref}$ range—–5.0V to +10V

$V_{out}$ max.—+20V

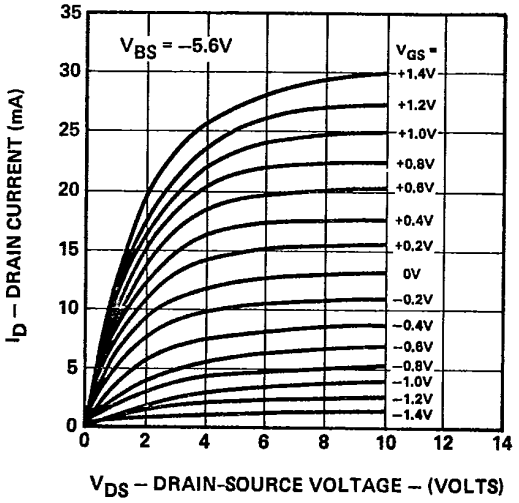
Input Bias Current—100 pA max., 4 pA typ.

Differential Input Bias Current—0.4 pA typ.

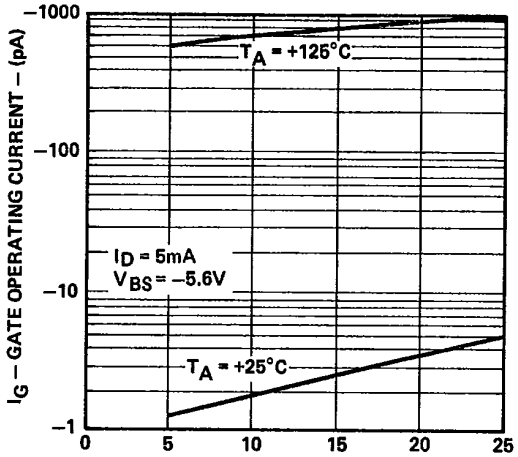
Gate Voltages must be positive with respect to Body (Substrate) Voltage at all times.

**TYPICAL PERFORMANCE CHARACTERISTICS** ($T_A$ = +25°C, per side, unless otherwise specified)

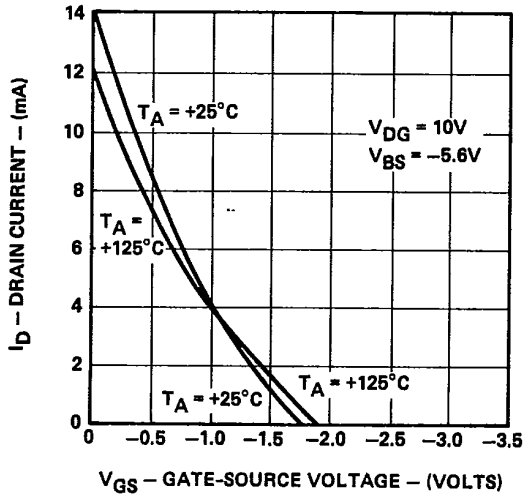
OUTPUT CHARACTERISTIC




GATE OPERATING CURRENT —VS— DRAIN-GATE VOLTAGE




TRANSFER CHARACTERISTIC




FORWARD TRANSCONDUCTANCE —VS— DRAIN CURRENT