United Monolithic Semiconductors

CHK015A-QIA

15W Power Packaged Transistor

GaN HEMT on SiC

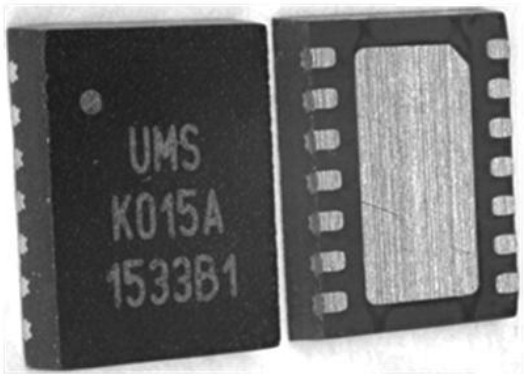
Description

The CHK015A-QIA is an unmatched packaged Gallium Nitride High Electron Mobility Transistor.

It offers general purpose and broadband solutions for a variety of RF power applications. It is well suited for multi-purpose applications such as radar and telecommunication.

The CHK015A-QIA is developed on a 0.5µm gate length GaN HEMT process. It requires an external matching circuitry.

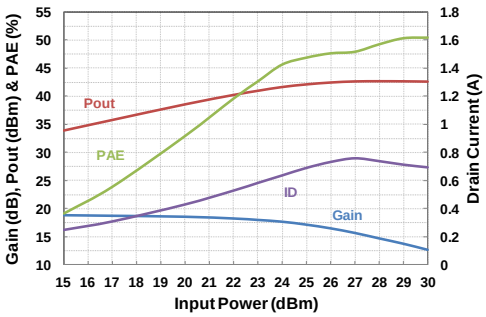
It is proposed in low cost plastic package providing low parasitic and low thermal resistance.



Main Features

- Wide band capability: up to 6GHz
- Pulsed and CW operating modes
- High power: > 15W
- High Efficiency: up to 70%
- DC bias: Vd=50Volt @ Id=100mA
- Low cost package: 14L-DFN3x4
- MTTF > 10^6 hours @ Tj=200°C

V_{DS} = 50V, I_{D_Q} = 100mA, Freq = 2.9GHz
Pulsed mode (100µs, 10%)



Performances on S-band Evaluation Board

Main Electrical Characteristics

Tcase= +25°C, **Pulsed mode**, F = 3GHz, V_{DS}=50V, I_{D_Q}=100mA

Symbol	Parameter	Min	Typ	Max	Unit
Gain	Linear Gain	18	20		dB
Pout	Output Power	15	20		W
PAE	Max Power Added Efficiency		60		%
G_{PAE_MAX}	Associated Gain at Max PAE		16		dB

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Recommended DC Operating Ratings

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage			50	V	
V_{GS_Q}	Gate to Source Voltage		-1.9		V	V_D=50V. I_{D_Q}=100mA
I_{D_Q}	Quiescent Drain Current		0.1	0.35	A	V_D=50V
I_{D_MAX}	Drain Current		0.65	(1)	A	V_D=50V. compressed mode
I_{G_MAX}	Gate Current (forward mode)		0	24	mA	Compressed mode
T_{j_MAX}	Junction temperature(1)			200	°C	

(1) Power dissipation must be considered

DC Characteristics

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-3	-2	-1	V	V_D=50V. I_D= I_{DSS} /100
I_{D_SAT}	Saturated Drain Current		2.7 (1)		A	V_D=7V. V_G=2V
I_{G_leak}	Gate Leakage Current (reverse mode)	-0.8			mA	V_D=50V. V_G=-7V
V_{BDS}	Drain-Source Break-down Voltage		180		V	V_G=-7V. I_D=20mA
R_{TH}	Thermal Resistance (2)		6		°C/W	CW

(1) For information, limited by I_{D_MAX} . see on Absolute Maximum Ratings

(2) CW mode, reference = package back-side

RF Characteristics

Tcase= +25°C. Pulsed mode

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
G_{SS}	Small Signal Gain @ 3GHz Small Signal Gain @ 6GHz	18 11	20 13		dB dB	V_D=50V. I_{D_Q}=100mA
P_{SAT}	Saturated Output Power	15	20		W	V_D=50V. I_{D_Q}=100mA
PAE	Max PAE @ 3GHz Max PAE @ 6GHz		60 50		% %	V_D=50V. I_{D_Q}=100mA
G_{PAE_MAX}	Associated Gain at Max PAE @ 3GHz @ 6GHz		 16 9		 dB dB	V_D=50V. I_{D_Q}=100mA

These values are the intrinsic performance of the packaged device. They are deduced from measurements and simulations. They are considered in the reference plane defined by the leads of the package, at the connection interface with the PCB.

The typical performance achievable in more than 10% frequency band around 3GHz was demonstrated using the reference board 61502522 presented hereafter.

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Absolute Maximum Ratings

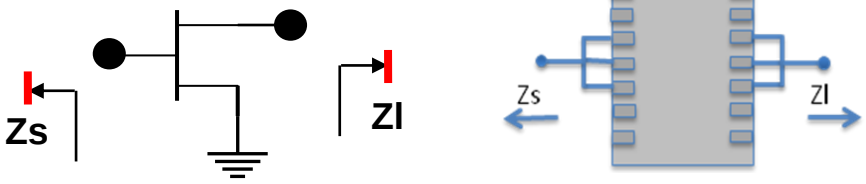
Tcase= +25°C[(1) (2) (3)]

Symbol	Parameter	Rating	Unit	Note
V_{DS}	Drain-Source Biasing Voltage	60	V	
V_{GS_Q}	Gate-Source Biasing Voltage	-10. +2	V	
I_{G_MAX}	Maximum Gate Current (forward mode)	48	mA	
I_{G_MIN}	Minimum Gate Current (reverse mode)	-2	mA	
I_{D_MAX}	Maximum Drain Current	2	A	(4)
P_{IN}	Maximum Input Power			(5)
T_j	Junction Temperature	220	°C	
T_{STG}	Storage Temperature	-55 to +150	°C	
T_{Case}	Case Operating Temperature	See note	°C	(4)

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.
(3) The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other. Otherwise deterioration or destruction of the device may take place.
(4) Max junction temperature must be considered
(5) Linked to and limited by I_{G_MAX} & I_{G_MIN} values. Maximum input power depends on frequency.

Simulated Source and Load Impedances

V_{DS} = 50V. I_{D_Q} = 100mA



Frequency (MHz)	Zs	Zl	Pout (W)	PAE (%)
1000	2.96+ j13.07	39.21+ j33.14	21.16	66.69
2000	1.67+ j3.96	18.07+ j24.40	20.88	64.09
3000	1.79- j0.80	11.08+ j17.47	20.68	61.61
4000	1.57- j4.15	6.76+ j10.26	20.40	58.47
5000	1.68- j7.33	4.70+ j5.82	19.92	56.04
6000	2.04- j10.45	4.05+ j2.61	19.32	52.49

The impedances are chosen as a trade-off between Output Power. PAE and Stability of the device. These values are given in the reference plane defined by the connection between the transistor leads and the PCB according to the footprint above mentioned

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Typical Simulated Package Sij parameters

Tamb. = +25°C. V_{DS} = 50V. I_{D_Q} = 100mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.25	0.930	-86.7	0.018	38.8	30.010	129.0	0.610	-44.6
0.50	0.890	-125.0	0.022	16.0	18.860	104.5	0.490	-65.2
0.75	0.880	-142.9	0.023	3.1	13.170	90.3	0.460	-77.7
1.00	0.880	-153.1	0.023	-6.0	9.930	80.0	0.470	-87.5
1.25	0.880	-159.8	0.023	-13.2	7.860	71.6	0.500	-95.9
1.50	0.880	-164.8	0.022	-19.4	6.420	64.3	0.530	-103.2
1.75	0.890	-168.7	0.021	-24.8	5.380	57.7	0.560	-109.9
2.00	0.890	-171.9	0.020	-29.6	4.580	51.7	0.600	-115.8
2.25	0.890	-174.7	0.019	-33.9	3.960	46.1	0.630	-121.3
2.50	0.900	-177.2	0.019	-37.9	3.460	40.9	0.660	-126.3
2.75	0.900	-179.6	0.018	-41.5	3.050	36.0	0.680	-130.9
3.00	0.900	178.3	0.017	-44.7	2.710	31.5	0.710	-135.2
3.25	0.900	176.2	0.016	-47.7	2.430	27.1	0.730	-139.2
3.50	0.910	174.2	0.015	-50.4	2.190	23.0	0.750	-142.9
3.75	0.910	172.3	0.014	-52.8	1.990	19.0	0.770	-146.4
4.00	0.910	170.5	0.013	-54.9	1.810	15.3	0.780	-149.7
4.25	0.910	168.6	0.012	-56.7	1.660	11.7	0.800	-152.8
4.50	0.910	166.8	0.011	-58.3	1.530	8.2	0.810	-155.8
4.75	0.910	165.1	0.010	-59.6	1.420	4.8	0.820	-158.7
5.00	0.910	163.3	0.009	-60.5	1.320	1.6	0.830	-161.4
5.25	0.910	161.6	0.009	-61.0	1.230	-1.6	0.840	-164.0
5.50	0.910	159.8	0.008	-61.0	1.150	-4.7	0.850	-166.5
5.75	0.910	158.0	0.007	-60.5	1.090	-7.7	0.850	-168.9
6.00	0.910	156.3	0.007	-59.2	1.020	-10.6	0.860	-171.3
6.25	0.910	154.5	0.006	-57.0	0.970	-13.5	0.860	-173.6
6.50	0.910	152.7	0.005	-53.6	0.920	-16.4	0.870	-175.9
6.75	0.910	150.9	0.005	-48.6	0.880	-19.2	0.870	-178.1
7.00	0.910	149.1	0.004	-41.6	0.840	-22.0	0.880	179.8
7.25	0.910	147.2	0.004	-32.5	0.800	-24.8	0.880	177.6
7.50	0.910	145.4	0.004	-21.7	0.770	-27.5	0.880	175.5
7.75	0.910	143.4	0.004	-10.4	0.740	-30.2	0.890	173.4
8.00	0.910	141.5	0.004	0.2	0.720	-33.0	0.890	171.4
8.25	0.910	139.5	0.005	8.8	0.690	-35.7	0.890	169.3
8.50	0.900	137.5	0.005	15.4	0.670	-38.4	0.890	167.2
8.75	0.900	135.4	0.006	20.0	0.650	-41.1	0.890	165.2
9.00	0.900	133.3	0.007	23.2	0.630	-43.9	0.890	163.1
9.25	0.900	131.1	0.008	25.2	0.620	-46.6	0.900	161.0
9.50	0.900	128.8	0.009	26.3	0.600	-49.4	0.900	158.9
9.75	0.890	126.5	0.010	26.7	0.590	-52.2	0.900	156.8
10.00	0.890	124.2	0.011	26.6	0.580	-55.0	0.900	154.6
10.25	0.890	121.7	0.012	26.1	0.570	-57.8	0.900	152.5
10.50	0.880	119.2	0.014	25.2	0.560	-60.7	0.900	150.3
11.00	0.880	113.9	0.016	22.6	0.540	-66.6	0.900	145.8

These values are given in the reference plane defined by the connection between the transistor leads and the PCB according to the footprint previously mentioned

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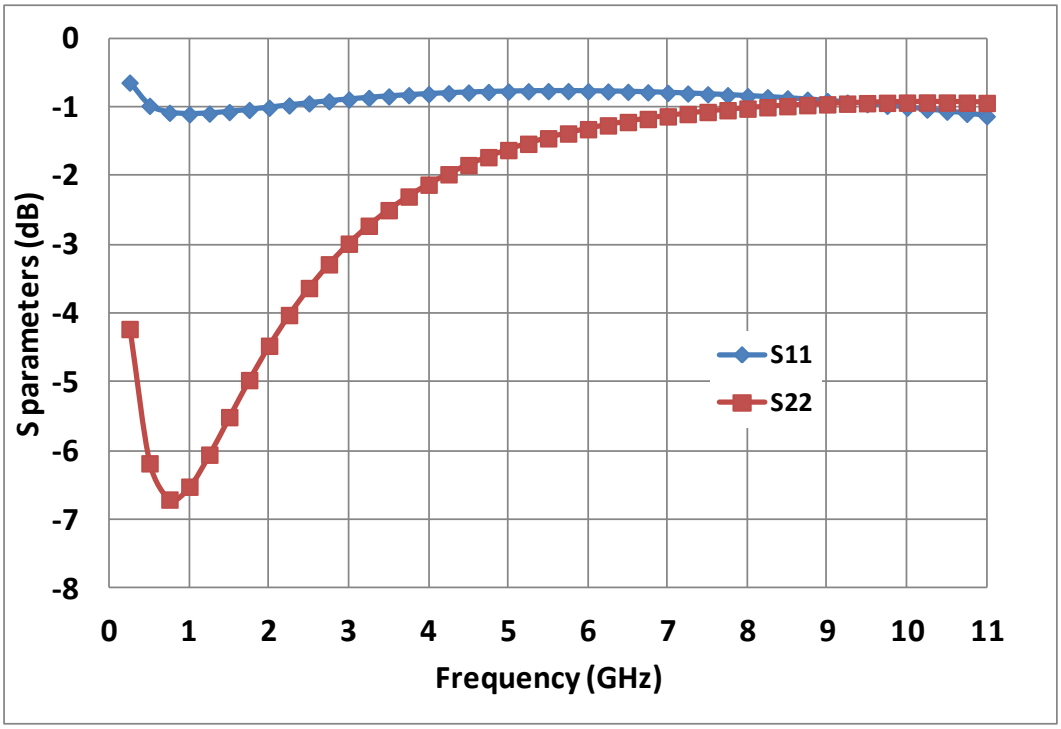
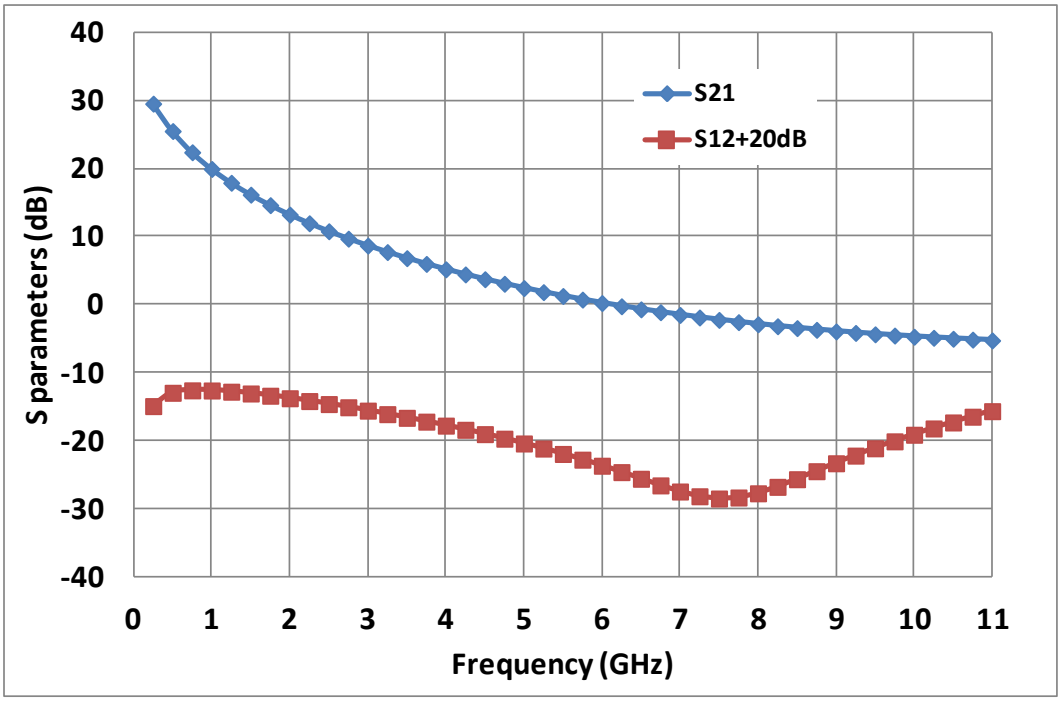
Typical Simulated S-parameters

Tcase = +25°C. CW mode. V_{DS}=50V. I_{D_Q}=100mA.





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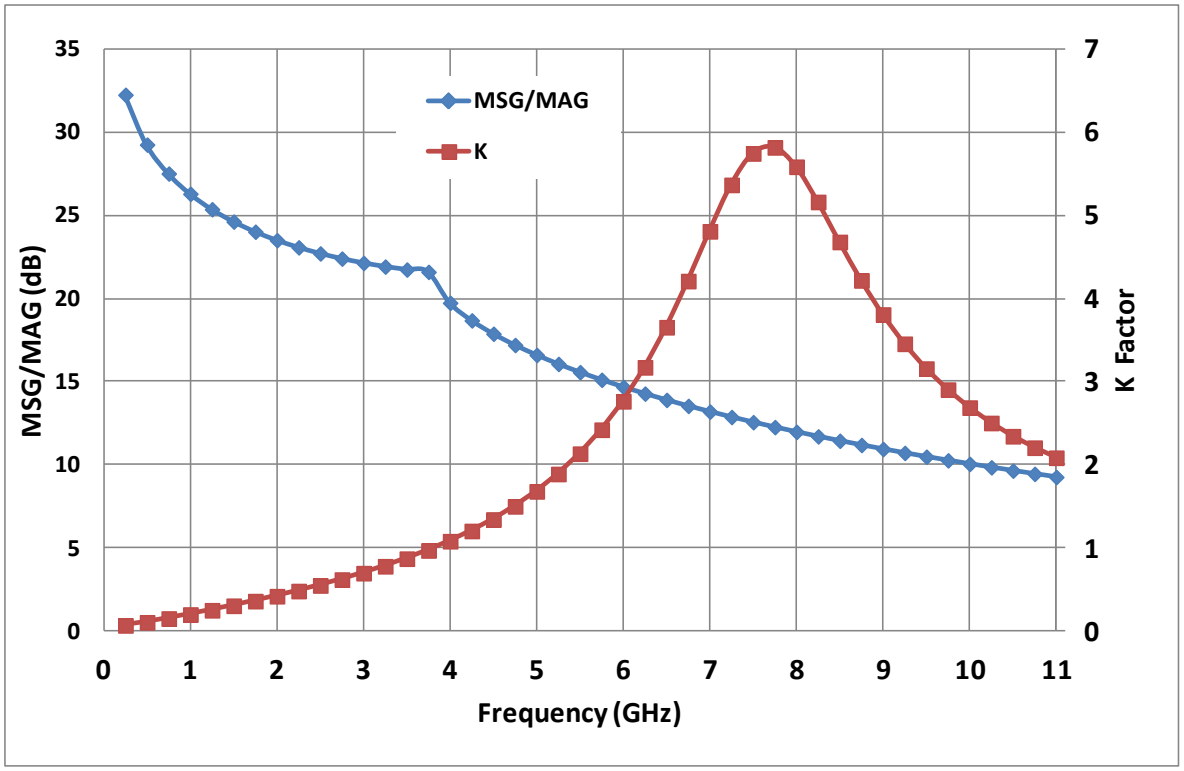
Simulated Maximum Gain & Stability Characteristics

Tcase= +25°C. CW mode. V_{DS}=50V. I_{D_Q}=100mA



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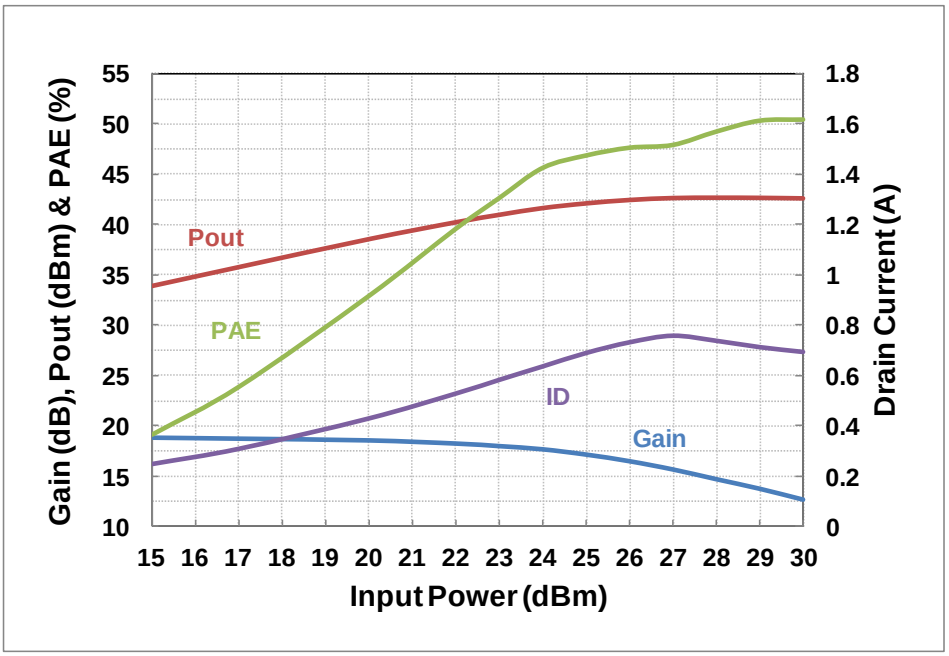
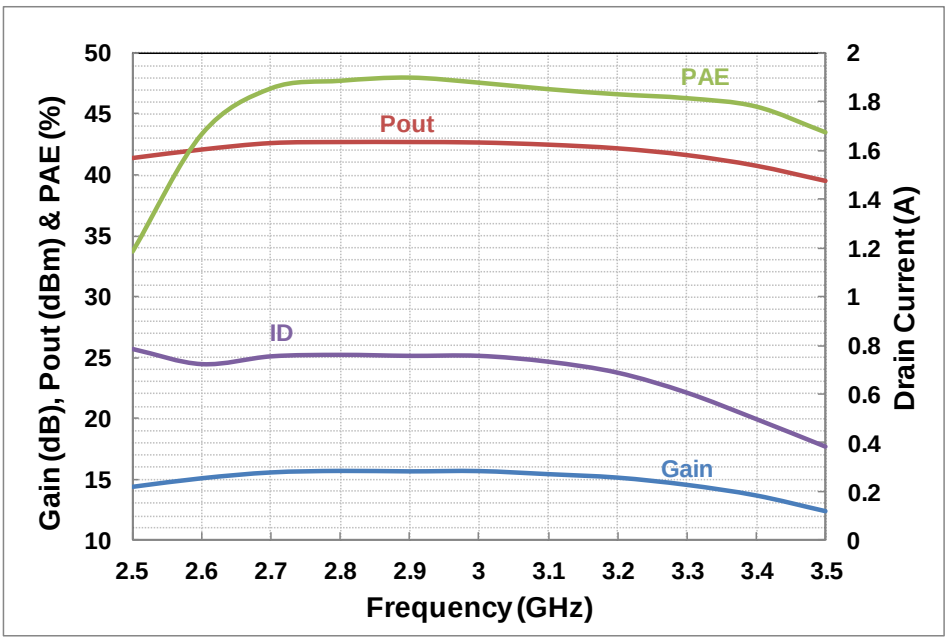
Typical Performance on Evaluation Board (ref 61502522)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = +25°C. Pulsed Mode [1]. V_{DS}=50V. I_{D_Q}=100mA

Pout. PAE. Gain & ID @ Freq=2.9GHz



Pout. PAE. Gain & ID @ Pin=27dBm



[1] Input RF and gate voltage are pulsed. Conditions are 100µs width. 10% duty cycle and 1µs offset between DC and RF pulse.

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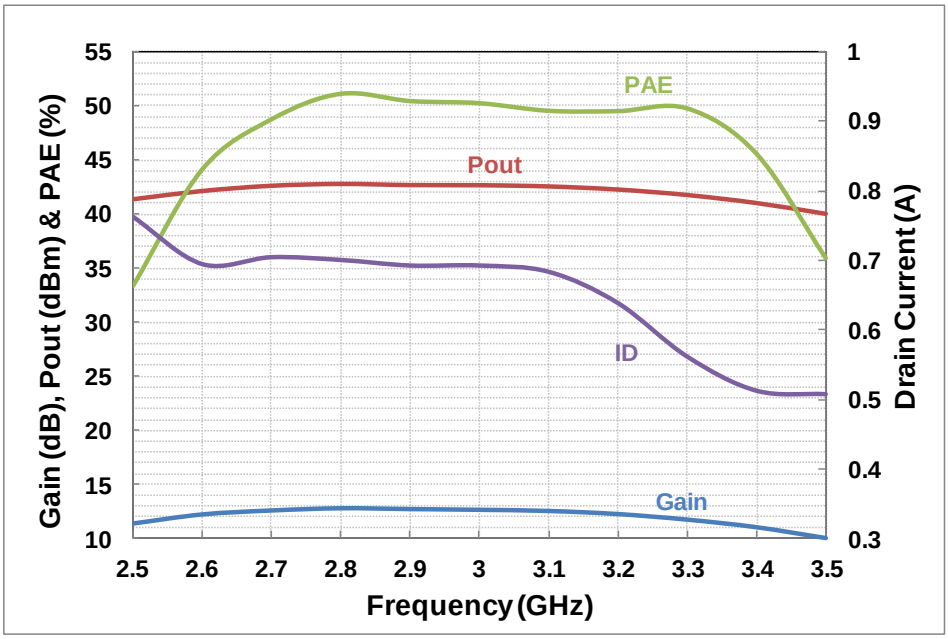
Typical Performance on Evaluation Board (ref 61502522)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = +25°C. Pulsed Mode [(1)]. V_{DS}=50V. I_{D_Q}=100mA

Pout. PAE. Gain & ID @ Pin=30dBm



[(1)] Input RF and gate voltage are pulsed. Conditions are 100µs width. 10% duty cycle and 1µs offset between DC and RF pulse.

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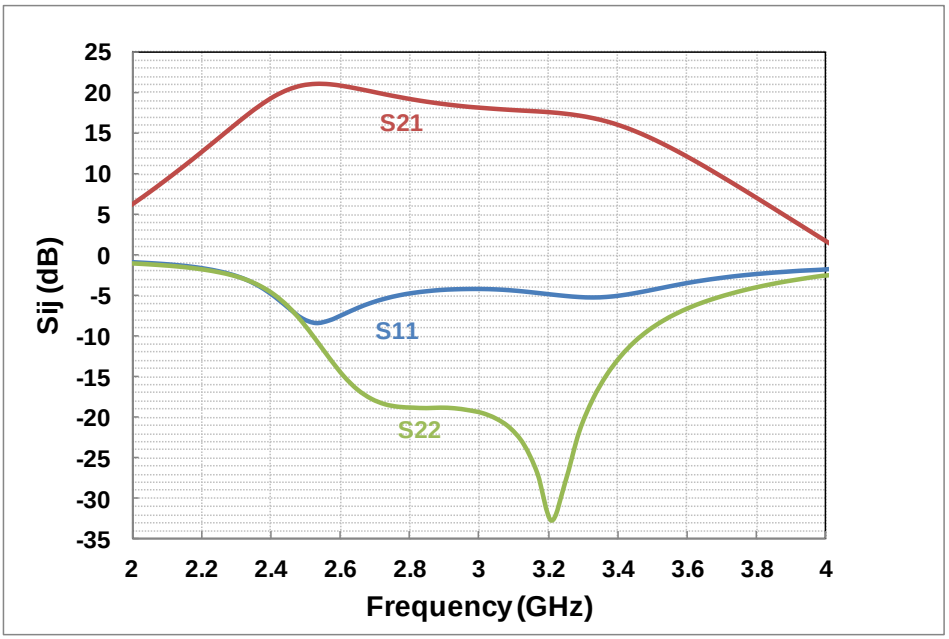
Typical Performance on Evaluation Board (ref 61502522)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = +25°C. CW mode. V_{DS}=50V. I_{D_Q}=100mA

S parameters versus frequency



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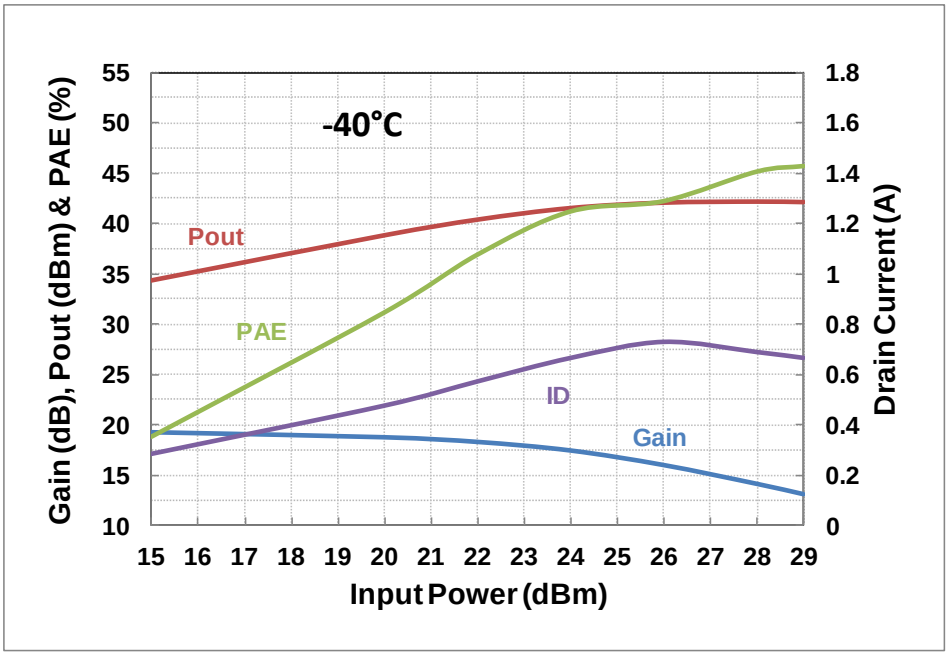
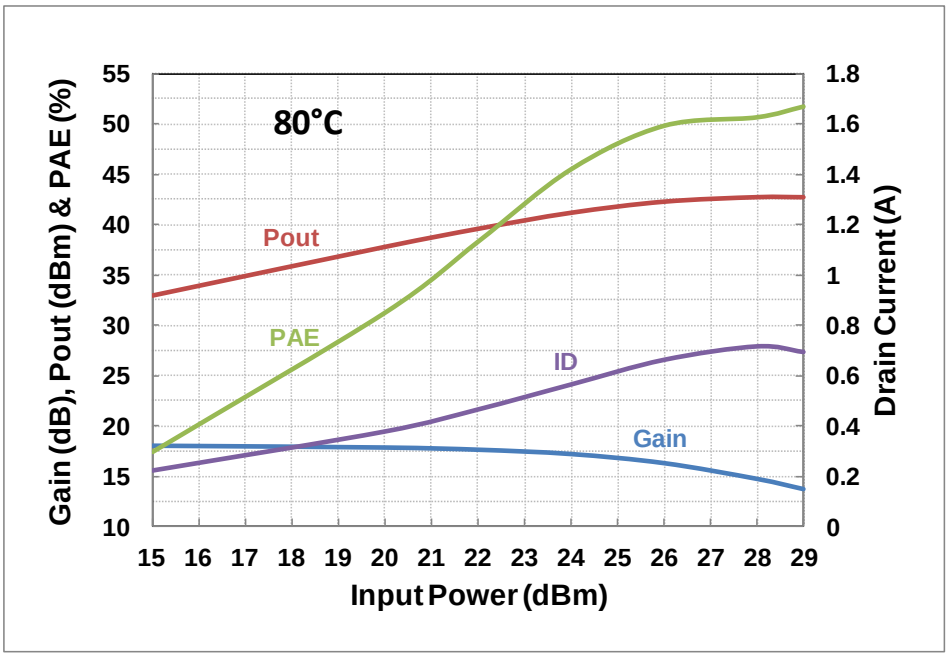
Typical Performance in Temperature (on Evaluation Board)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = -40°C, +80°C, Pulsed Mode [(1)], V_{DS}=50V, I_{D_Q}=100mA

Pout, PAE, Gain & Id @ 2.9GHz & -40°C



Pout, PAE, Gain & Id @ 2.9GHz & +80°C



[(1)] Input RF and gate voltage are pulsed. Conditions are 100µs width, 10% duty cycle and 1µs offset between DC and RF pulse.

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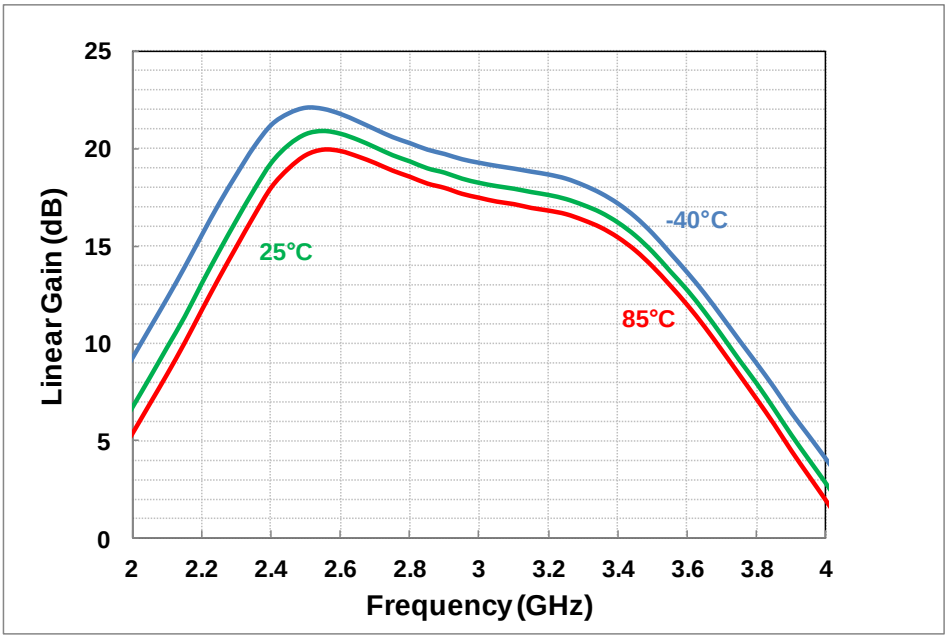
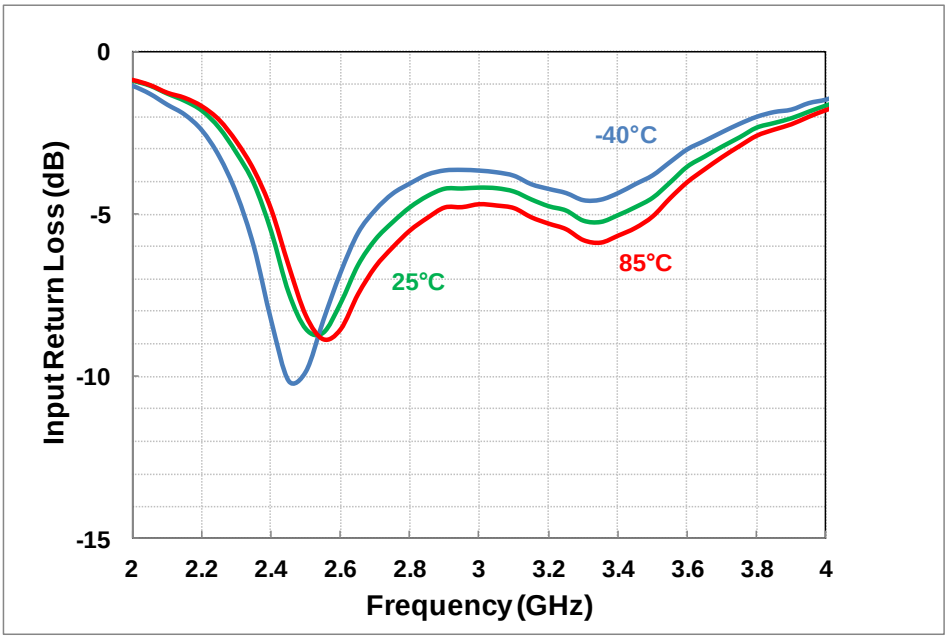
Typical Performance in Temperature (on Evaluation Board)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = -40°C, +25°C, +85°C, CW mode. V_{DS}=50V, I_{D_Q}=100mA (fixed @ +25°C)

Linear Gain versus temperature with ID_Q fixed @ each temperature (100mA)



Input Return Loss versus temperature with I_{D_Q} fixed @ each temperature (100mA)



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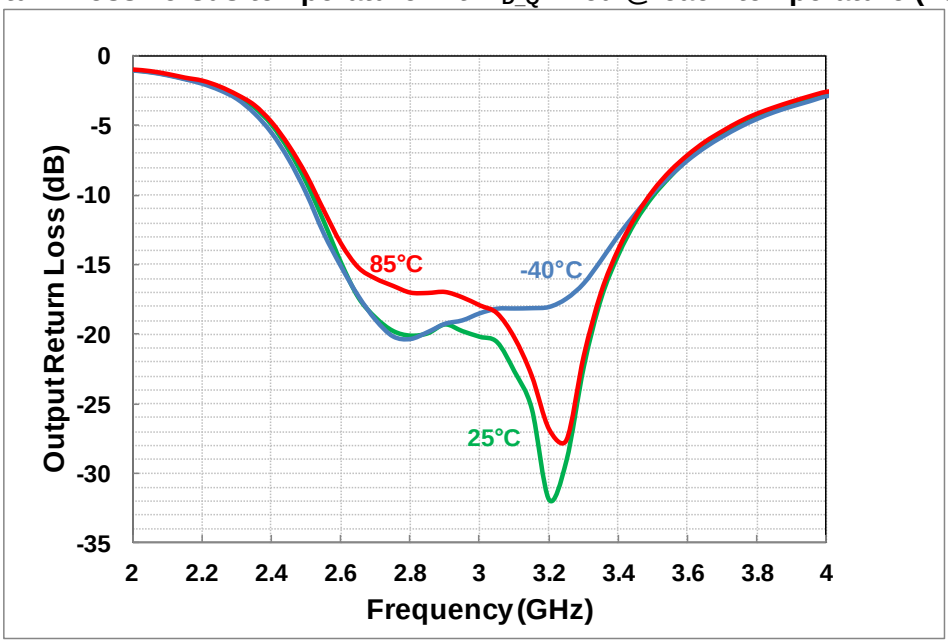
Typical Performance in Temperature (on Evaluation Board)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = -40°C, +25°C, +85°C, CW mode. VDS=50V, ID_Q=100mA (fixed @ +25°C)

Output Return Loss versus temperature with I_{D_Q} fixed @ each temperature (100mA)



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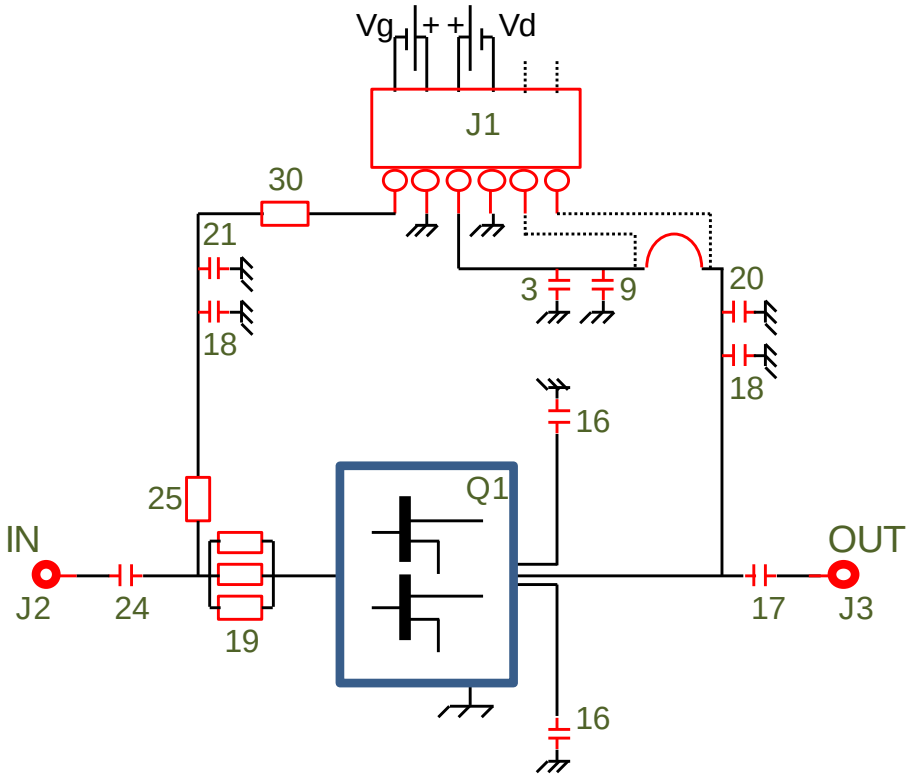
Demonstration Amplifier Low Frequency Equivalent Schematic (Ref. 61502522)



Demonstration Amplifier Bill of Materials (Ref. 61502522)

Designator	Type	Value - Description	Qty
24	Capacitor	1pF. +/- 0.1pF. 0603	1
16	Capacitor	4.7pF. +/- 0.25pF. 0603	1
17	Capacitor	3.9pF. +/- 0.25pF. 0603	1
18	Capacitor	20pF. +/- 5%. 0603	2
20	Capacitor	100pF. +/- 5%. 0603	1
21	Capacitor	1nF. +/- 5%. 0805	1
9	Capacitor	1µF. +/- 10%. 1210	1
3	Capacitor	68µF. +/- 20%	1
25	Resistor	49.9Ω. +/- 1%. 0603	1
19	Resistor	3Ω +/- 1%. 0603	3
30	Resistor	100Ω +/- 1%. 0603	1
J1	Connector	CMS 6cts	1
J2. J3	Connector	SMA	2
Q1	Packaged Transistor	CHK015A-QIA	1
-	PCB	TACONIC RF35P h=0.203mm	-

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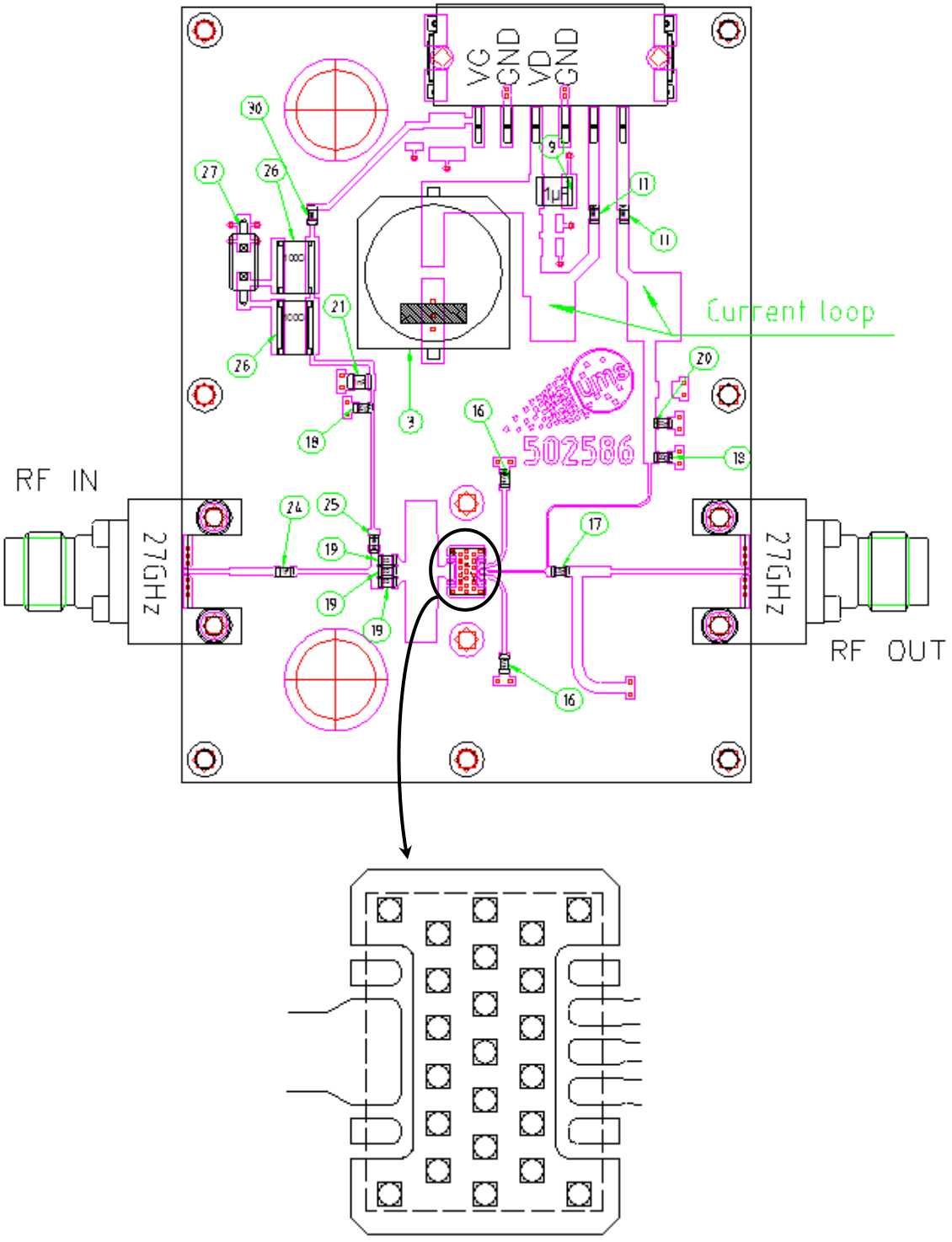
Demonstration Amplifier Circuit Outline (Ref. 61502522)



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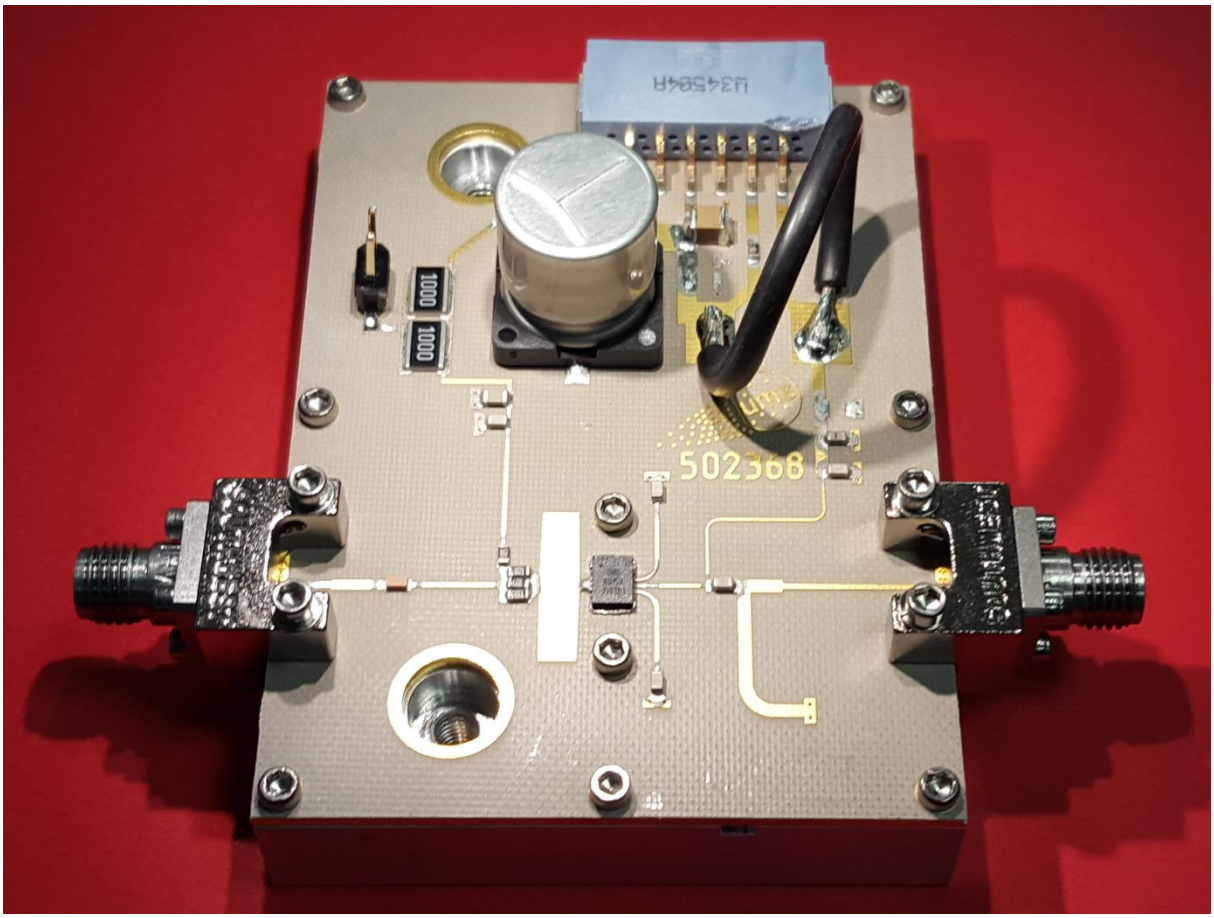
Demonstration Amplifier Circuit (Ref. 61502522)



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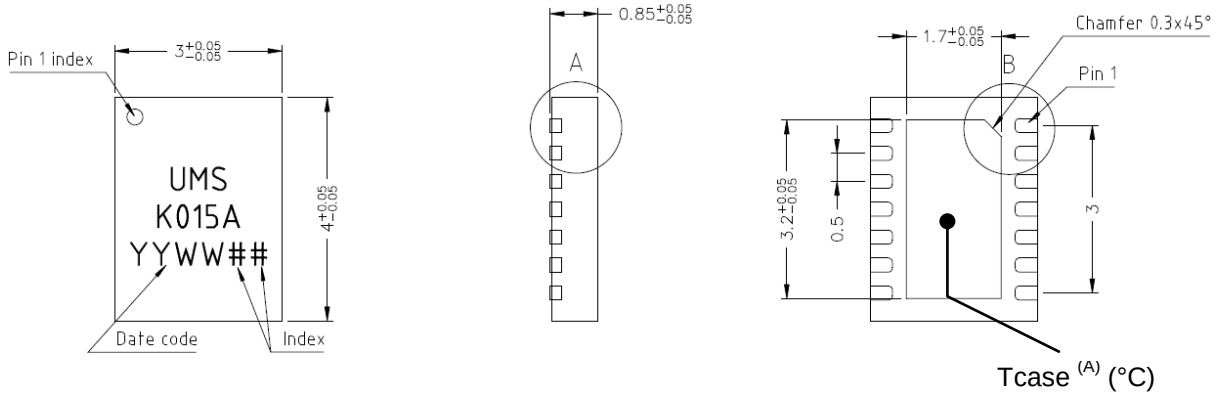
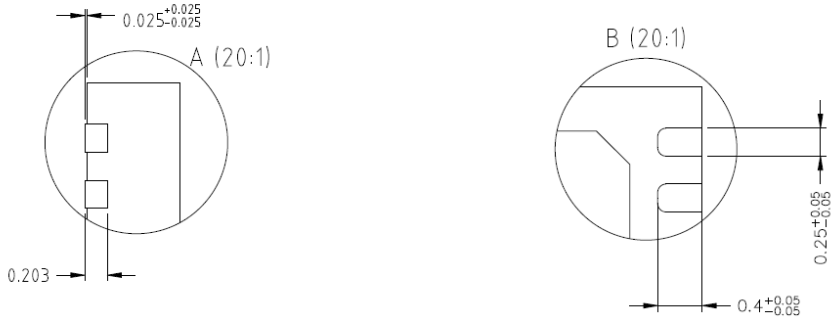
Package outline





Matte tin. Lead Free (Green)	1- Nc	6- Nc	11- D2
Units : mm	2- Nc	7- Nc	12- D1
From the standard : JEDEC MO-220	3- G1	8- Gnd	13- Nc
	4- G2	9- Nc	14- Gnd
15- Gnd	5- G3	10- D3	

(A) Tcase locates the reference point used to monitor the device temperature. This point has been taken at the device / system interface to ease system thermal design.

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Notes

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

DFN 3x4 package:	CHK015A-QIA/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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