

N-Channel Logic Level Enhancement Mode Power MOSFET

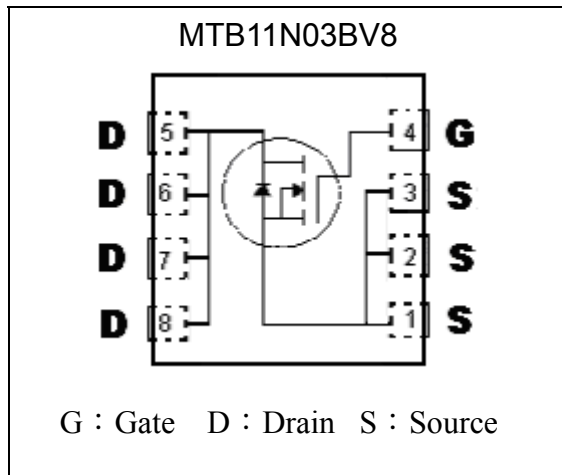
MTB11N03BV8

BV _{DSS}		30V
I _D @ T _C =25°C, V _{GS} =10V		44A
I _D @ T _A =25°C, V _{GS} =10V		14A
R _{DSON(TYP)}	V _{GS} =10V, I _D =14A	7.3mΩ
	V _{GS} =4.5V, I _D =12A	11.2mΩ

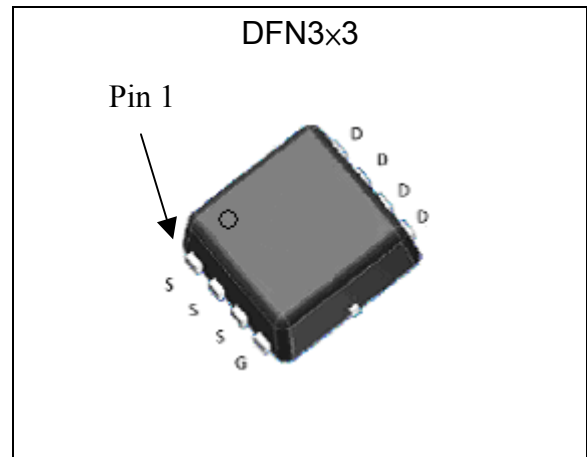
Features

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Pb-free lead plating and halogen-free package

Equivalent Circuit

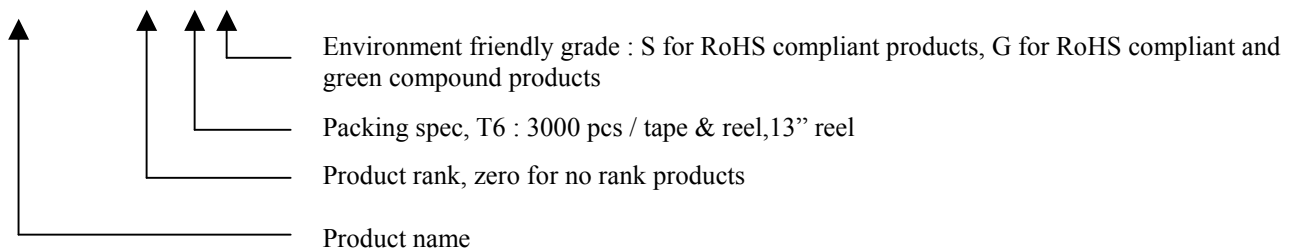


Outline



Ordering Information

Device	Package	Shipping
MTB11N03BV8-0-T6-G	DFN3x3 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C, unless otherwise specified)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V _{DS}	30	V	
Gate-Source Voltage	V _{GS}	±25		
Continuous Drain Current @ V _{GS} =10V, T _C =25°C(Silicon Limit)	I _D	44	A	
Continuous Drain Current @ V _{GS} =10V, T _C =100°C(Silicon Limit)		27.8		
Continuous Drain Current @ V _{GS} =10V, T _C =25°C(Package Limit)		26		
Continuous Drain Current @ V _{GS} =10V, T _A =25°C		14		
Continuous Drain Current @ V _{GS} =10V, T _A =70°C		11.2		
Pulsed Drain Current		I _{DM}		56 *1
Avalanche Current	I _{AS}	30		
Avalanche Energy @ L=0.1mH, I _D =21A, R _G =25Ω	E _{AS}	22	mJ	
Total Power Dissipation	P _D	T _C =25°C	36	W
		T _A =25°C	3.5 *2	
Operating Junction and Storage Temperature Range	T _j , T _{stg}	-55~+150	°C	

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	3.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{th,j-a}	36 *2	°C/W

Note : 1. Pulse width limited by maximum junction temperature.
 2. Surface mounted on a 1 in² pad of 2oz copper, ≤10s. In practice R_{th,j-a} will be determined by customer's PCB characteristics. 125°C/W when mounted on a minimum pad of 2 oz. copper.

Characteristics (T_C=25°C, unless otherwise specified)

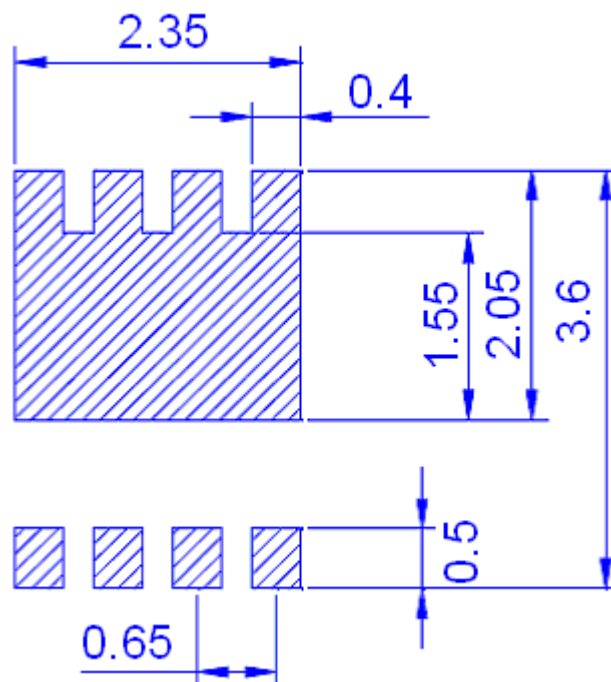
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
B _V D _{SS}	30	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	1.2	-	2.5		V _{DS} = V _{GS} , I _D =250μA
G _{FS} *1	-	18	-	S	V _{DS} =5V, I _D =11A
I _{GSS}	-	-	±100	nA	V _{GS} =±25V
I _{DSS}	-	-	1	μA	V _{DS} =30V, V _{GS} =0V
	-	-	5		V _{DS} =24V, V _{GS} =0V, T _j =55°C
R _{DS(ON)} *1	-	7.3	8.8	mΩ	V _{GS} =10V, I _D =14A
	-	11.2	13.4		V _{GS} =4.5V, I _D =12A
Dynamic					
C _{iss}	-	745	-	pF	V _{DS} =15V, V _{GS} =0V, f=1MHz
C _{oss}	-	168	-		
C _{rss}	-	95	-		
Q _g *1,2	-	15.8	-	nC	V _{DS} =15V, V _{GS} =10V, I _D =19A
Q _{gs} *1,2	-	3	-		
Q _{gd} *1,2	-	3.6	-		

Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
t _{d(ON)} *1, 2	-	9	13.5	ns	V _{DS} =15V, I _D =10A, V _{GS} =10V, R _{GS} =1 Ω
t _r *1, 2	-	15.8	23.7		
t _{d(OFF)} *1, 2	-	29.4	44.1		
t _f *1, 2	-	8.4	12.6		
t _{d(ON)} *1, 2	-	14.2	21.3	ns	V _{DS} =15V, I _D =10A, V _{GS} =4.5V, R _{GS} =1 Ω
t _r *1, 2	-	23	34.5		
t _{d(OFF)} *1, 2	-	19	28.5		
t _f *1, 2	-	12.2	18.3		
R _g	-	2.1	-	Ω	f=1MHz
Source-Drain Diode					
I _S *1	-	-	14	A	
I _{SM} *3	-	-	56		
V _{SD} *1	-	0.83	1.2	V	I _S =14A, V _{GS} =0V
t _{rr}	-	9.8	-	ns	I _F =10A, dI _F /dt=100A/μs
Q _{rr}	-	3.8	-	nC	

Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

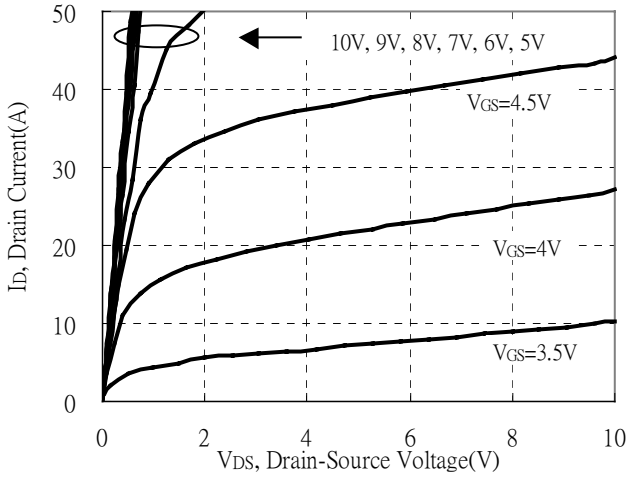
Recommended Soldering Footprint



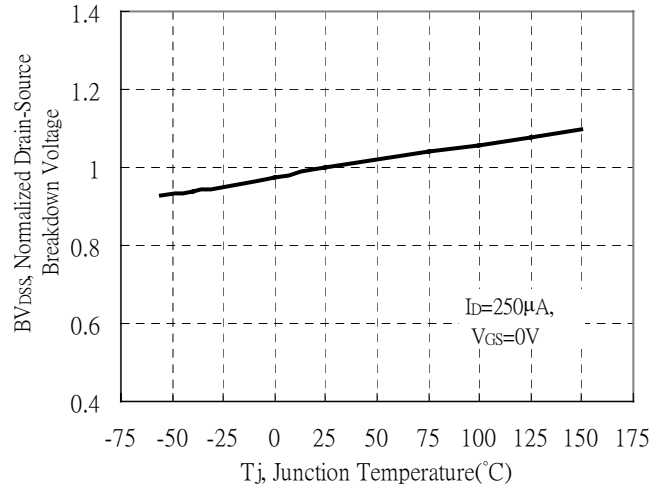
unit : mm

Typical Characteristics

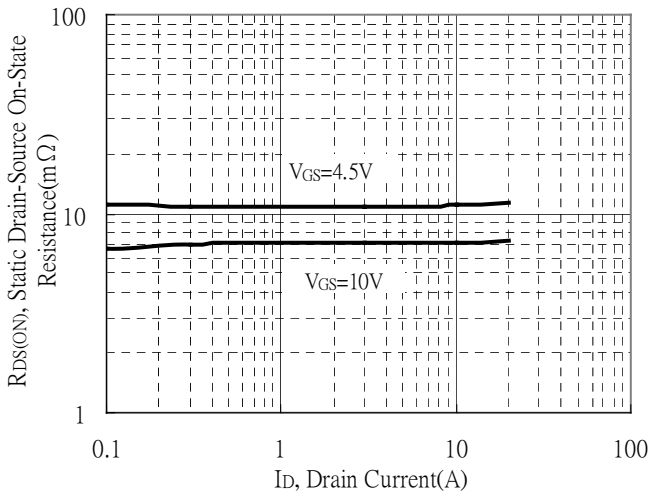
Typical Output Characteristics



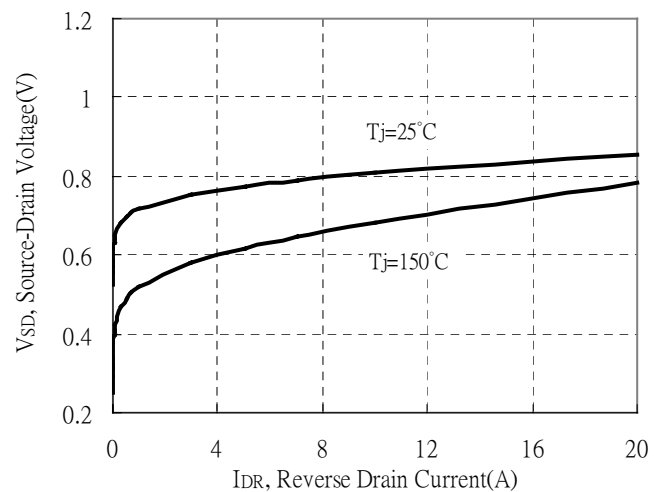
Breakdown Voltage vs Ambient Temperature



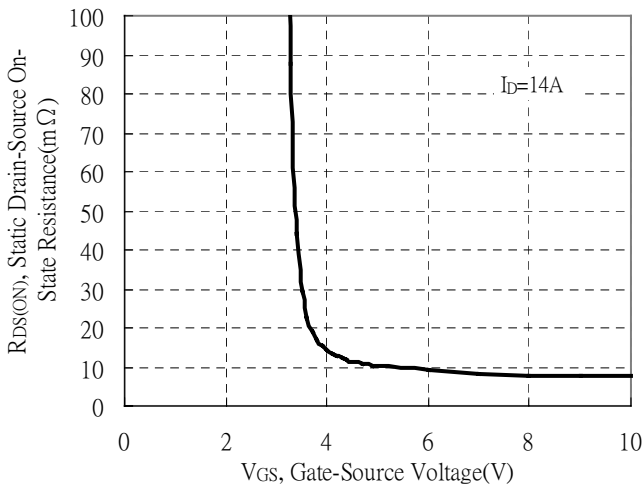
Static Drain-Source On-State resistance vs Drain Current



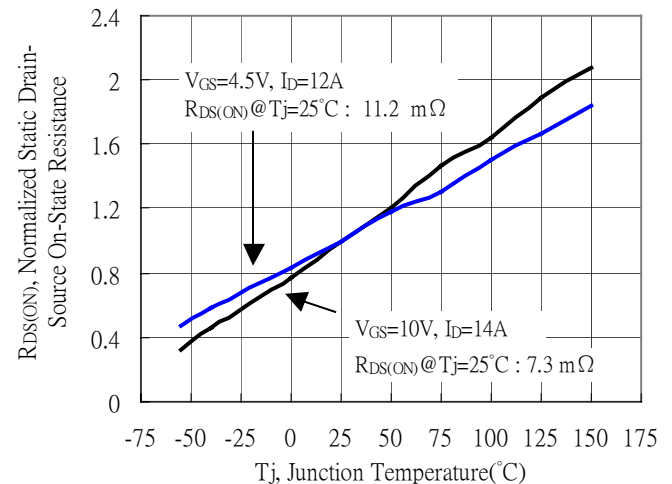
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

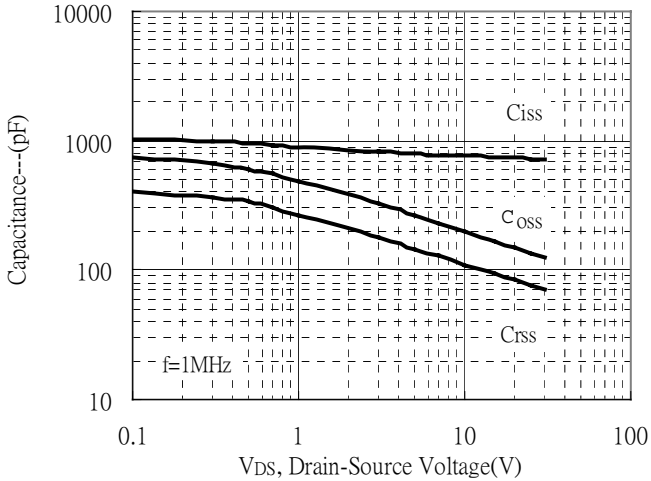


Drain-Source On-State Resistance vs Junction Temperature

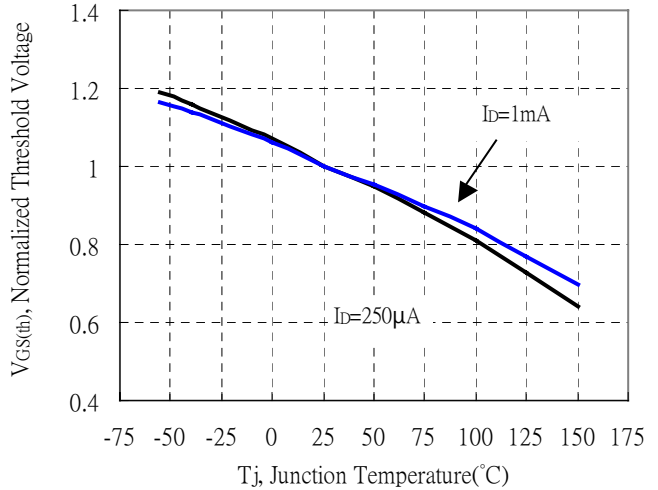


Typical Characteristics(Cont.)

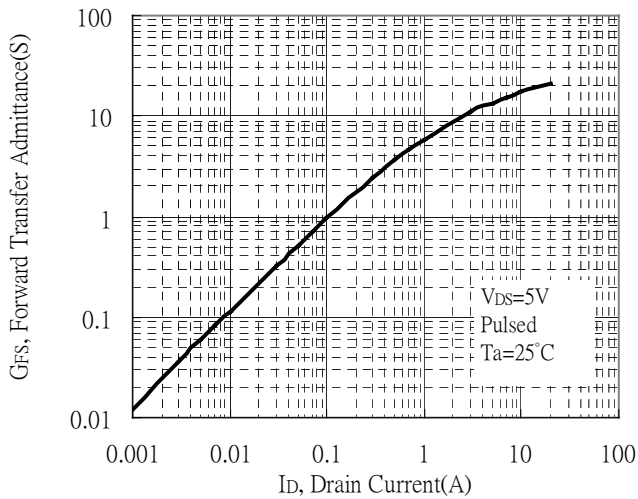
Capacitance vs Drain-to-Source Voltage



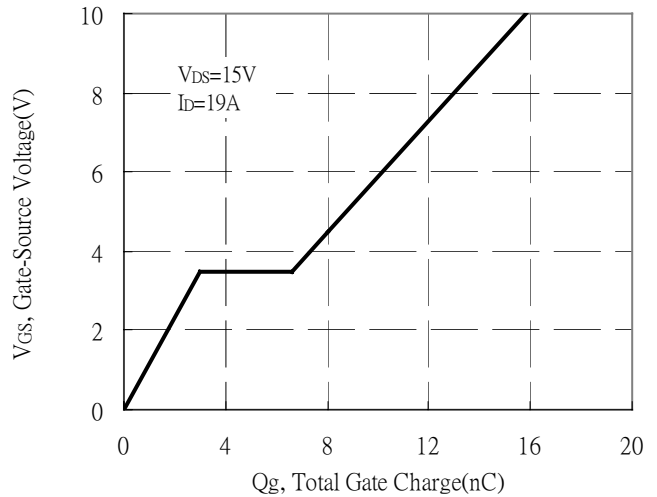
Threshold Voltage vs Junction Temperature



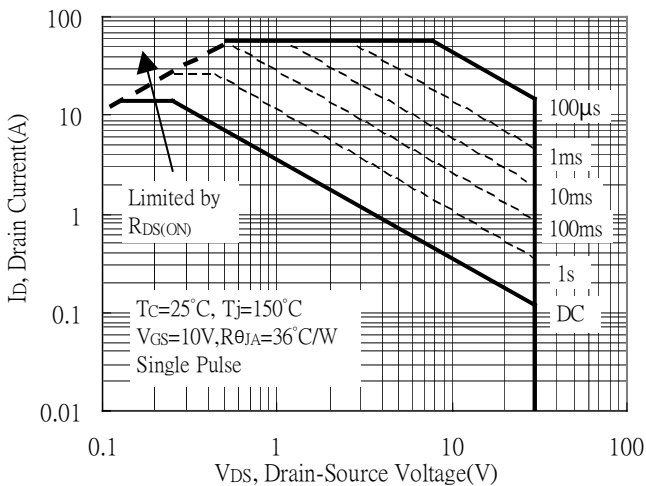
Forward Transfer Admittance vs Drain Current



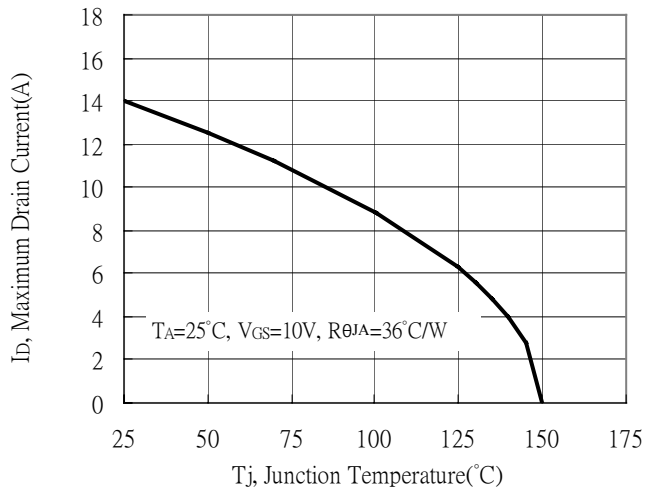
Gate Charge Characteristics



Maximum Safe Operating Area

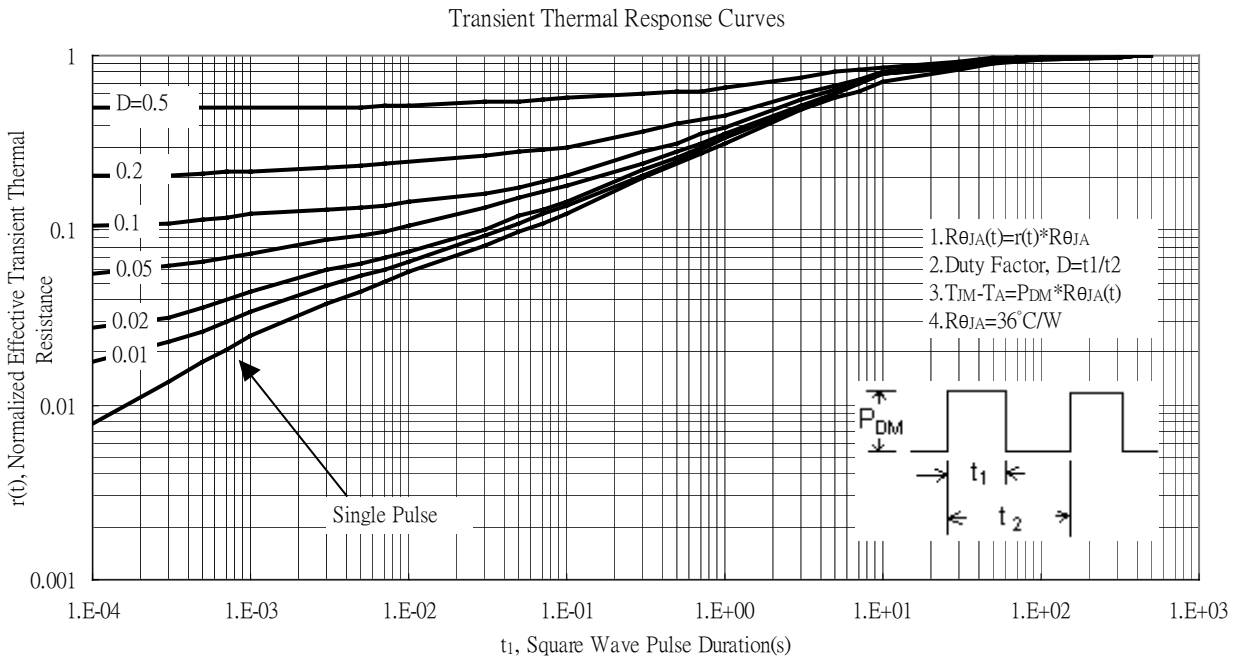
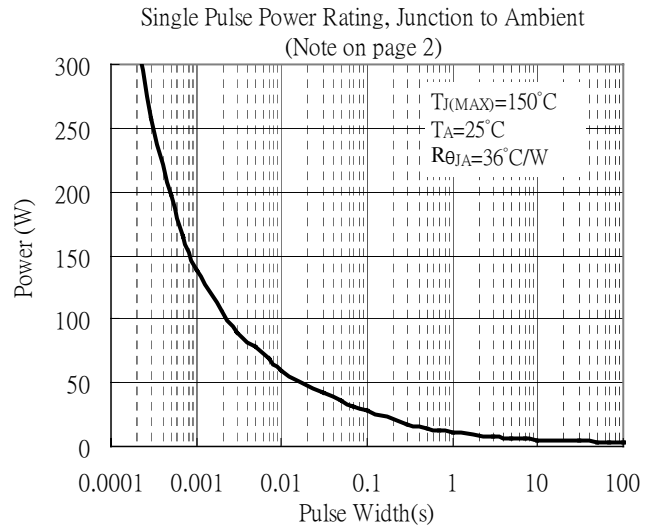
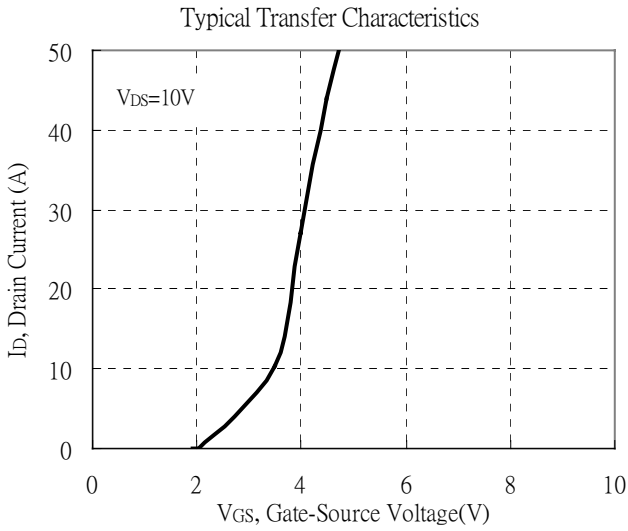


Maximum Drain Current vs Junction Temperature

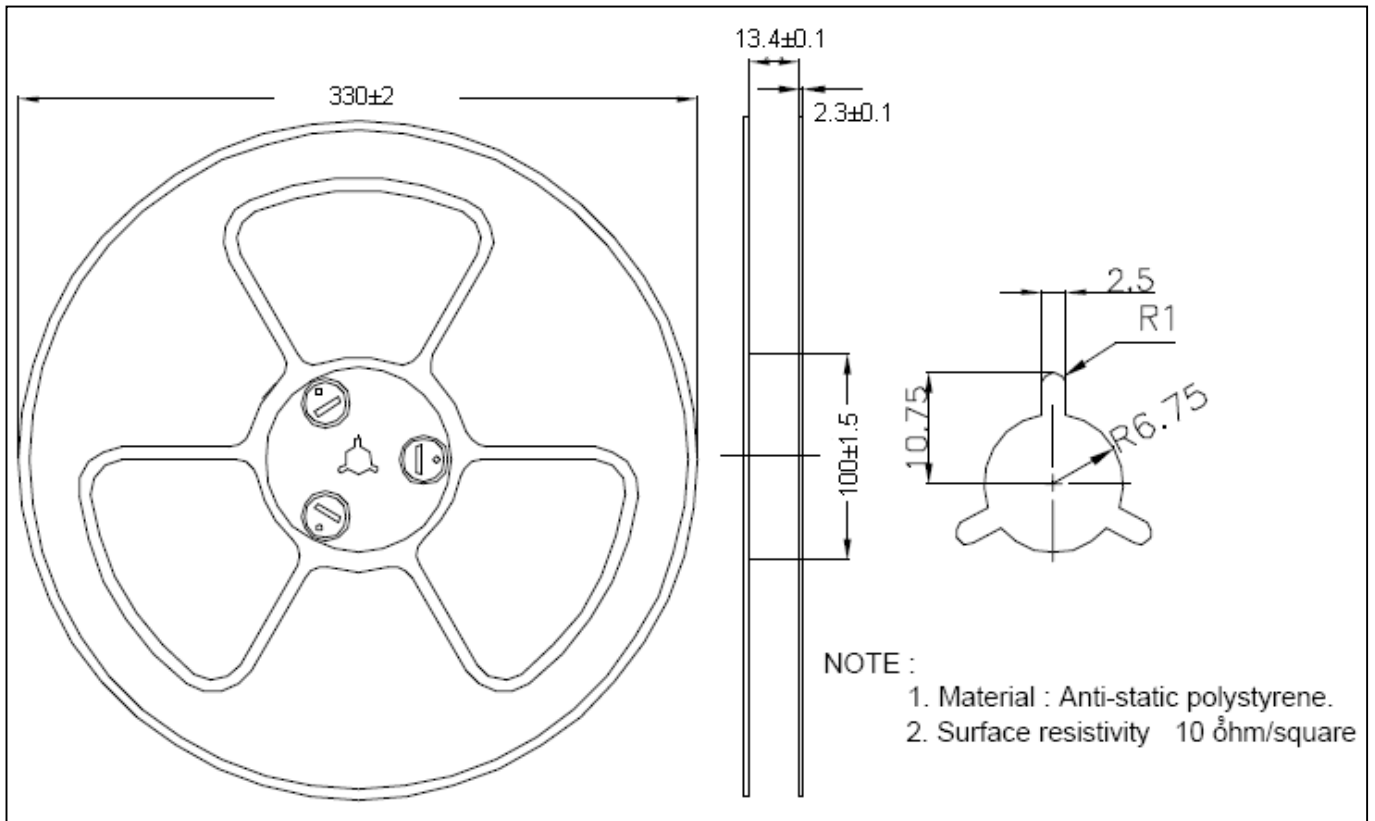




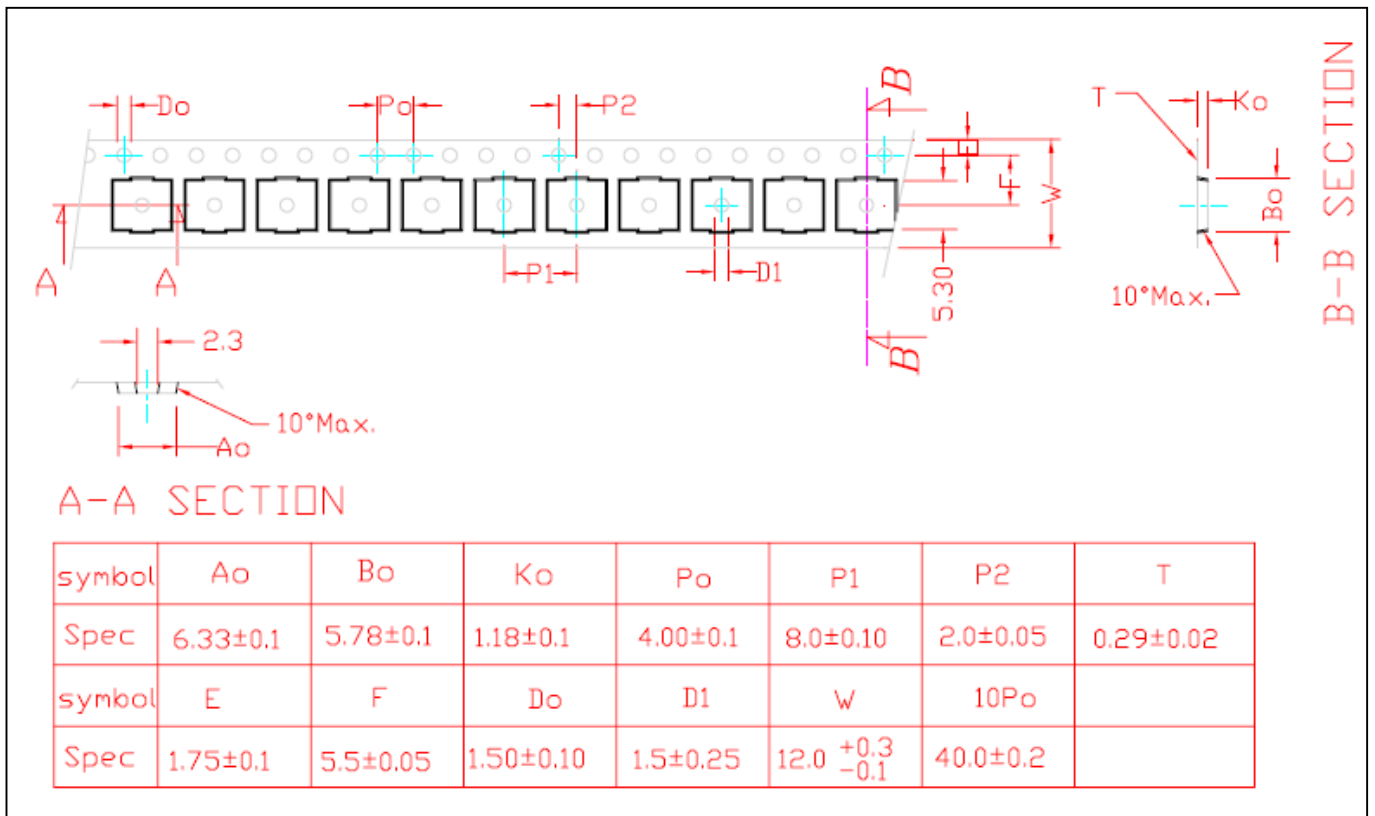
Typical Characteristics(Cont.)



Reel Dimension



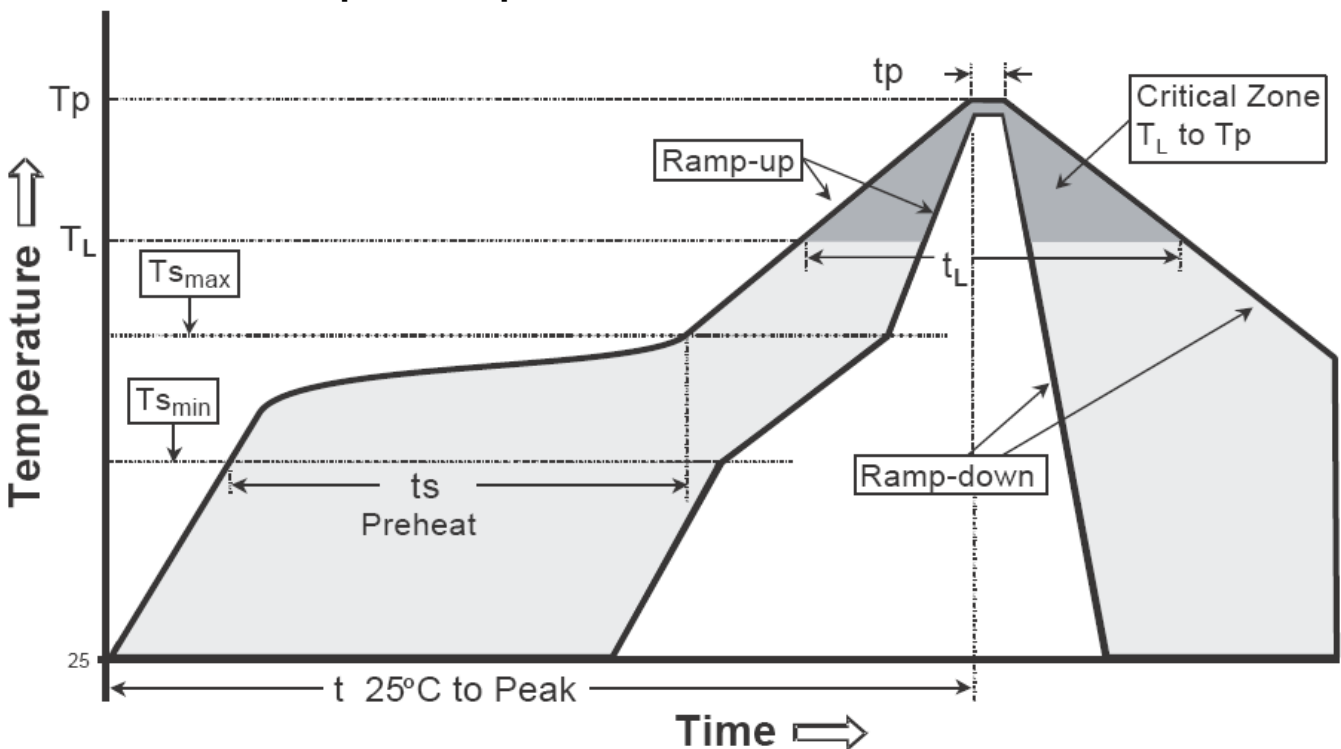
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

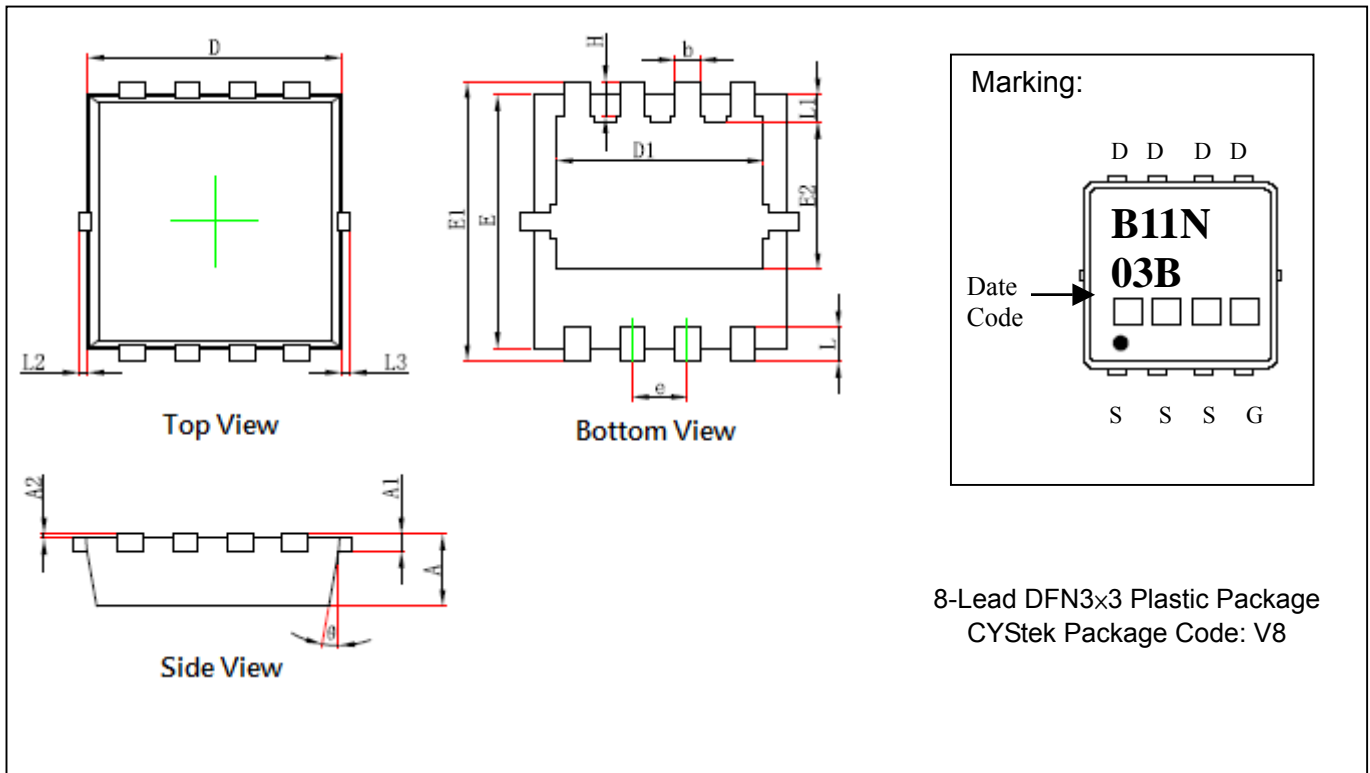
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

DFN3x3 Dimension



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.026	0.033	0.650	0.850	b	0.008	0.016	0.200	0.400
A1	0.006	REF	0.152	REF	e	0.022	0.030	0.550	0.750
A2	0.000	0.002	0.000	0.050	L	0.012	0.020	0.300	0.500
D	0.114	0.122	2.900	3.100	L1	0.007	0.019	0.180	0.480
D1	0.091	0.102	2.300	2.600	L2	0.000	0.004	0.000	0.100
E	0.114	0.122	2.900	3.100	L3	0.000	0.004	0.000	0.100
E1	0.124	0.136	3.150	3.450	H	0.012	0.020	0.315	0.515
E2	0.060	0.076	1.535	1.935	θ	9°	13°	9°	13°

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.