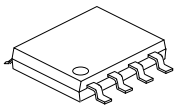
U74AHC1G74

CMOS IC

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET



SOP-8

■ DESCRIPTION

The **UTC U74AHC1G74** is a single positive-edge-triggered D-type flip-flop.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval,data at the D input can be changed without affecting the levels at the outputs.

■ FEATURES

* Operation voltage range: 2 ~ 5.5V
* Max t_{Pd} of 7.3 ns at 5 V
* Low static power consumption; I_{CC}=2μA (Max.)
* ±8mA output drive at 5 V

■ ORDERING INFORMATION

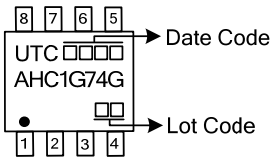
Ordering Number	Package	Packing
U74AHC1G74G-S08-R	SOP-8	Tape Reel

U74AHC1G74G-S08-R

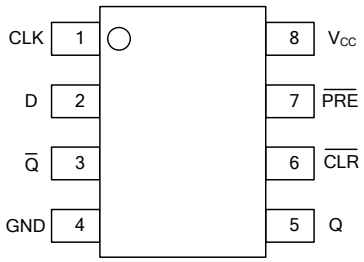
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S08: SOP-8
(3) G: Halogen Free and Lead Free

■ MARKING



■ PIN CONFIGURATION

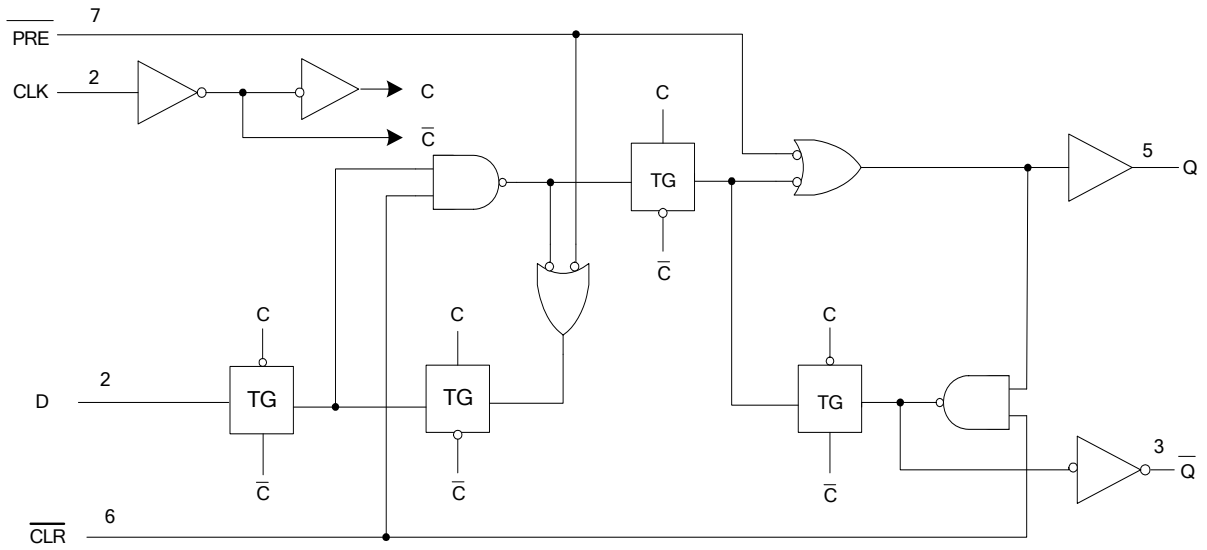


■ FUNCTION TABLE (each gate)

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note)	H (Note)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

Note: This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage	V_{IN}		-0.5 ~ +7.0	V
Output Voltage	V_{OUT}		-0.5 ~ V_{CC} +0.5	V
Continuous V_{CC} or GND Current	I_{CC}		±50	mA
Continuous Output Current	I_{OUT}	-0.5V<V_{OUT}<V_{CC}+0.5V	±25	mA
Input Clamp Current	I_{IK}	V_{IN}< -0.5	-20	mA
Output Clamp Current	I_{OK}	V_{OUT}< -0.5 or V_{OUT}>V_{CC}+0.5V (Note 2)	±20	mA
Storage Temperature Range	T_{STG}		-65 ~ + 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	2.0	5.0	5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
Operating Temperature	T_A		-40		+85	°C
Input Transition Rise or Fall Rate	Δt/Δv	V_{CC}=3.3 ± 0.3V			100	ns/V
		V_{CC}=5.0 ± 0.5V			20	ns/V

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=2.0V		1.5			V
		V_{CC}=3.0V		2.1			V
		V_{CC}=5.5V		3.85			V
Low-level Input Voltage	V_{IL}	V_{CC}=2.0V				0.5	V
		V_{CC}=3.0V				0.9	V
		V_{CC}=5.5V				1.65	V
High-level output voltage (all outputs)	V_{OH}	V_{CC}=2.0V	V_{IN}=V_{IH} or V_{IL}, I_{OH}=-50μA	1.9	2.0		V
		V_{CC}=3.0V		2.9	3.0		V
		V_{CC}=5.5V		4.4	4.5		V
High-Level Output Voltage		V_{CC}=3.0V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=-4.0mA		2.58			V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=-8.0mA		3.94			V
Low-level output voltage (all outputs)	V_{OL}	V_{CC}=2.0V	V_{IN}=V_{IH} or V_{IL}, I_{OH}=50μA			0.1	V
		V_{CC}=3.0V				0.1	V
		V_{CC}=5.5V				0.1	V
Low-Level Output Voltage		V_{CC}=3.0V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=4.0mA				0.36	V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=8.0mA				0.36	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}=V_{CC} or GND				±0.1	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0				2	μA
Input Capacitance	C_{IN}	V_{IN}=V_{CC} or GND			2	10	pF

■ SWITCHING CHARACTERISTICS (GND=0V, $t_r = t_f \leq 3.0$ns, T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Minimum Frequency Response	f_{Max}	C_L=15pF	V_{CC}=3.0V ~ 3.6V	80	125		MHz
			V_{CC}=4.5V ~5.5V	130	170		MHz
		C_L=50pF	V_{CC}=3.0V ~ 3.6V	50	75		MHz
			V_{CC}=4.5V ~5.5V	90	115		MHz
Propagation delay from input ($\overline{PRE}$ or $\overline{CLR}$) to output (Q or $\overline{Q}$)	t_{PLH} / t_{PHL}	C_L=15pF	V_{CC}=3.0V ~ 3.6V		7.6	12.3	ns
			V_{CC}=4.5V ~ 5.5V		4.8	7.7	ns
		C_L=50pF	V_{CC}=3.0V ~ 3.6V		10.1	15.8	ns
			V_{CC}=4.5V ~ 5.5V		6.3	9.7	ns
Propagation delay from input (CLK) to output(Q or $\overline{Q}$)	t_{PLH} / t_{PHL}	C_L=15pF	V_{CC}=3.0V ~ 3.6V		6.7	11.9	ns
			V_{CC}=4.5V ~ 5.5V		4.6	7.3	ns
		C_L=50pF	V_{CC}=3.0V ~ 3.6V		9.2	15.4	ns
			V_{CC}=4.5V ~ 5.5V		6.1	9.3	ns

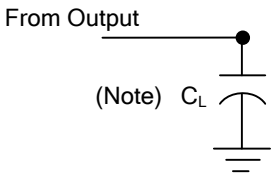
■ TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pulse duration	t_w	V_{CC}=3.0V ~ 3.6V	6			ns
		V_{CC}=4.5V ~ 5.5V	5			ns
Setup time before CLK↑ from Data to $\overline{PRE}$ or $\overline{CLR}$ inactive	t_{su}	V_{CC}=3.0V ~ 3.6V	6			ns
		V_{CC}=4.5V ~ 5.5V	5			ns
Hold time, data after CLK↑	t_h	V_{CC}=3.0V ~ 3.6V	0.5			ns
		V_{CC}=4.5V ~ 5.5V	0.5			ns

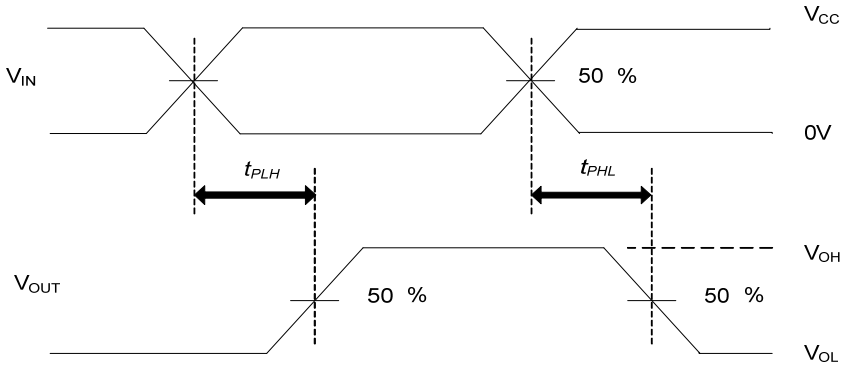
■ OPERATING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	C_L=50pF, f=1MHz		32		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT



PROPAGATION DELAY TIMES

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, Z_O = 50Ω, t_r ≤3ns, t_f ≤3ns.