KSZ8081RNA/RND

10BASE-T/100BASE-TX PHY with RMII Support

Features

- Single-Chip 10BASE-T/100BASE-TX IEEE 802.3 Compliant Ethernet Transceiver
- RMII v1.2 Interface Support with a 50 MHz Reference Clock Output to MAC, and an Option to Input a 50 MHz Reference Clock
- RMII Back-to-Back Mode Support for a 100 Mbps Copper Repeater
- MDC/MDIO Management Interface for PHY Register Configuration
- Programmable Interrupt Output
- LED Outputs for Link and Activity Status Indication
- On-Chip Termination Resistors for the Differential Pairs
- Baseline Wander Correction
- HP Auto MDI/MDI-X to Reliably Detect and Correct Straight-Through and Crossover Cable Connections with Disable and Enable Option
- Auto-Negotiation to Automatically Select the Highest Link-Up Speed (10/100 Mbps) and Duplex (Half/Full)
- Power-Down and Power-Saving Modes
- LinkMD® TDR-Based Cable Diagnostics to Identify Faulty Copper Cabling
- Parametric NAND Tree Support for Fault Detection Between Chip I/Os and the Board
- HBM ESD Rating (6 kV)
- Loopback Modes for Diagnostics
- Single 3.3V Power Supply with V_{DD} I/O Options for 1.8V, 2.5V, or 3.3V
- Built-In 1.2V Regulator for Core
- Available in 24-pin 4 mm x 4 mm QFN Package

Target Applications

- Game Consoles
- IP Phones
- IP Set-Top Boxes
- IP TVs
- LOM
- Printers

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1.0 INTRODUCTION

1.1 General Description

The KSZ8081RNA/RND is a single-supply 10BASE-T/100BASE-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081RNA/RND is a highly-integrated PHY solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low-noise regulator to supply the 1.2V core, and by offering 1.8/2.5/3.3V digital I/O interface support.

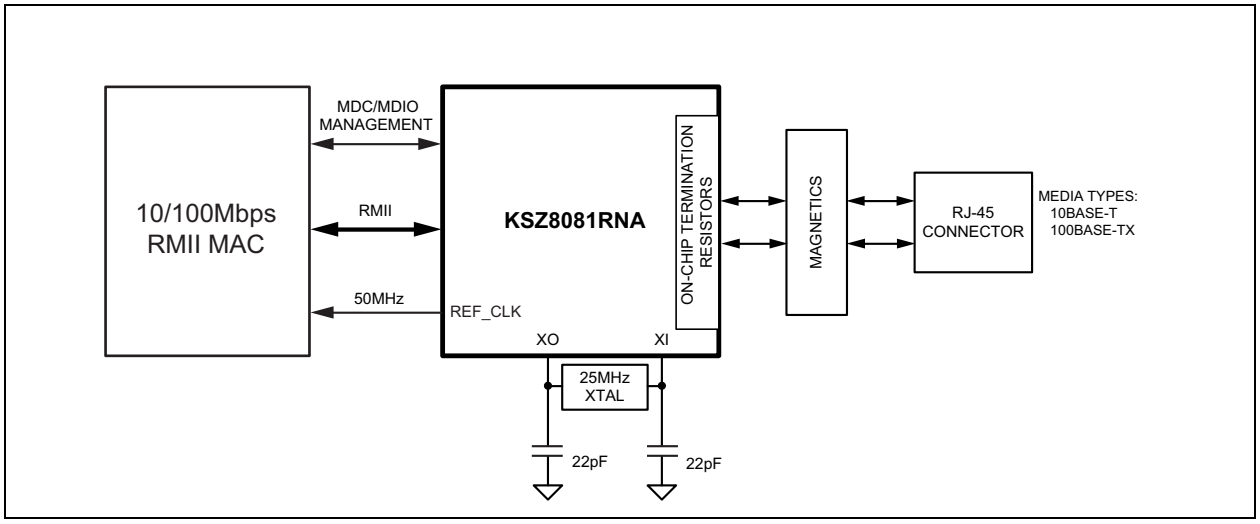
The KSZ8081RNA/RND offers the Reduced Media Independent Interface (RMII) for direct connection to RMII-compliant MACs in Ethernet processors and switches.

As the power-up default, the KSZ8081RNA/RND uses a 25 MHz crystal to generate all required clocks, including the 50 MHz RMII reference clock output for the MAC. The KSZ8081RND is the version that takes in the 50 MHz RMII reference clock as the power-up default.

To facilitate system bring-up and debugging in production testing and in product deployment, parametric NAND tree support enables fault detection between KSZ8081RNA/RND I/Os and the board. LinkMD® TDR-based cable diagnostics identify faulty copper cabling.

The KSZ8081RNA and KSZ8081RND are available in 24-pin, lead-free QFN packages.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 24-QFN PIN ASSIGNMENT (TOP VIEW)

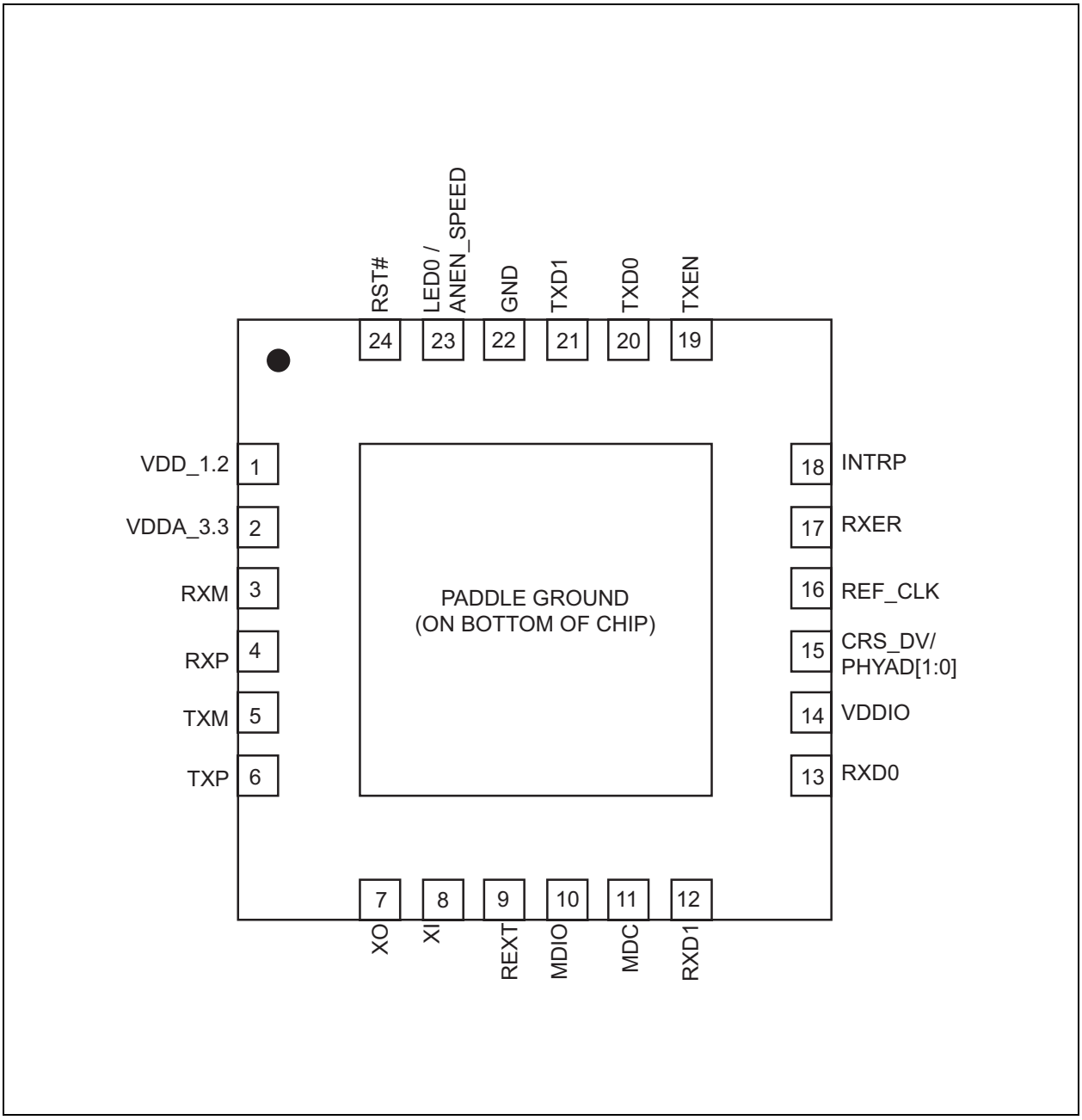


TABLE 2-1: SIGNALS - KSZ8081RNA/RND

Pin Number	Pin Name	Type Note 2-1	Description
1	VDD_1.2	P	1.2V Core V_{DD} (power supplied by KSZ8081RNA/KSZ8081RND). Decouple with 2.2 µF and 0.1 µF capacitors to ground.
2	VDDA_3.3	P	3.3V Analog V_{DD}.
3	RXM	I/O	Physical Receive or Transmit Signal (– differential).
4	RXP	I/O	Physical Receive or Transmit Signal (+ differential).
5	TXM	I/O	Physical Transmit or Receive Signal (– differential).
6	TXP	I/O	Physical Transmit or Receive Signal (+ differential).
7	XO	O	Crystal Feedback for 25 MHz Crystal. This pin is a no connect if an oscillator or external clock source is used.
8	XI	I	RMII – 25 MHz Mode: 25 MHz ±50 ppm Crystal/Oscillator/External Clock Input RMII – 50 MHz Mode: 50 MHz ±50 ppm Oscillator/External Clock Input For unmanaged mode (power-up default setting): – KSZ8081RNA takes in the 25 MHz crystal/clock on this pin. – KSZ8081RND takes in the 50 MHz clock on this pin. After power-up, both the KSZ8081RNA and KSZ8081RND can be programmed to either the 25 MHz mode or 50 MHz mode using PHY Register 1Fh Bit [7]. See also REF_CLK (Pin 16).
9	REXT	I	Set PHY Transmit Output Current. Connect a 6.49 kΩ resistor to ground on this pin.
10	MDIO	Ipu/ Opu	Management Interface (MII) Data I/O. This pin has a weak pull-up, is open-drain, and requires an external 1.0 kΩ pull-up resistor.
11	MDC	Ipu	Management Interface (MII) Clock Input. This clock pin is synchronous to the MDIO data pin.
12	RXD1	Ipd/O	RMII Receive Data Output[1] (Note 2-2).
13	RXD0	Ipu/O	RMII Receive Data Output[0] (Note 2-2).
14	VDDIO	P	3.3V, 2.5V, or 1.8V Digital V_{DD}.
15	CRS_DV/ PHYAD[1:0]	Ipd/O	RMII Mode: Carrier Sense/Receive Data Valid Output. Config. Mode: The pull-up/pull-down value is latched as PHYAD[1:0] at the de-assertion of reset. See the Strapping Options section for details.

TABLE 2-1: SIGNALS - KSZ8081RNA/RND (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th>Description</th></tr>
<tr><td>16</td><td>REF_CLK</td><td>Ipd/O</td><td>RMII – 25 MHz Mode: This pin provides the 50 MHz RMII reference clock output to the MAC.
RMII – 50 MHz Mode: This pin is a no connect.
For unmanaged mode (power-up default setting),
– KSZ8081RNA is in RMII – 25 MHz mode and outputs the 50 MHz RMII reference clock on this pin.
– KSZ8081RND is in RMII – 50 MHz mode and does not use this pin.

After power-up, both KSZ8081RNA and KSZ8081RND can be programmed to either 25 MHz mode or 50 MHz mode using PHY Register 1Fh Bit [7].
See also XI (Pin 8).</td></tr>
<tr><td>17</td><td>RXER</td><td>Ipd/O</td><td>RMII Receive Error Output.
At the de-assertion of reset, this pin needs to latch in a pull-down value for normal operation. If MAC side pulls this pin high, see Register 16h, Bit [15] for solution. It is better having an external pull-down resistor to avoid MAC side pulls this pin high.</td></tr>
<tr><td>18</td><td>INTRP</td><td>Ipu/ Opu</td><td>Interrupt Output: Programmable interrupt output. This pin has a weak pull-up, is open drain, and requires an external 1.0 kΩ pull-up resistor.</td></tr>
<tr><td>19</td><td>TXEN</td><td>I</td><td>RMII Transmit Enable Input.</td></tr>
<tr><td>20</td><td>TXD0</td><td>I</td><td>RMII Transmit Data Input [0] (Note 2-3).</td></tr>
<tr><td>21</td><td>TXD1</td><td>I/O</td><td>RMII Transmit Data Input [1] (Note 2-3).
NAND Tree Mode: NAND Tree output pin.</td></tr>
<tr><td>22</td><td>GND</td><td>GND</td><td>Ground.</td></tr>
<tr><td rowspan="11">23</td><td rowspan="11">LED0/
ANEN_SPEED</td><td rowspan="11">Ipu/O</td><td>LED Output: Programmable LED0 Output.
Config. Mode: Latched as auto-negotiation enable (Register 0h, Bit [12]) and Speed (Register 0h, Bit [13]) at the de-assertion of reset. See the Strapping Options section for details.
The LED0 pin is programmable using Register 1Fh bits [5:4], and is defined as follows:</td></tr>
<tr><td>LED Mode = [00]</td></tr>
<tr><td><table><tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No Link</td><td>High</td><td>OFF</td></tr><tr><td>Link</td><td>Low</td><td>ON</td></tr><tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr></table></td></tr>
<tr><td>LED Mode = [01]</td></tr>
<tr><td><table><tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No Link</td><td>High</td><td>OFF</td></tr><tr><td>Link</td><td>Low</td><td>ON</td></tr></table></td></tr>
<tr><td>LED Mode = [10], [11]: Reserved</td></tr>
<tr><td>24</td><td>RST#</td><td>Ipu</td><td>Chip Reset (active-low).</td></tr>
</table>

TABLE 2-1: SIGNALS - KSZ8081RNA/RND (CONTINUED)

Pin Number	Pin Name	Type Note 2-1	Description
Paddle	GND	GND	Ground.

Note 2-1 P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value).
Ipu/O = Input with internal pull-up (see Section 6.0, "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipu/Opu = Input with internal pull-up (see Electrical Characteristics for value) and output with internal pull-up (see Electrical Characteristics for value).

Note 2-2 RMII RX Mode: The RXD[1:0] bits are synchronous with the 50 MHz RMII Reference Clock. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent by the PHY to the MAC.

Note 2-3 RMII TX Mode: The TXD[1:0] bits are synchronous with the 50 MHz RMII Reference Clock. For each clock period in which TXEN is asserted, two bits of data are received by the PHY from the MAC.

The PHYAD[1:0] strap-in pin is latched at the de-assertion of reset. In some systems, the RMII MAC receive input pins may drive high/low during power-up or reset, and consequently cause the PHYAD[1:0] strap-in pin, a shared pin with the RMII CRS_DV signal, to be latched to the unintended high/low state. In this case an external pull-up (4.7 kΩ) or pull-down (1.0 kΩ) should be added on the PHYAD[1:0] strap-in pin to ensure that the intended value is strapped-in correctly.

TABLE 2-2: STRAP-IN OPTIONS - KSZ8081RNA/RND

Pin Number	Pin Name	Type Note 2-4	Description
15	PHYAD[1:0]	Ipd/O	The PHY Address is latched at the de-assertion of reset and is configurable to either one of the following two values: Pull-up = PHY Address is set to 00011b (0x3h) Pull-down (default) = PHY Address is set to 00000b (0x0h) PHY Address Bits [4:2] are set to 000 by default.
23	ANEN_SPEED	Ipu/O	Auto-Negotiation Enable and SPEED Mode Pull-up (default) = Enable Auto-Negotiation and set 100 Mbps Speed Pull-down = Disable Auto-Negotiation and set 10 Mbps Speed At the de-assertion of reset, this pin value is latched into Register 0h Bit [12] for Auto-negotiation enable/disable, Register 0h Bit [13] for the speed select, and Register 4h (Auto-Negotiation Advertisement) for the speed capability support.

Note 2-4 Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8081RNA is an integrated, single 3.3V supply, fast Ethernet transceiver. It is fully compliant with the IEEE 802.3 Specification, and reduces board cost and simplifies board layout by using on-chip termination resistors for the two differential pairs and by integrating the regulator to supply the 1.2V core.

On the copper media side, the KSZ8081RNA supports 10BASE-T and 100BASE-TX for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable, and HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8081RNA offers the Reduced Media Independent Interface (RMII) for direct connection with RMII-compliant Ethernet MAC processors and switches

The MII management bus option gives the MAC processor complete access to the KSZ8081RNA control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

As the power-up default, the KSZ8081RNA uses a 25 MHz crystal to generate all required clocks, including the 50 MHz RMII reference clock output for the MAC. The KSZ8081RND version uses the 50 MHz RMII reference clock as the power-up default.

The KSZ8081RNA/RND is used to refer to both KSZ8081RNA and KSZ8081RND versions in this data sheet.

3.1 10BASE-T/100BASE-TX Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 6.49 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data-conversion circuit converts MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal to NRZ format. This signal is sent through the de-scrambler, then the 4B/5B decoder. Finally, the NRZ serial data is converted to MII format and provided as the input data to the MAC.

3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The scrambler spreads the power spectrum of the transmitted signal to reduce electromagnetic interference (EMI) and baseline wander. The de-scrambler recovers the scrambled signal.

3.1.4 10BASE-T TRANSMIT

The 10BASE-T drivers are incorporated with the 100BASE-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10BASE-T signals with typical amplitude of 2.5V peak. The 10BASE-T signals have harmonic contents that are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV, or with short pulse widths, to prevent noise at the RXP and RXM inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8081RNA/RND decodes a data frame. The receive clock is kept active during idle periods between data receptions.

3.1.6 PLL CLOCK SYNTHESIZER

The KSZ8081RNA/RND in RMII – 25 MHz Clock mode generates all internal clocks and all external clocks for system timing from an external 25 MHz crystal, oscillator, or reference clock. For the KSZ8081RNA/RND in RMII – 50 MHz clock mode, these clocks are generated from an external 50 MHz oscillator or system clock.

3.1.7 AUTO-NEGOTIATION

The KSZ8081RNA/RND conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

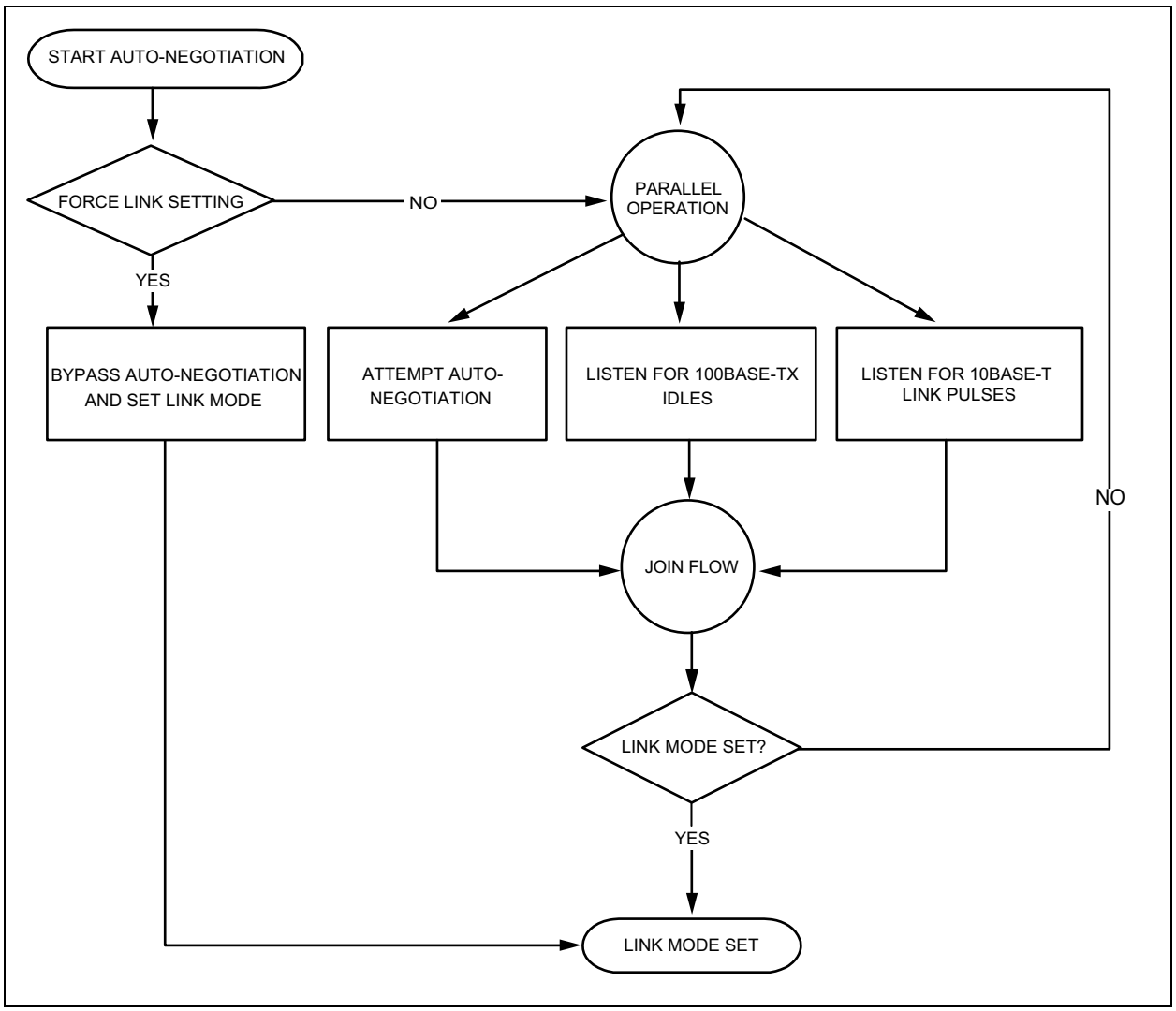
If auto-negotiation is not supported or the KSZ8081RNA/RND link partner is forced to bypass auto-negotiation, then the KSZ8081RNA/RND sets its operating mode by observing the signal at its receiver. This is known as parallel detection, which allows the KSZ8081RNA/RND to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

Auto-negotiation is enabled by either hardware pin strapping (ANEN_SPEED, Pin 23) or software (Register 0h, Bit [12]).

By default, auto-negotiation is enabled after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled by Register 0h, Bit [12]. If auto-negotiation is disabled, the speed is set by Register 0h, Bit [13], and the duplex is set by Register 0h, Bit [8].

The auto-negotiation link-up process is shown in Figure 3-1.

FIGURE 3-1: AUTO-NEGOTIATION FLOW CHART



3.2 RMII Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Pin count is 8 pins (3 pins for data transmission, 4 pins for data reception, and 1 pin for the 50 MHz reference clock).
- 10 Mbps and 100 Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 2 bits wide, a dibit.

3.2.1 RMII SIGNAL DEFINITION

Table 3-1 describes the RMII signals. Refer to RMII Specification v1.2 for detailed information.

TABLE 3-1: RMII SIGNAL DEFINITION

RMII Signal Name	Direction with Respect to PHY, KSZ8081 Signal	Direction with Respect to MAC	Description
REF_CLK	Output (25 MHz Clock Mode)/ No Connect (50 MHz Clock Mode)	Input/ Input or No Connect	Synchronous 50 MHz reference clock for receive, transmit, and control interface
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data[1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data[1:0]
RXER	Output	Input or Not Required	Receive Error

3.2.1.1 Reference Clock (REF_CLK)

REF_CLK is a continuous 50 MHz clock that provides the timing reference for TXEN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

For RMII – 25 MHz Clock Mode, the KSZ8081RNA/RND generates and outputs the 50 MHz RMII REF_CLK to the MAC at REF_CLK (Pin 16).

For RMII – 50 MHz Clock Mode, the KSZ8081RNA/RND takes in the 50 MHz RMII REF_CLK from the MAC or system board at XI (Pin 8) and leaves the REF_CLK (Pin 16) as no connect.

3.2.1.2 Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting dibits on TXD[1:0] for transmission. It is asserted synchronously with the first dibit of the preamble and remains asserted while all dibits to be transmitted are presented on the RMII. It is negated before the first REF_CLK following the final dibit of a frame.

TXEN transitions synchronously with respect to REF_CLK.

3.2.1.3 Transmit Data[1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TXEN is asserted, the PHY accepts TXD[1:0] for transmission.

TXD[1:0] is 00 to indicate idle when TXEN is de-asserted. The PHY ignores values other than 00 on TXD[1:0] while TXEN is de-asserted.

3.2.1.4 Carrier Sense/Receive Data Valid (CRS_DV)

The PHY asserts CRS_DV when the receive medium is non-idle. It is asserted asynchronously when a carrier is detected. This happens when squelch is passed in 10 Mbps mode, and when two non-contiguous 0s in 10 bits are detected in 100 Mbps mode. Loss of carrier results in the de-assertion of CRS_DV.

While carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered dibit of the frame through the final recovered dibit. It is negated before the first REF_CLK that follows the final dibit. The data on RXD[1:0] is considered valid after CRS_DV is asserted. However, because the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is 00 until receive signals are properly decoded.

3.2.1.5 Receive Data[1:0] (RXD[1:0])

RXD[1:0] transitions synchronously with respect to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY.

RXD[1:0] is 00 to indicate idle when CRS_DV is de-asserted. The MAC ignores values other than 00 on RXD[1:0] while CRS_DV is de-asserted.

3.2.1.6 Receive Error (RXER)

RXER is asserted for one or more REF_CLK periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame being transferred from the PHY.

RXER transitions synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RXER has no effect on the MAC.

3.2.1.7 Collision Detection (COL)

The MAC regenerates the COL signal of the MII from TXEN and CRS_DV.

3.2.2 RMII SIGNAL DIAGRAM – 25/50 MHZ CLOCK MODE

The KSZ8081RNA/RND RMII pin connections to the MAC for 25 MHz clock mode are shown in Figure 3-2. The connections for 50 MHz clock mode are shown in Figure 3-3.

3.2.2.1 RMII – 25 MHz Clock Mode

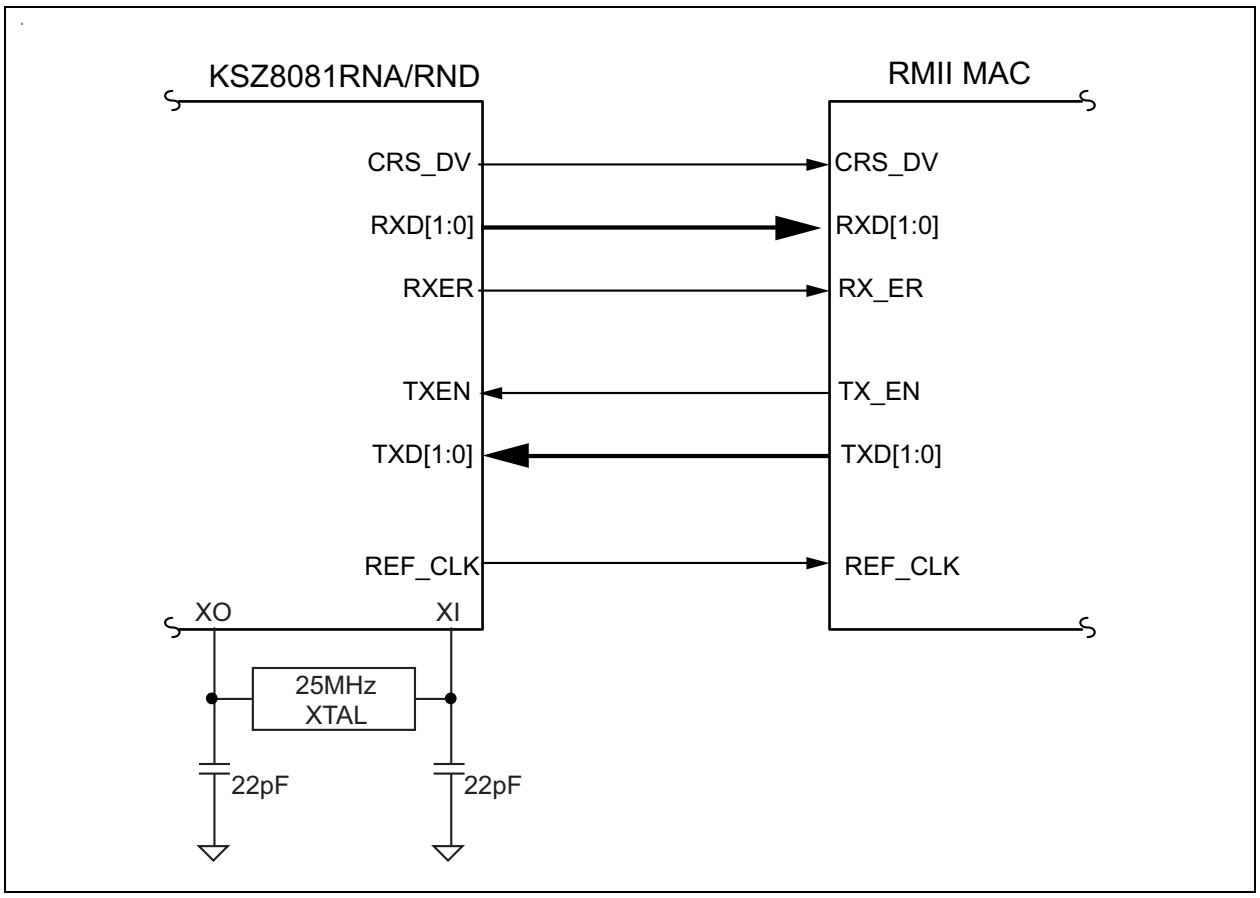
The KSZ8081RNA is configured to RMII – 25 MHz clock mode after it is powered up or hardware reset with the following:

- A 25 MHz crystal connected to XI, XO (Pins 8, 7), or an external 25 MHz clock source (oscillator) connected to XI

The KSZ8081RND can optionally be configured to RMII – 25 MHz clock mode after it is powered up or hardware reset and software programmed with the following:

- A 25 MHz crystal connected to XI, XO (Pins 8, 7), or an external 25 MHz clock source (oscillator) connected to XI
- Register 1Fh, Bit [7] programmed to ‘1’ to select RMII – 25 MHz clock mode

FIGURE 3-2: KSZ8081RNA/RND RMII INTERFACE (RMII - 25 MHZ CLOCK MODE)



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3.2.2.2 RMII – 50 MHz Clock Mode

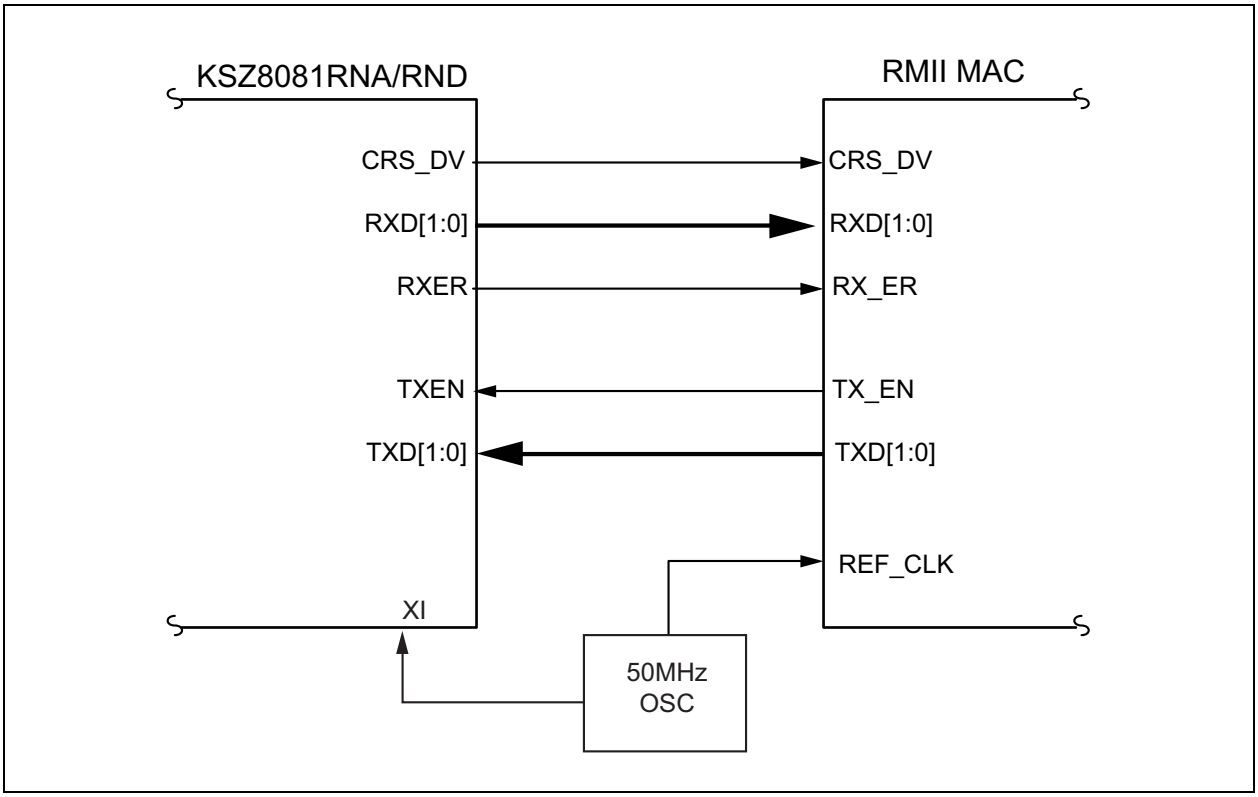
The KSZ8081RND is configured to RMII – 50 MHz clock mode after it is powered up or hardware reset with the following:

- An external 50 MHz clock source (oscillator) connected to XI (Pin 8)

The KSZ8081RNA can optionally be configured to RMII – 50 MHz clock mode after it is powered up or hardware reset and software programmed with the following:

- An external 50 MHz clock source (oscillator) connected to XI (Pin 8)
- Register 1Fh, Bit [7] programmed to '1' to select RMII – 50 MHz clock mode

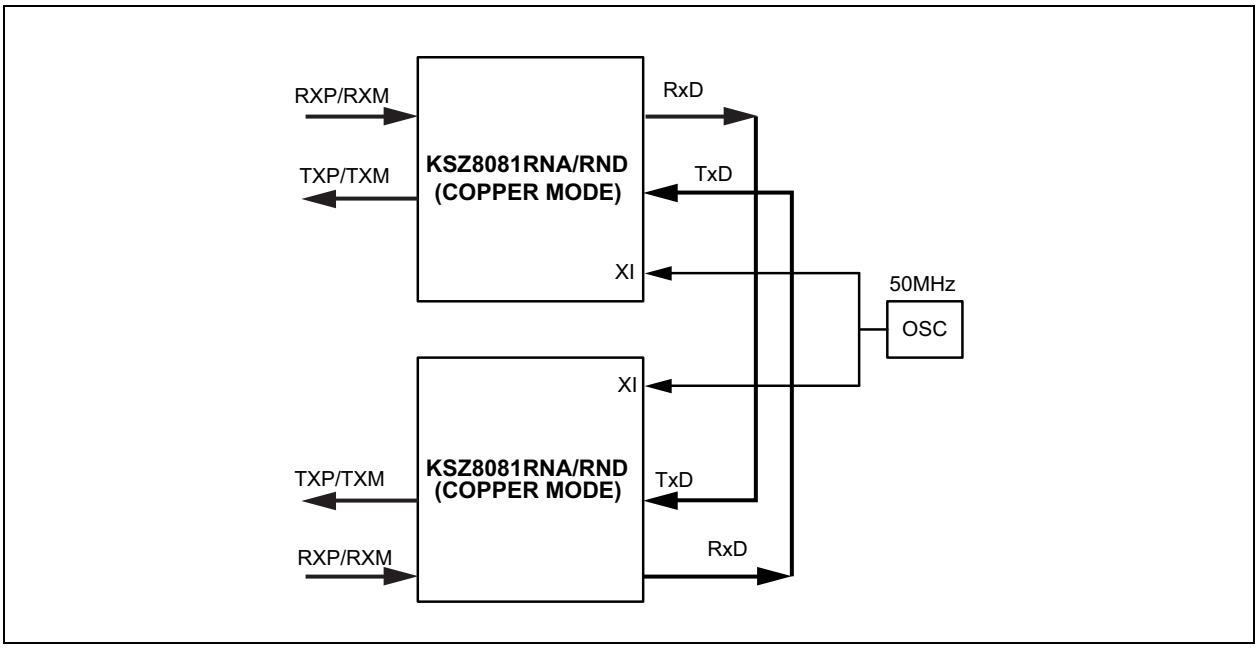
FIGURE 3-3: KSZ8081RNA/RND RMII INTERFACE (RMII - 50 MHZ CLOCK MODE)



3.3 Back-to-Back Mode – 100 Mbps Copper Repeater

Two KSZ8081RNA/RND devices can be connected back-to-back to form a managed 100BASE-TX copper repeater.

FIGURE 3-4: KSZ8081RNA/RND AND KSZ8081RNA/RND RMII BACK-TO-BACK COPPER REPEATER



3.3.1 RMII BACK-TO-BACK MODE

In RMII back-to-back mode, a KSZ8081RNA/RND interfaces with another KSZ8081RNA/RND to provide a 100 Mbps copper repeater solution.

The KSZ8081RNA/RND devices are configured to RMII back-to-back mode after power-up or reset, and software programming, with the following:

- A common 50 MHz reference clock connected to XI (Pin 8)
- Register 1Fh, Bit [7] programmed to ‘1’ to select RMII – 50 MHz clock mode for KSZ8081RNA

KSZ8081RND is set to RMII – 50 MHz clock mode as the default after power up or hardware reset.

- Register 16h, Bits [6] and [1] programmed to ‘1’ and ‘1’, respectively, to enable RMII back-to-back mode.
- RMII signals connected as shown in Table 3-2.

TABLE 3-2: RMII SIGNAL CONNECTION FOR RMII BACK-TO-BACK MODE (100BASE-TX COPPER REPEATER)

KSZ8081RNA/RND (100BASE-TX Copper) [Device 1]			KSZ8081RNA/RND (100BASE-TX Copper) [Device 2]		
Pin Name	**Pin Number**	**Pin Type**	**Pin Name**	**Pin Number**	**Pin Type**
CRS_DV	15	Output	TXEN	19	Input
RXD1	12	Output	TXD1	21	Input
RXD0	13	Output	TXD0	20	Input
TXEN	19	Input	CRS_DV	15	Output
TXD1	21	Input	RXD1	12	Output
TXD0	20	Input	RXD0	13	Output

3.4 MII Management (MIIM) Interface

The KSZ8081RNA/RND supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows an upper-layer device, such as a MAC processor, to monitor and control the state of the KSZ8081RNA/RND. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows the external controller to communicate with one or more PHY devices.
- A set of 16-bit MDIO registers. Registers [0:8] are standard registers, and their functions are defined in the IEEE 802.3 Specification. The additional registers are provided for expanded functionality. See the Register Map section for details.

The KSZ8081RNA/RND supports only two unique PHY addresses. The PHYAD[1:0] strapping pin is used to select either 0h or 3h as the unique PHY address for the KSZ8081RNA/RND device.

PHY address 0h is defined as the broadcast PHY address according to the IEEE 802.3 Specification, and can be used to read/write to a single PHY device, or write to multiple PHY devices simultaneously. For the KSZ8081RNA/RND, PHY address 0h defaults to the broadcast PHY address after power-up, but PHY address 0h can be disabled as the broadcast PHY address using software to assign it as a unique PHY address.

For applications that require two KSZ8081RNA/RND PHYs to share the same MDIO interface with one PHY set to address 0h and the other PHY set to address 3h, use PHY address 0h (defaults to broadcast after power-up) to set both PHYs' Register 16h, Bit [9] to '1' to assign PHY address 0h as a unique (non-broadcast) PHY address.

Table 3-3 shows the MII management frame format for the KSZ8081RNA/RND.

TABLE 3-3: MII MANAGEMENT FRAME FORMAT FOR THE KSZ8081RNA/RND

	Preamble	Start of Frame	Read/ Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	000AA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	000AA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.5 Interrupt (INTRP)

INTRP (Pin 18) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8081RNA/RND PHY register. Bits [15:8] of Register 1Bh are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Bits [7:0] of Register 1Bh are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Register 1Bh.

Bit [9] of Register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ8081RNA/RND control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

3.6 HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the need to decide whether to use a straight cable or a crossover cable between the KSZ8081RNA/RND and its link partner. This feature allows the KSZ8081RNA/RND to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and assigns transmit and receive pairs to the KSZ8081RNA/RND accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a '1' to Register 1Fh, Bit [13]. MDI and MDI-X mode is selected by Register 1Fh, Bit [14] if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Table 3-4 shows how the IEEE 802.3 Standard defines MDI and MDI-X.

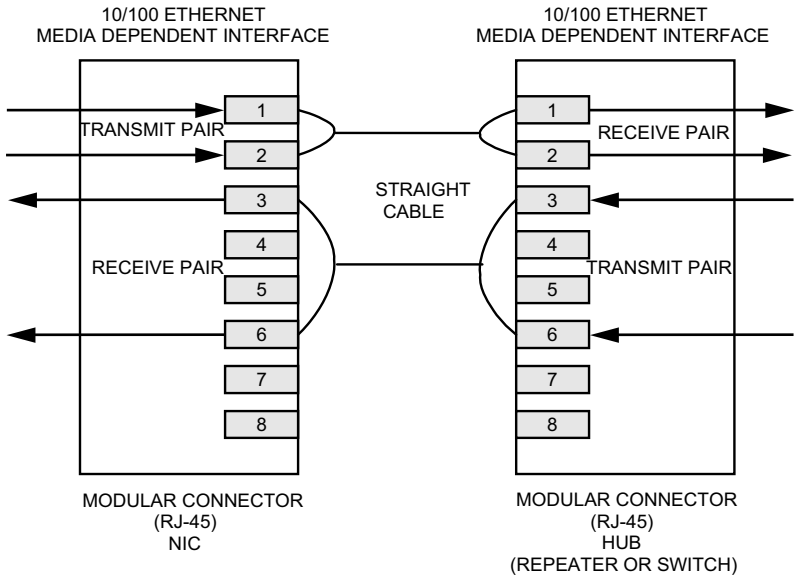
TABLE 3-4: MDI/MDI-X PIN DESCRIPTION

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TX+	1	RX+
2	TX–	2	RX–
3	RX+	3	TX+
6	RX–	6	TX–

3.6.1 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-5 shows a typical straight cable connection between a NIC card (MDI device) and a switch or hub (MDI-X device).

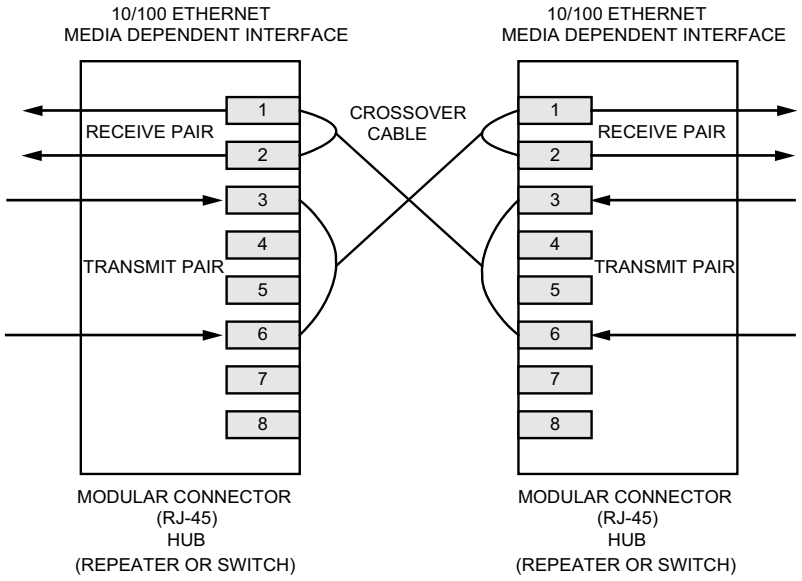
FIGURE 3-5: TYPICAL STRAIGHT CABLE CONNECTION



3.6.2 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-6 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-6: TYPICAL CROSSOVER CABLE CONNECTION



3.7 Loopback Mode

The KSZ8081RNA/RND supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

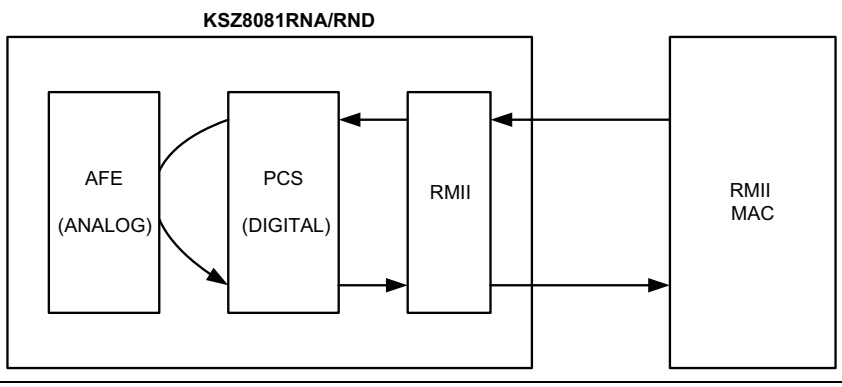
3.7.1 LOCAL (DIGITAL) LOOPBACK

This loopback mode checks the RMII transmit and receive data paths between the KSZ8081RNA/RND and the external MAC, and is supported for both speeds (10/100 Mbps) at full-duplex.

The loopback data path is shown in Figure 3-7.

1. The RMII MAC transmits frames to the KSZ8081RNA/RND.
2. Frames are wrapped around inside the KSZ8081RNA/RND.
3. The KSZ8081RNA/RND transmits frames back to the RMII MAC.
4. Except the frames back to the RMII MAC, the transmit frames also go out from the copper port.

FIGURE 3-7: LOCAL (DIGITAL) LOOPBACK



The following programming action and register settings are used for local loopback mode:

For 10/100 Mbps loopback:

Set Register 0h,

Bit [14] = 1 // Enable local loopback mode

Bit [13] = 0/1 // Select 10 Mbps/100 Mbps speed

Bit [12] = 0 // Disable auto-negotiation

Bit [8] = 1 // Select full-duplex mode

Follow the steps below if you don't want the frames go out from the copper port in the local loopback.

1. Set register 1Fh bit [3] to '1' to disable the transmitter.
2. Run local loopback test as above.
3. Set register 1Fh bit [3] to '0' to enable the transmitter.

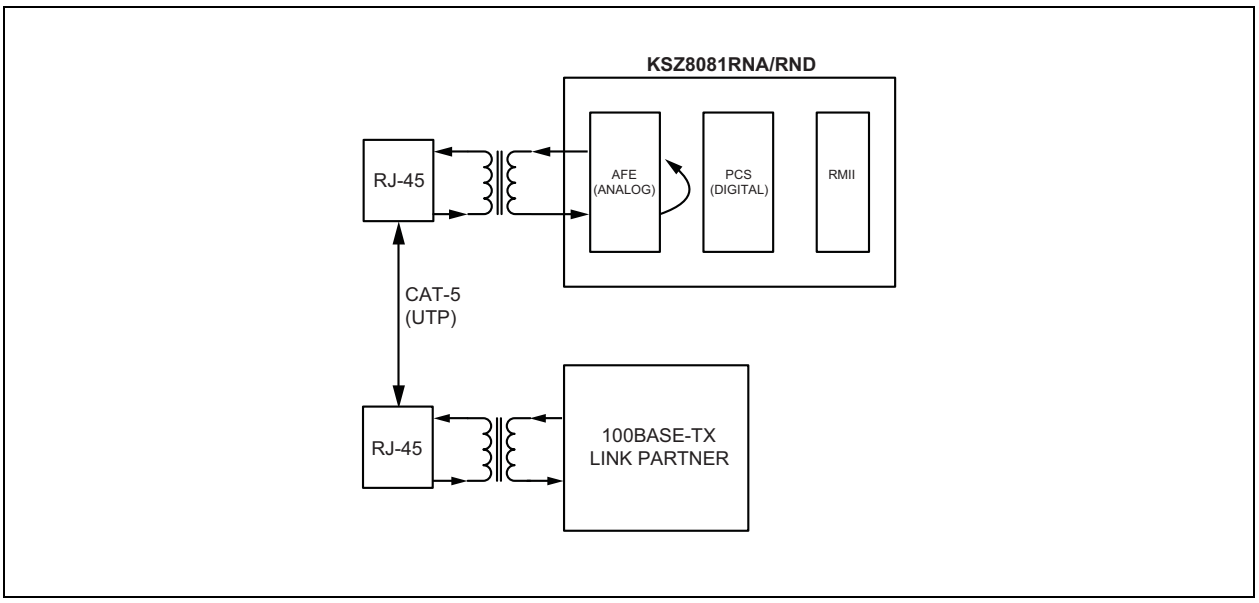
3.7.2 REMOTE (ANALOG) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the KSZ8081RNA/RND and its link partner, and is supported for 100BASE-TX full-duplex mode only.

The loopback data path is shown in Figure 3-8.

1. The Fast Ethernet (100BASE-TX) PHY link partner transmits frames to the KSZ8081RNA/RND.
2. Frames are wrapped around inside the KSZ8081RNA/RND.
3. The KSZ8081RNA/RND transmits frames back to the Fast Ethernet (100BASE-TX) PHY link partner.

FIGURE 3-8: REMOTE (ANALOG) LOOPBACK



The following programming steps and register settings are used for remote loopback mode:

1. Set Register 0h,

Bits [13] = 1 // Select 100Mbps speed

Bit [12] = 0 // Disable auto-negotiation

Bit [8] = 1 // Select full-duplex mode

Or just auto-negotiate and link up at 100BASE-TX full-duplex mode with the link partner.

2. Set Register 1Fh,

Bit [2] = 1 // Enable remote loopback mode

3.8 LinkMD® Cable Diagnostic

The LinkMD function uses time-domain reflectometry (TDR) to analyze the cabling plant for common cabling problems. These include open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing Register 1Dh, the LinkMD Control/Status register, in conjunction with Register 1Fh, the PHY Control 2 register. The latter register is used to disable Auto MDI/MDI-X and to select either MDI or MDI-X as the cable differential pair for testing.

3.8.1 USAGE

The following is a sample procedure for using LinkMD with Registers 1Dh and 1Fh:

1. Disable auto MDI/MDI-X by writing a ‘1’ to Register 1Fh, bit [13].
2. Start cable diagnostic test by writing a ‘1’ to Register 1Dh, bit [15]. This enable bit is self-clearing.
3. Wait (poll) for Register 1Dh, bit [15] to return a ‘0’, and indicating cable diagnostic test is completed.
4. Read cable diagnostic test results in Register 1Dh, bits [14:13]. The results are as follows:

   00 = normal condition (valid test)

   01 = open condition detected in cable (valid test)

   10 = short condition detected in cable (valid test)

   11 = cable diagnostic test failed (invalid test)

The ‘11’ case, invalid test, occurs when the device is unable to shut down the link partner. In this instance, the test is not run, since it would be impossible for the device to determine if the detected signal is a reflection of the signal generated or a signal from another source.

5. Get distance to fault by concatenating Register 1Dh, bits [8:0] and multiplying the result by a constant of 0.38. The distance to the cable fault can be determined by the following formula:

EQUATION 3-1:

$$\text{Distance to cable fault in meters} = 0.38 \times \text{Register 1Dh, bits[8:0]}$$

Concatenated value of Registers 1Dh bits [8:0] should be converted to decimal before multiplying by 0.38.

The constant (0.38) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.9 NAND Tree Support

The KSZ8081RNA/RND provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8081RNA/RND digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the TXD1 pin provides the output for the nested NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving each NAND tree input pin low, sequentially, according to the NAND tree pin order
- Checking the NAND tree output to make sure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

Table 3-5 lists the NAND tree pin order.

TABLE 3-5: NAND TREE TEST PIN ORDER FOR KSZ8081RNA/RND

Pin Number	Pin Name	NAND Tree Description
10	MDIO	Input
11	MDC	Input
12	RXD1	Input
13	RXD0	Input
15	CRS_DV	Input
16	REF_CLK	Input
18	INTRP	Input
19	TXEN	Input
23	LED0	Input
20	TXD0	Input
21	TXD1	Output

3.9.1 NAND TREE I/O TESTING

Use the following procedure to check for faults on the KSZ8081RNA/RND digital I/O pin connections to the board:

1. Enable NAND tree mode by setting Register 16h, Bit [5] to '1'.
2. Use board logic to drive all KSZ8081RNA/RND NAND tree input pins high.
3. Use board logic to drive each NAND tree input pin, in KSZ8081RNA/RND tree pin order, as follows:
   a) Toggle the first pin (MDIO) from high to low, and verify that the TDX1 pin switches from high to low to indicate that the first pin is connected properly.
   b) Leave the first pin (MDIO) low.
   c) Toggle the second pin (MDC) from high to low, and verify that the TXD1 pin switches from low to high to indicate that the second pin is connected properly.
   d) Leave the first pin (MDIO) and the second pin (MDC) low.
   e) Toggle the third pin from high to low, and verify that the TXD1 pin switches from high-to-low to indicate that the third pin is connected properly.
   f) Continue with this sequence until all KSZ8081RNA/RND NAND tree input pins have been toggled.

Each KSZ8081RNA/RND NAND tree input pin must cause the TXD1 output pin to toggle high-to-low or low-to-high to indicate a good connection. If the TXD1 pin fails to toggle when the KSZ8081RNA/RND input pin toggles from high to low, the input pin has a fault.

3.10 Power Management

The KSZ8081RNA/RND incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

3.10.1 POWER-SAVING MODE

Power-saving mode is used to reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a '1' to Register 1Fh, Bit [10], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

In this mode, the KSZ8081RNA/RND shuts down all transceiver blocks except the transmitter, energy detect, and PLL circuits.

By default, power-saving mode is disabled after power-up.

3.10.2 ENERGY-DETECT POWER-DOWN MODE

Energy-detect power-down (EDPD) mode is used to further reduce transceiver power consumption when the cable is unplugged. It is enabled by writing a '0' to Register 18h, Bit [11], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

EDPD mode works with the PLL off (set by writing a '1' to Register 10h, Bit [4] to automatically turn the PLL off in EDPD mode) to turn off all KSZ8081RNA/RND transceiver blocks except the transmitter and energy-detect circuits.

TABLE 3-6: KSZ8081RNA/RND POWER PIN DESCRIPTION

Power Pin	Pin Number	Description
VDD_1.2	1	Decouple with 2.2 µF and 0.1 µF capacitors to ground.
VDDA_3.3	2	Connect to board's 3.3V supply through a ferrite bead. Decouple with 22 µF and 0.1 µF capacitors to ground.
VDDIO	14	Connect to board's 3.3V supply for 3.3V VDDIO. Decouple with 22 µF and 0.1 µF capacitors to ground.

3.12 Typical Current/Power Consumption

Table 3-7, Table 3-8, and Table 3-9 show typical values for current consumption by the transceiver (VDDA_3.3) and digital I/O (VDDIO) power pins and typical values for power consumption by the KSZ8081RNA/RND device for the indicated nominal operating voltage combinations. These current and power consumption values include the transmit driver current and on-chip regulator current for the 1.2V core.

TABLE 3-7: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 3.3V)

Condition	3.3V Transceiver (VDDA_3.3)	3.3V Digital I/Os (VDDIO)	Total Chip Power
100BASE-TX Link-up (no traffic)	34 mA	12 mA	152 mW
100BASE-TX Full-duplex @ 100% utilization	34 mA	13 mA	155 mW
10BASE-T Link-up (no traffic)	14 mA	11 mA	82.5 mW
10BASE-T Full-duplex @ 100% utilization	30 mA	11 mA	135 mW
Power-saving mode (Reg. 1Fh, Bit [10] = 1)	14 mA	10 mA	79.2 mW
EDPD mode (Reg. 18h, Bit [11] = 0)	10 mA	10 mA	66 mW
EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1)	3.77 mA	1.54 mA	1.75 mW
Software power-down mode (Reg. 0h, Bit [11] =1)	2.59 mA	1.51 mA	13.5 mW
Software power-down mode (Reg. 0h, Bit [11] =1) and slow-oscillator mode (Reg. 11h, Bit [5] =1)	1.36 mA	0.45 mA	5.97 mW

TABLE 3-8: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 2.5V)

Condition	3.3V Transceiver (VDDA_3.3)	2.5V Digital I/Os (VDDIO)	Total Chip Power
100BASE-TX Link-up (no traffic)	34 mA	12 mA	142 mW
100BASE-TX Full-duplex @ 100% utilization	34 mA	13 mA	145 mW
10BASE-T Link-up (no traffic)	15 mA	11 mA	77 mW
10BASE-T Full-duplex @ 100% utilization	27 mA	11 mA	117 mW
Power-saving mode (Reg. 1Fh, Bit [10] = 1)	15 mA	10 mA	74.5 mW
EDPD mode (Reg. 18h, Bit [11] = 0)	11 mA	10 mA	61.3 mW
EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1)	3.55 mA	1.35 mA	15.1 mW
Software power-down mode (Reg. 0h, Bit [11] =1)	2.29 mA	1.34 mA	10.9 mW
Software power-down mode (Reg. 0h, Bit [11] =1) and slow-oscillator mode (Reg. 11h, Bit [5] =1)	1.15 mA	0.29 mA	4.52 mW

TABLE 3-9: TYPICAL CURRENT/POWER CONSUMPTION (VDDA_3.3 = 3.3V, VDDIO = 1.8V)

Condition	3.3V Transceiver (VDDA_3.3)	1.8V Digital I/Os (VDDIO)	Total Chip Power
100BASE-TX Link-up (no traffic)	34 mA	11 mA	132 mW
100BASE-TX Full-duplex @ 100% utilization	34 mA	12 mA	134 mW
10BASE-T Link-up (no traffic)	15 mA	10 mA	67.5 mW
10BASE-T Full-duplex @ 100% utilization	27 mA	10 mA	107 mW
Power-saving mode (Reg. 1Fh, Bit [10] = 1)	15 mA	9 mA	65.7 mW
EDPD mode (Reg. 18h, Bit [11] = 0)	11 mA	9 mA	52.5 mW
EDPD mode (Reg. 18h, Bit [11] = 0) and PLL off (Reg. 10h, Bit [4] = 1)	4.05 mA	1.21 mA	15.5 mW
Software power-down mode (Reg. 0h, Bit [11] =1)	2.79 mA	1.21 mA	11.4 mW
Software power-down mode (Reg. 0h, Bit [11] =1) and slow-oscillator mode (Reg. 11h, Bit [5] =1)	1.65 mA	0.19 mA	5.79 mW

4.0 REGISTER DESCRIPTIONS

This chapter describes the various control and status registers (CSRs).

4.1 Register Map

TABLE 4-1: REGISTERS SUPPORTED BY KSZ8081RNA/RND

Register Number (hex)	Description
0h	Basic Control
1h	Basic Status
2h	PHY Identifier 1
3h	PHY Identifier 2
4h	Auto-Negotiation Advertisement
5h	Auto-Negotiation Link Partner Ability
6h	Auto-Negotiation Expansion
7h	Auto-Negotiation Next Page
8h	Link Partner Next Page Ability
9h	Reserved
10h	Digital Reserved Control
11h	AFE Control 1
12h - 14h	Reserved
15h	RXER Counter
16h	Operation Mode Strap Override
17h	Operation Mode Strap Status
18h	Expanded Control
19h - 1Ah	Reserved
1Bh	Interrupt Control/Status
1Ch	Reserved
1Dh	LinkMD Control/Status
1Eh	PHY Control 1
1Fh	PHY Control 2

4.2 Register Descriptions

TABLE 4-2: REGISTER DESCRIPTIONS

Address	Name	Description	Mode Note 4-1	Default
Register 0h – Basic Control				
0.15	Reset	1 = Software reset 0 = Normal operation This bit is self-cleared after a ‘1’ is written to it.	RW/SC	0
0.14	Loopback	1 = Loopback mode 0 = Normal operation	RW	0
0.13	Speed Select	1 = 100Mbps 0 = 10Mbps This bit is ignored if auto-negotiation is enabled (Register 0.12 = 1).	RW	Set by the ANEN_-SPEED strapping pin. See the Strap-In Options - KSZ8081RNA/RND section for details.

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, the auto-negotiation result overrides the settings in Registers 0.13 and 0.8.	RW	Set by the ANEN_SPEED strapping pin. See the Strap-In Options - KSZ8081RNA/RND section for details.
0.11	Power-Down	1 = Power-down mode 0 = Normal operation If software reset (Register 0.15) is used to exit power-down mode (Register 0.11 = 1), two software reset writes (Register 0.15 = 1) are required. The first write clears power-down mode; the second write resets the chip and re-latches the pin strapping pin values.	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from MII 0 = Normal operation	RW	0
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation. This bit is self-cleared after a ‘1’ is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	1
0.7	Collision Test	1 = Enable COL test 0 = Disable COL test	RW	0
0.6:0	Reserved	Reserved	RO	000_0000
Register 1h - Basic Status				
1.15	100Base-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100Base-TX Full-Duplex	1 = Capable of 100Mbps full-duplex 0 = Not capable of 100Mbps full-duplex	RO	1
1.13	100Base-TX Half-Duplex	1 = Capable of 100Mbps half-duplex 0 = Not capable of 100Mbps half-duplex	RO	1
1.12	10Base-T Full-Duplex	1 = Capable of 10Mbps full-duplex 0 = Not capable of 10Mbps full-duplex	RO	1
1.11	10Base-T Half-Duplex	1 = Capable of 10Mbps half-duplex 0 = Not capable of 10Mbps half-duplex	RO	1
1.10:7	Reserved	Reserved	RO	000_0
1.6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Can perform auto-negotiation 0 = Cannot perform auto-negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
1.0	Extended Capability	1 = Supports extended capability registers	RO	1
Register 2h - PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). KENDIN Communication's OUI is 0010A1 (hex).	RO	0022h
Register 3h - PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). KENDIN Communication's OUI is 0010A1 (hex).	RO	0001_01
3.9:4	Model Number	Six-bit manufacturer's model number	RO	01_0110
3.3:0	Revision Number	Four-bit manufacturer's revision number	RO	Indicates silicon revision to Rev. A; A2 = 0x0, A3 = 0x1.
Register 4h - Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability Note: Recommend to set this bit to '0'.	RW	1
4.14	Reserved	Reserved	RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved	Reserved	RO	0
4.11:10	Pause	[00] = No pause [10] = Asymmetric pause [01] = Symmetric pause [11] = Asymmetric and symmetric pause	RW	00
4.9	100BASE-T4	1 = T4 capable 0 = No T4 capability	RO	0
4.8	100BASE-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RW	Set by the ANEN_SPEED strapping pin. See the Strap-In Options - KSZ8081RNA/RND section for details.
4.7	100BASE-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RW	Set by the ANEN_SPEED strapping pin. See the Strap-In Options - KSZ8081RNA/RND section for details.
4.6	10BASE-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RW	1
4.5	10BASE-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001
Register 5h - Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved	Reserved	RO	0
5.11:10	Pause	[00] = No pause [10] = Asymmetric pause [01] = Symmetric pause [11] = Asymmetric and symmetric pause	RO	00
5.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
5.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RO	0
5.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RO	0
5.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RO	0
5.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0001
Register 6h - Auto-Negotiation Expansion				
6.15:5	Reserved	Reserved	RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	RO	0
Register 7h - Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next pages will follow 0 = Last page	RW	0
7.14	Reserved	Reserved	RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic 1 0 = Logic 0	RO	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
16.8:7	Reserved	Reserved	RW	0_0
16.6	RMII B-to-B Override	1 = Override strap-in for RMII back-to-back mode (also set Bit 1 of this register to '1')	RW	0
16.5	NAND Tree Override	1 = Override strap-in for NAND tree mode	RW	0
16.4:2	Reserved	Reserved	RW	0_00
16.1	RMII Override	1 = Override strap-in for RMII mode	RW	1
16.0	Reserved	Reserved	RW	0
Register 17h - Operation Mode Strap Status				
17.15:13	PHYAD[2:0] Strap-In Status	[000] = Strap to PHY Address 0 [011] = Strap to PHY Address 3 The KSZ8081RNA/RND supports only PHY addresses 0h and 3h.	RO	
17.12:2	Reserved	Reserved	RO	
17.1	RMII Strap-In Status	1 = Strap to RMII mode	RO	
17.0	Reserved	Reserved	RO	
Register 18h - Expanded Control				
18.15:12	Reserved	Reserved	RW	0000
18.11	EDPD Disabled	Energy-detect power-down mode 1 = Disable 0 = Enable See also Register 10h, Bit [4] for PLL off.	RW	1
18.10:0	Reserved	Reserved	RW	000_0000_0000
Register 1Bh – Interrupt Control/Status				
1B.15	Jabber Interrupt Enable	1 = Enable jabber interrupt 0 = Disable jabber interrupt	RW	0
1B.14	Receive Error Interrupt Enable	1 = Enable receive error interrupt 0 = Disable receive error interrupt	RW	0
1B.13	Page Received Interrupt Enable	1 = Enable page received interrupt 0 = Disable page received interrupt	RW	0
1B.12	Parallel Detect Fault Interrupt Enable	1 = Enable parallel detect fault interrupt 0 = Disable parallel detect fault interrupt	RW	0
1B.11	Link Partner Acknowledge Interrupt Enable	1 = Enable link partner acknowledge interrupt 0 = Disable link partner acknowledge interrupt	RW	0
1B.10	Link-Down Interrupt Enable	1= Enable link-down interrupt 0 = Disable link-down interrupt	RW	0
1B.9	Remote Fault Interrupt Enable	1 = Enable remote fault interrupt 0 = Disable remote fault interrupt	RW	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
1B.8	Link-Up Interrupt Enable	1 = Enable link-up interrupt 0 = Disable link-up interrupt	RW	0
1B.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occur	RO/SC	0
1B.6	Receive Error Interrupt	1 = Receive error occurred 0 = Receive error did not occur	RO/SC	0
1B.5	Page Receive Interrupt	1 = Page receive occurred 0 = Page receive did not occur	RO/SC	0
1B.4	Parallel Detect Fault Interrupt	1 = Parallel detect fault occurred 0 = Parallel detect fault did not occur	RO/SC	0
1B.3	Link Partner Acknowledge Interrupt	1 = Link partner acknowledge occurred 0 = Link partner acknowledge did not occur	RO/SC	0
1B.2	Link-Down Interrupt	1 = Link-down occurred 0 = Link-down did not occur	RO/SC	0
1B.1	Remote Fault Interrupt	1 = Remote fault occurred 0 = Remote fault did not occur	RO/SC	0
1B.0	Link-Up Interrupt	1 = Link-up occurred 0 = Link-up did not occur	RO/SC	0
Register 1Dh – LinkMD Control/Status				
1D.15	Cable Diagnostic Test Enable	1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared. 0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read.	RW/SC	0
1D.14:13	Cable Diagnostic Test Result	[00] = Normal condition [01] = Open condition has been detected in cable [10] = Short condition has been detected in cable [11] = Cable diagnostic test has failed	RO	00
1D.12	Short Cable Indicator	1 = Short cable (<10 meter) has been detected by LinkMD	RO	0
1D.11:9	Reserved	Reserved	RW	000
1D.8:0	Cable Fault Counter	Distance to fault	RO	0_0000_0000
Register 1Eh – PHY Control 1				
1E.15:10	Reserved	Reserved	RO	0000_00
1E.9	Enable Pause (Flow Control)	1 = Flow control capable 0 = No flow control capability	RO	0
1E.8	Link Status	1 = Link is up 0 = Link is down	RO	0
1E.7	Polarity Status	1 = Polarity is reversed 0 = Polarity is not reversed	RO	
1E.6	Reserved	Reserved	RO	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
1E.5	MDI/MDI-X State	1 = MDI-X 0 = MDI	RO	
1E.4	Energy Detect	1 = Signal present on receive differential pair 0 = No signal detected on receive differential pair	RO	0
1E.3	PHY Isolate	1 = PHY in isolate mode 0 = PHY in normal operation	RW	0
1E.2:0	Operation Mode Indication	[000] = Still in auto-negotiation [001] = 10Base-T half-duplex [010] = 100Base-TX half-duplex [011] = Reserved [100] = Reserved [101] = 10Base-T full-duplex [110] = 100Base-TX full-duplex [111] = Reserved	RO	000
Register 1Fh – PHY Control 2				
1F.15	HP_MDIX	1 = HP Auto MDI/MDI-X mode 0 = Microchip Auto MDI/MDI-X mode	RW	1
1F.14	MDI/MDI-X Select	When Auto MDI/MDI-X is disabled, 1 = MDI-X mode Transmit on RXP,RXM (Pins 4, 3) and Receive on TXP,TXM (Pins 6, 5) 0 = MDI mode Transmit on TXP,TXM (Pins 6, 5) and Receive on RXP,RXM (Pins 4, 3)	RW	0
1F.13	Pair Swap Disable	1 = Disable Auto MDI/MDI-X 0 = Enable Auto MDI/MDI-X	RW	0
1F.12	Reserved	Reserved	RW	0
1F.11	Force Link	1 = Force link pass 0 = Normal link operation This bit bypasses the control logic and allows the transmitter to send a pattern even if there is no link.	RW	0
1F.10	Power Saving	1 = Enable power saving 0 = Disable power saving	RW	0
1F.9	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
1F.8	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
1F.7	RMII Reference Clock Select	1 = For KSZ8081RNA, clock input to XI (Pin 8) is 50MHz for RMII – 50MHz clock mode. For KSZ8081RND, clock input to XI (Pin 8) is 25MHz for RMII – 25MHz clock code. 0 = For KSZ8081RNA, clock input to XI (Pin 8) is 25MHz for RMII – 25MHz clock code. For KSZ8081RND, clock input to XI (Pin 8) is 50MHz for RMII – 50MHz clock mode.	RW	0
1F.6	Reserved	Reserved	RW	0
1F.5:4	LED Mode	[00] = LED0: Link/Activity [01] = LED0: Link [10], [11] = Reserved	RW	00
1F.3	Disable Transmitter	1 = Disable transmitter 0 = Enable transmitter	RW	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode Note 4-1	Default
1F.2	Remote Loopback	1 = Remote (analog) loopback is enabled 0 = Normal mode	RW	0
1F.1	Reserved	Reserved	RW	0
1F.0	Disable Data Scrambling	1 = Disable scrambler 0 = Enable scrambler	RW	0

Note 4-1 RW = Read/Write; RO = Read Only; SC = Self-Cleared; LH = Latch High; LL = Latch Low.

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage (V_{IN})

($V_{DD_1.2}$) ..... –0.5V to +1.8V

(V_{DDIO}, $V_{DDA_3.3}$) ..... –0.5V to +5.0V

Input Voltage (all inputs) ..... –0.5V to +5.0V

Output Voltage (all outputs) ..... –0.5V to +5.0V

Lead Temperature (soldering, 10s) ..... +260°C

Storage Temperature (T_S) ..... –55°C to +150°C

*Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

5.2 Operating Ratings**

Supply Voltage

($V_{DDIO_3.3}$, $V_{DDA_3.3}$) ..... +3.135V to +3.465V

($V_{DDIO_2.5}$) ..... +2.375V to +2.625V

($V_{DDIO_1.8}$) ..... +1.710V to +1.890V

Ambient Temperature

(T_A Commercial) ..... 0°C to +70°C

(T_A Industrial) ..... –40°C to +85°C

Maximum Junction Temperature (T_J max.) ..... +125°C

Thermal Resistance (, $_{JA}$) ..... +47.84°C/W

Thermal Resistance (, $_{JC}$) ..... +14.71°C/W

**The device is not guaranteed to function outside its operating ratings.

Note:	Do not drive input signals without power supplied to the device.

6.0 ELECTRICAL CHARACTERISTICS

T_A = 25°C. Specification is for packaged product only.

TABLE 6-1: ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Note
Supply Current (V_{DDIO}, $V_{DDA_3.3}$ = 3.3V), Note 6-1						
10BASE-T	$I_{DD1_3.3V}$	—	41	—	mA	Full-duplex traffic @ 100% utilization
100BASE-TX	$I_{DD2_3.3V}$	—	47	—	mA	Full-duplex traffic @ 100% utilization
EDPD Mode	$I_{DD3_3.3V}$	—	20	—	mA	Ethernet cable disconnected (Reg. 18h.11 = 0)
Power-Down Mode	$I_{DD4_3.3V}$	—	4	—	mA	Software power-down (Reg. 0h.11 = 1)
CMOS Level Inputs						
Output High Voltage	V_{OH}	2.4	—	—	V	V_{DDIO} = 3.3V
		2.0	—	—	V	V_{DDIO} = 2.5V
		1.5	—	—	V	V_{DDIO} = 1.8V
Output Low Voltage	V_{OL}	—	—	0.4	V	V_{DDIO} = 3.3V
		—	—	0.4	V	V_{DDIO} = 2.5V
		—	—	0.3	V	V_{DDIO} = 1.8V
Output Tri-State Leakage	$\|I_{OZ}\|$	—	—	10	µA	—
LED Output						
Output Drive Current	I_{LED}	—	8	—	mA	LED0 pin
All Pull-Up/Pull-Down Pins (including Strapping Pins)						
Internal Pull-Up Resistance	pu	30	45	73	kΩ	V_{DDIO} = 3.3V
		39	61	102	kΩ	V_{DDIO} = 2.5V
		48	99	178	kΩ	V_{DDIO} = 1.8V
Internal Pull-Down Resistance	pd	26	43	79	kΩ	V_{DDIO} = 3.3V
		34	59	113	kΩ	V_{DDIO} = 2.5V
		53	99	200	kΩ	V_{DDIO} = 1.8V
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_O	0.95	—	1.05	V	100Ω termination across differential output
Output Voltage Imbalance	V_{IMB}	—	—	2	%	100Ω termination across differential output
Rise/Fall Time	t_r/t_f	3	—	5	ns	—
Rise/Fall Time Imbalance	—	0	—	0.5	ns	—
Duty Cycle Distortion	—	—	—	±0.25	ns	—
Overshoot	—	—	—	5	%	—
Output Jitter	—	—	0.7	—	ns	Peak-to-peak
10BASE-T Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_P	2.2	—	2.8	V	100Ω termination across differential output
Jitter Added	—	—	—	3.5	ns	Peak-to-peak
Rise/Fall Time	t_r/t_f	—	25	—	ns	—
10BASE-T Receive						
Squelch Threshold	V_{SQ}	—	400	—	mV	5 MHz square wave
Transmitter - Drive Setting						
Reference Voltage of I_{SET}	V_{SET}	—	0.65	—	V	$R(I_{SET})$ = 6.49 kΩ

7.0 TIMING DIAGRAMS

7.1 RMII Timing

FIGURE 7-1: RMII TIMING - DATA RECEIVED FROM RMII

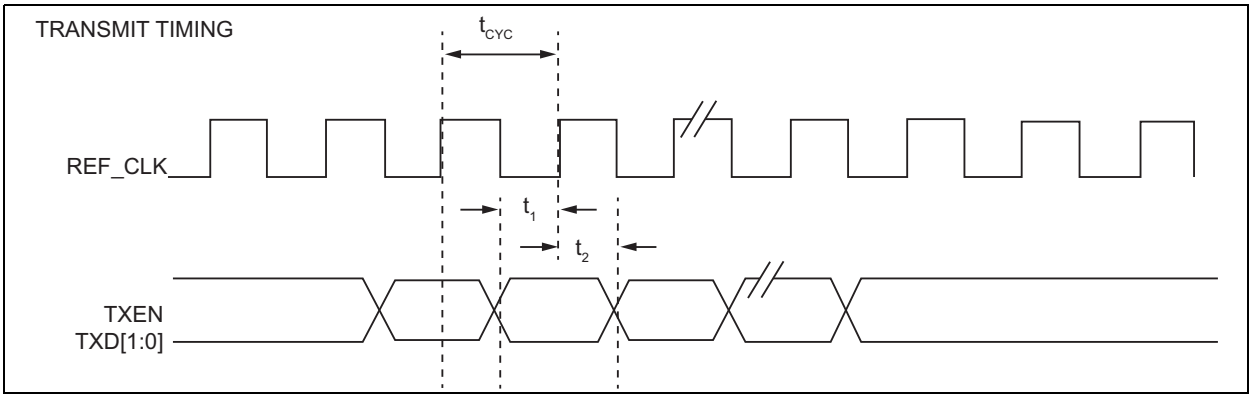


FIGURE 7-2: RMII TIMING - DATA INPUT TO RMII

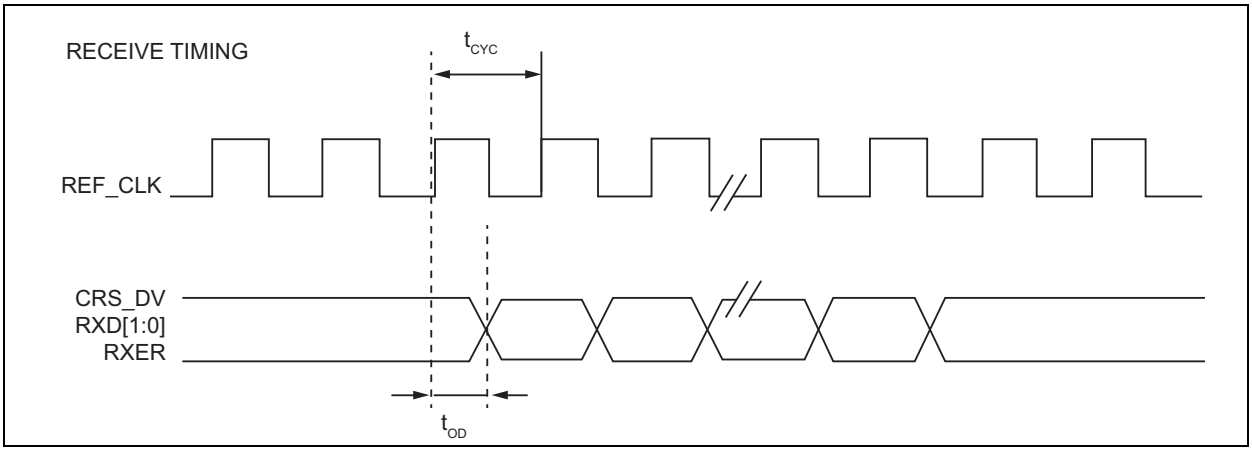


TABLE 7-1: RMII TIMING PARAMETERS (25 MHZ INPUT TO XI PIN, 50 MHZ OUTPUT FROM REF_CLK PIN)

Parameter	Description	Min.	Typ.	Max.	Units
t_{CYC}	Clock cycle	—	20	—	ns
t_1	Setup time	4	—	—	ns
t_2	Hold time	2	—	—	ns
t_{OD}	Output delay	7	10	13	ns

TABLE 7-2: RMII TIMING PARAMETERS (50 MHZ INPUT TO XI PIN)

Parameter	Description	Min.	Typ.	Max.	Units
t_{CYC}	Clock cycle	—	20	—	ns
t_1	Setup time	4	—	—	ns
t_2	Hold time	2	—	—	ns
t_{OD}	Output delay	8	11	13	ns

7.2 Auto-Negotiation Timing

FIGURE 7-3: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING

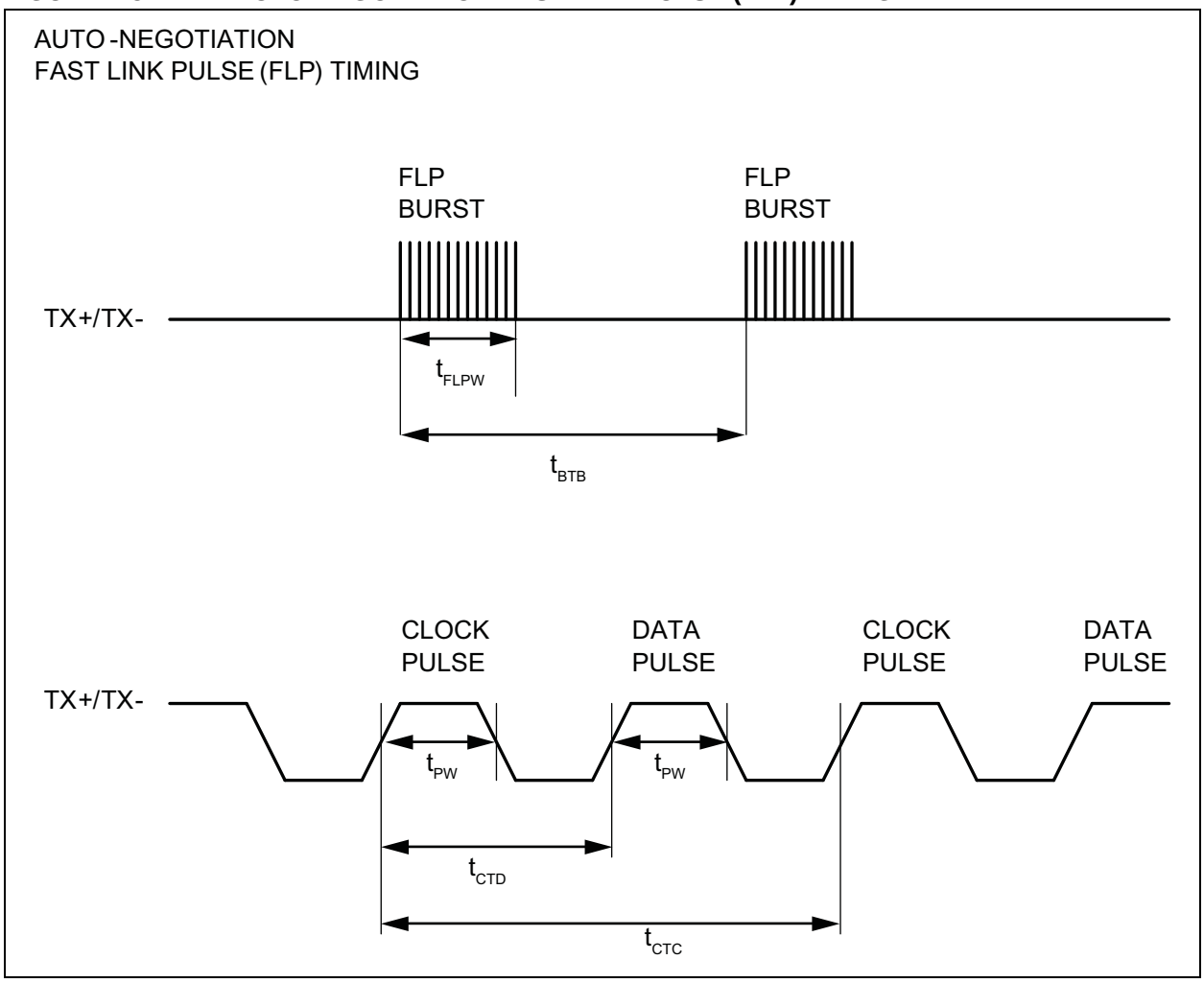


TABLE 7-3: AUTO-NEGOTIATION FAST LINK PULSE TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width	—	2	—	ms
t_{PW}	Clock/Data pulse width	—	100	—	ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
—	Number of clock/data pulses per FLP burst	17	—	33	—

7.3 MDC/MDIO Timing

FIGURE 7-4: MDC/MDIO TIMING

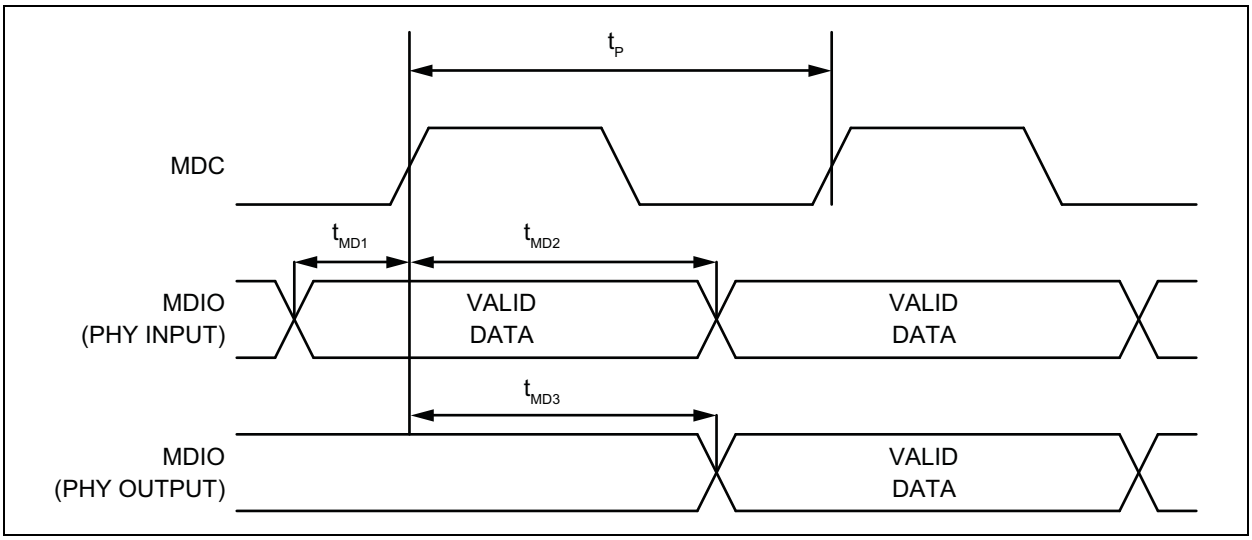


TABLE 7-4: MDC/MDIO TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
fc	MDC Clock Frequency	—	2.5	10	MHz
t_P	MDC period	—	400	—	ns
t_{MD1}	MDIO (PHY input) setup to rising edge of MDC	10	—	—	ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	4	—	—	ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC	5	222	—	ns

7.4 Power-Up/Reset Timing

The KSZ8081RNA/RND reset timing requirement is summarized in Figure 7-5 and Table 7-5.

FIGURE 7-5: POWER-UP/RESET TIMING

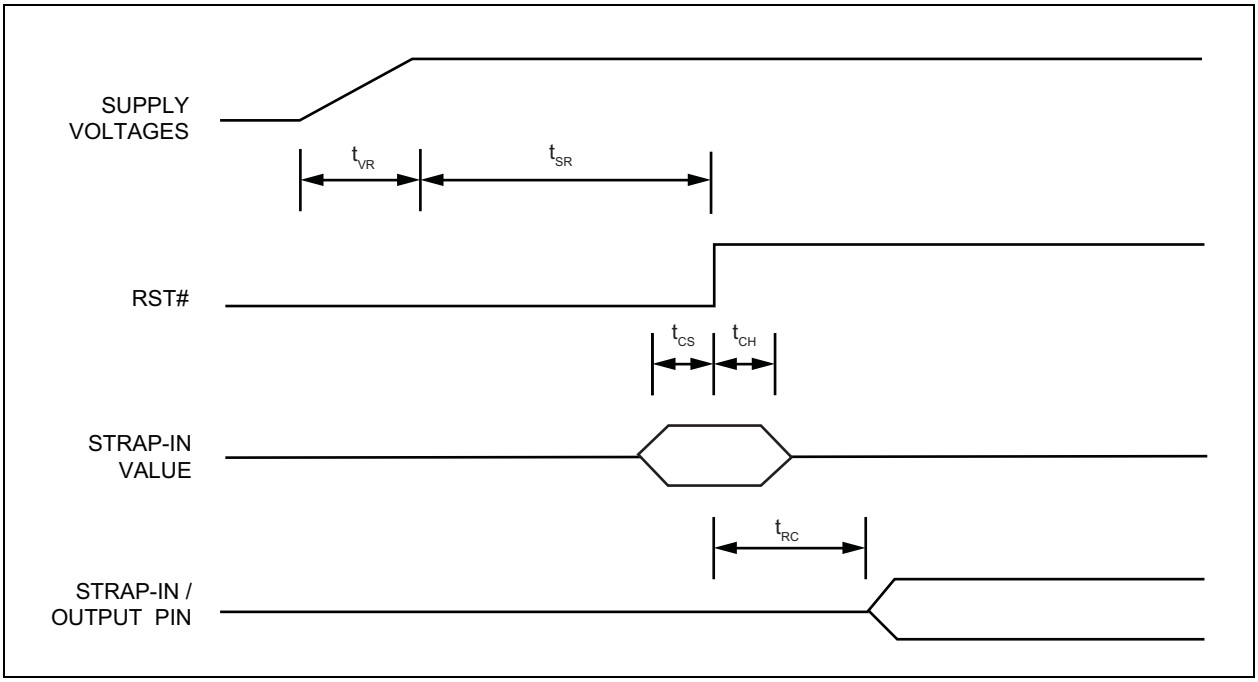


TABLE 7-5: POWER-UP/RESET TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{VR}	Supply voltage (V_{DDIO}, $V_{DDA_3.3}$) rise time	300	—	—	µs
t_{SR}	Stable supply voltage (V_{DDIO}, $V_{DDA_3.3}$) to reset high	10	—	—	ms
t_{CS}	Configuration setup time	5	—	—	ns
t_{CH}	Configuration hold time	5	—	—	ns
t_{RC}	Reset to strap-in pin output	6	—	—	ns

The supply voltage (V_{DDIO} and $V_{DDA_3.3}$) power-up waveform should be monotonic. The 300 µs minimum rise time is from 10% to 90%.

For warm reset, the reset (RST#) pin should be asserted low for a minimum of 500 µs. The strap-in pin values are read and updated at the de-assertion of reset.

After the de-assertion of reset, wait a minimum of 100 µs before starting programming on the MIIM (MDC/MDIO) interface.

8.0 RESET CIRCUIT

Figure 8-1 shows a reset circuit recommended for powering up the KSZ8081RNA/RND if reset is triggered by the power supply.

FIGURE 8-1: RECOMMENDED RESET CIRCUIT

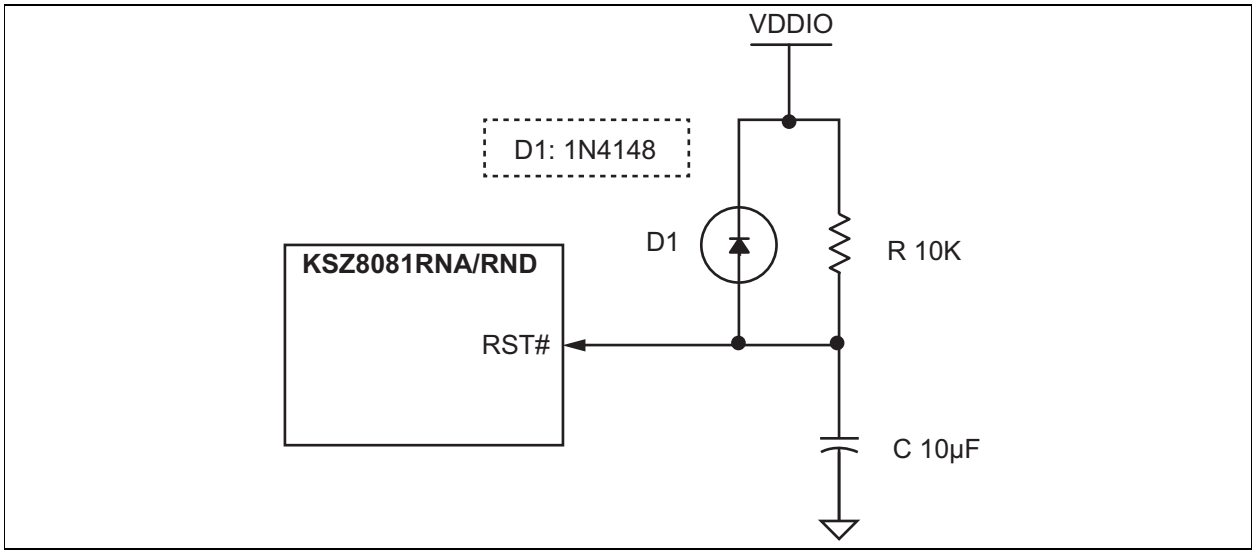
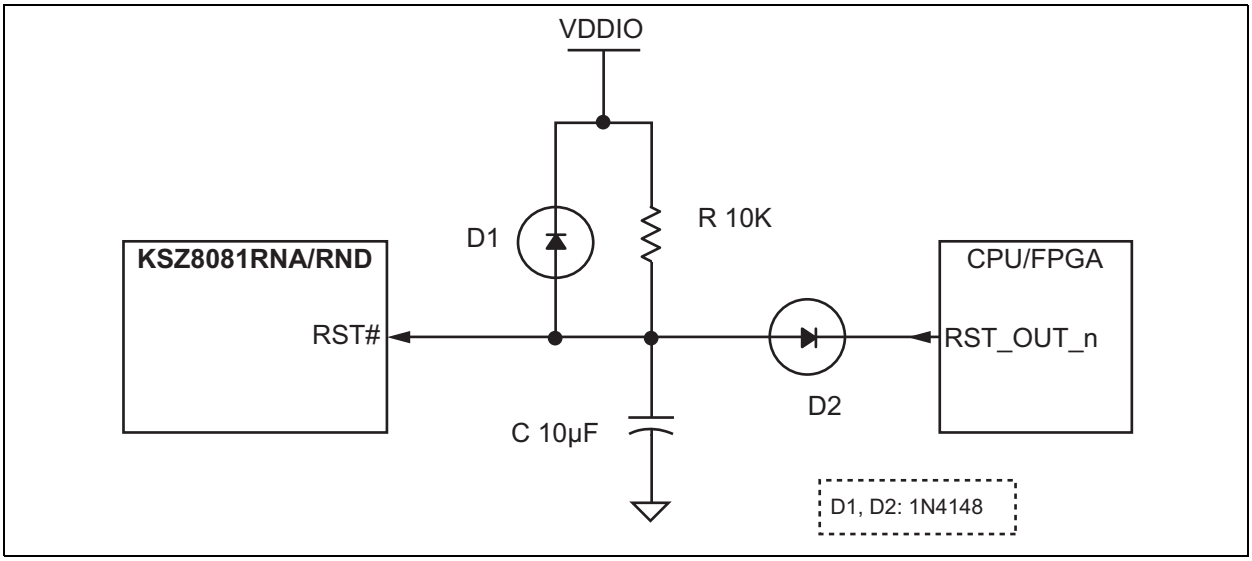


Figure 8-2 shows a reset circuit recommended for applications where reset is driven by another device (for example, the CPU or an FPGA). The reset out RST_OUT_n from CPU/FPGA provides the warm reset after power up reset. D2 is used if using different V_{DDIO} between the switch and CPU/FPGA, otherwise, the different V_{DDIO} will fight each other. If different V_{DDIO} have to use in a special case, a low V_F (<0.3V) diode is required (for example, Vishay's BAT54, MSS1P2L and so on), or a level shifter device can be used too. If Ethernet device and CPU/FPGA use same V_{DDIO} voltage, D2 can be removed to connect both devices directly. Usually, Ethernet device and CPU/FPGA should use same V_{DDIO} voltage.

FIGURE 8-2: RECOMMENDED RESET CIRCUIT FOR CPU/FPGA RESET OUTPUT



10.0 REFERENCE CLOCK - CONNECTION AND SELECTION

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ8081RNA/RND. For the KSZ8081RNA/RND in RMII – 25 MHz clock mode, the reference clock is 25 MHz. The reference clock connections to XI (Pin 8) and XO (Pin 7), and the reference clock selection criteria, are provided in Figure 10-1 and Table 10-1.

FIGURE 10-1: 25 MHZ CRYSTAL/OSCILLATOR REFERENCE CLOCK CONNECTION

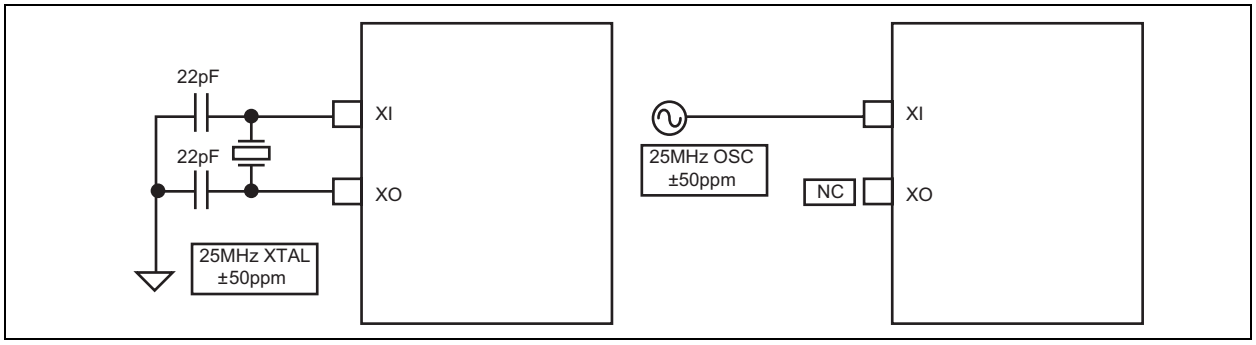


TABLE 10-1: 25 MHZ CRYSTAL/REFERENCE CLOCK SELECTION CRITERIA

Characteristics	Value
Frequency	25 MHz
Frequency Tolerance (max.); Note 10-1	±50 ppm
Crystal Series Resistance (typ.)	40Ω
Crystal Load Capacitance (typ.)	16 pF

Note 10-1 ±60 ppm for overtemperature crystal.

For the KSZ8081RNA/RND in RMII – 50 MHz clock mode, the reference clock is 50 MHz. The reference clock connection to XI (Pin 8), and the reference clock selection criteria are provided in Figure 10-2 and Table 10-2.

FIGURE 10-2: 50 MHZ OSCILLATOR/REFERENCE CLOCK CONNECTION

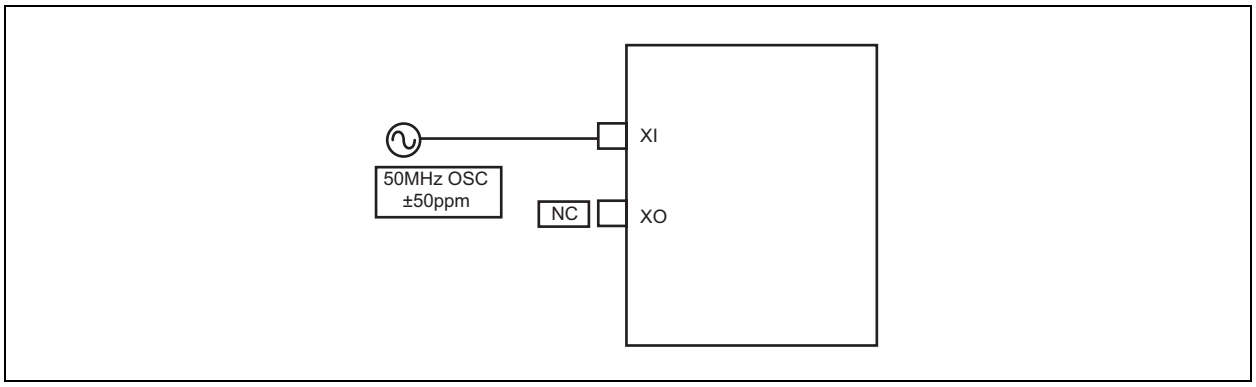


TABLE 10-2: 50 MHZ OSCILLATOR/REFERENCE CLOCK SELECTION CRITERIA

Characteristics	Value
Frequency	50 MHz
Frequency Tolerance (max.)	±50 ppm

11.0 MAGNETIC - CONNECTION AND SELECTION

A 1:1 isolation transformer is required at the line interface. Use one with integrated common-mode chokes for designs exceeding FCC requirements.

The KSZ8081RNA/RND design incorporates voltage-mode transmit drivers and on-chip terminations.

With the voltage-mode implementation, the transmit drivers supply the common-mode voltages to the two differential pairs. Therefore, the two transformer center tap pins on the KSZ8081RNA/RND side should not be connected to any power supply source on the board; instead, the center tap pins should be separated from one another and connected through separate 0.1 µF common-mode capacitors to ground. Separation is required because the common-mode voltage is different between transmitting and receiving differential pairs.

Figure 11-1 shows the typical magnetic interface circuit for the KSZ8081RNA/RND.

FIGURE 11-1: TYPICAL MAGNETIC INTERFACE CIRCUIT

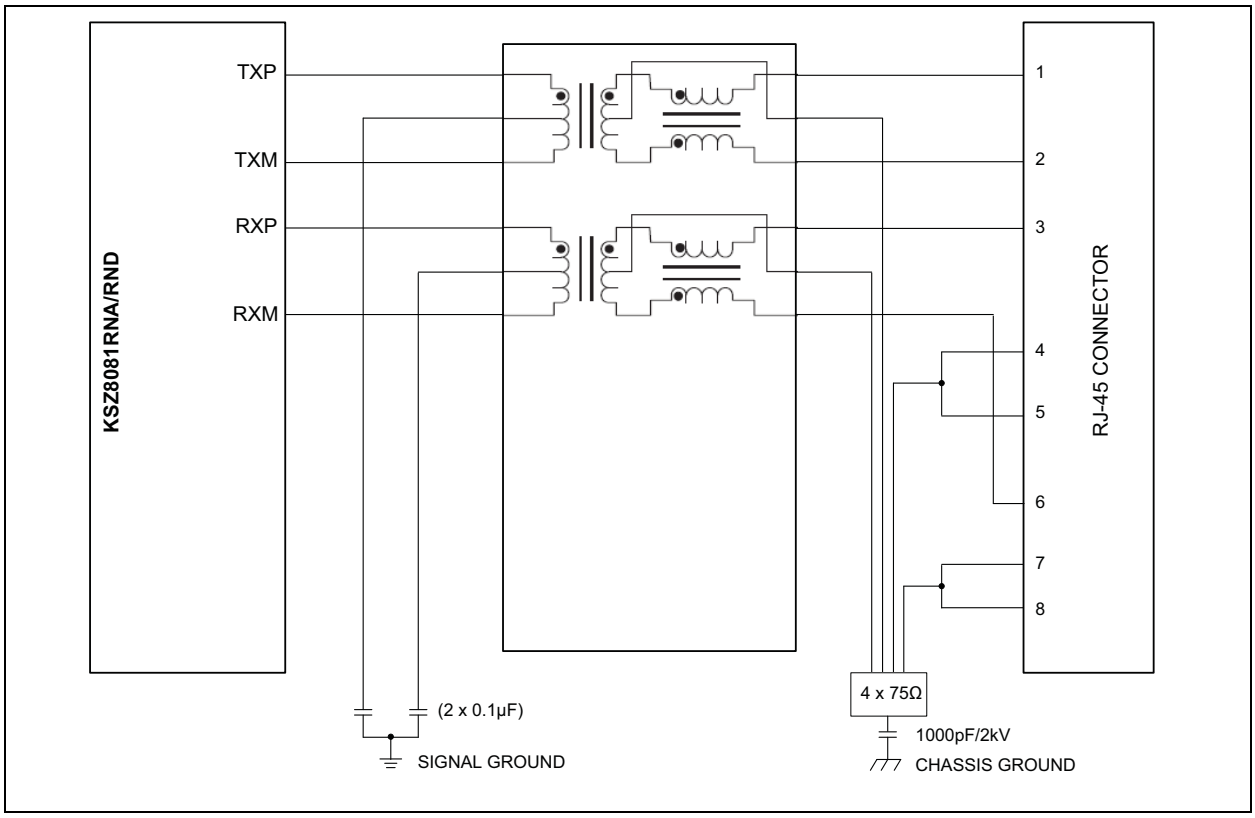


Table 11-1 lists recommended magnetic characteristics.

TABLE 11-1: MAGNETICS SELECTION CRITERIA

Parameter	Value	Test Conditions
Turns Ratio	1 CT : 1 CT	—
Open-Circuit Inductance (min.)	350 µH	100 mV, 100 kHz, 8 mA
Insertion Loss (max.)	–1.1 dB	100 kHz to 100 MHz
HIPOT (min.)	1500 V_{RMS}	—

Table 11-2 is a list of compatible single-port magnetics with separated transformer center tap pins on the PHY chip side that can be used with the KSZ8081RNA/RND.

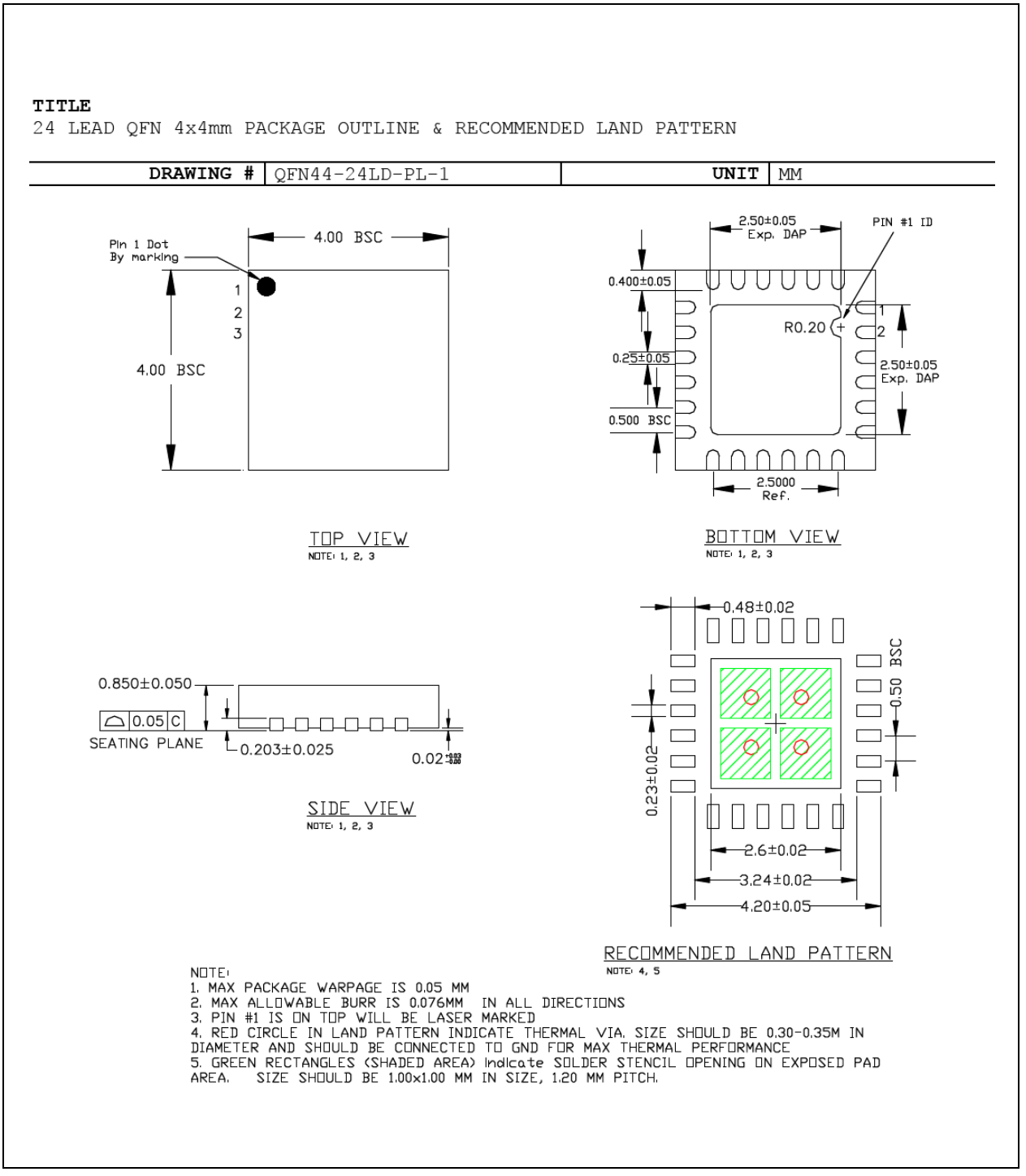
TABLE 11-2: COMPATIBLE SINGLE-PORT 10/100 MAGNETICS

Manufacturer	Part Number	Temperature Range	Magnetic + RJ-45
Bel Fuse	S558-5999-U7	0°C to 70°C	No
Bel Fuse	SI-46001-F	0°C to 70°C	Yes
Bel Fuse	SI-50170-F	0°C to 70°C	Yes
Delta	LF8505	0°C to 70°C	No
HALO	HFJ11-2450E	0°C to 70°C	Yes
HALO	TG110-E055N5	–40°C to 85°C	No
LANKom	LF-H41S-1	0°C to 70°C	No
Pulse	H1102	0°C to 70°C	No
Pulse	H1260	0°C to 70°C	No
Pulse	HX1188	–40°C to 85°C	No
Pulse	J00-0014	0°C to 70°C	Yes
Pulse	JX0011D21NL	–40°C to 85°C	Yes
TDK	TLA-6T718A	0°C to 70°C	Yes
Transpower	HB726	0°C to 70°C	No
Wurth/Midcom	000-7090-37R-LF1	–40°C to 85°C	No

12.0 PACKAGE OUTLINE

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

FIGURE 12-1: 24-LEAD QFN 4 MM X 4 MM PACKAGE



APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002199A (06-14-16)	—	Converted Micrel data sheet KSZ8081RNA/RND to Microchip DS00002199A. Minor text changes throughout.

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PART NO.	X	X	X	X
Device	Interface	Package	Special Attribute	Temperature

Device:	KSZ8081
Interface:	R = RMII
Package:	N = 24-pin QFN
Special Attribute:	A = 25 MHz Input/50 MHz Output Clocks D = 50 MHz Input Clock
Temperature:	CA = 0 C to +70 C (Commercial) IA = –40 C to +85 C (Industrial)

Examples:

a) KSZ8081RNACA
RMII Interface
24-pin QFN
25 MHz Input/50 MHz Output
Commercial Temperature

b) KSZ8081RNAIA
RMII Interface
24-pin QFN
25 MHz Input/50 MHz Output
Industrial Temperature

c) KSZ8081RNDCA
RMII Interface
24-pin QFN
50 MHz Input
Commercial Temperature

d) KSZ8081RNDIA
RMII Interface
24-pin QFN
50 MHz Input
Industrial Temperature

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