AN2603
Application note

ST1S09 high efficiency synchronous buck converter

Introduction

The ST1S09 family of synchronous step-down DC-DC converters is optimized for powering all low-voltage applications and, generally, to replaces high current linear solutions when power dissipation may cause high heating of the application environment. It provides up to 2 A over an input voltage range of 2.7 V to 5.5 V.

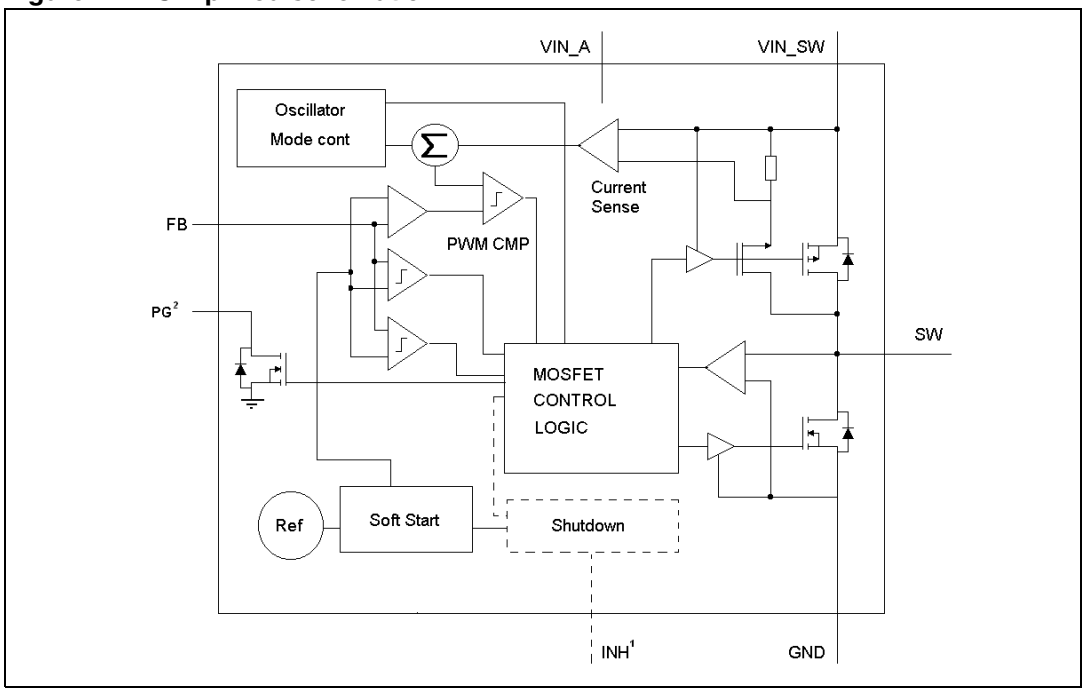
A high 1.5 MHz switching frequency allows the use of tiny surface-mount components, and in addition to the resistor divider to set the output voltage value, an inductor and two capacitors are required. A low output ripple is guaranteed by the current mode PWM topology and by the use of low ESR surface-mount ceramic capacitors.

The device is available in two versions: the ST1S09 with Power Good function and the ST1S09I with an Inhibit function.

The device is thermally protected and current limited to prevent damage due to accidental short circuit.

The ST1S09 family is available in the DFN6 3x3 package.

Figure 1. Simplified schematic



Note: 1 Available only for the ST1S09I

2 Available only for the ST1S09

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1 ST1S09 description

The ST1S09 is a family of adjustable current mode PWM synchronous step-down DC-DC converters with internal 2 A power switch. It is a complete 2 A switching regulator with internal compensation which eliminates the need for additional components. The ST1S09 devices operate at a fixed frequency of 1.5 MHz (typ).

To maintain good efficiency, the device operates in power-save mode at light load condition (*Figure 2* and *Figure 3*). When the load increases it automatically switches to PWM (pulse width modulation) mode, in order to reduce the output voltage ripple (*Figure 4* and *Figure 5*).

Figure 2. Inductor current at light load

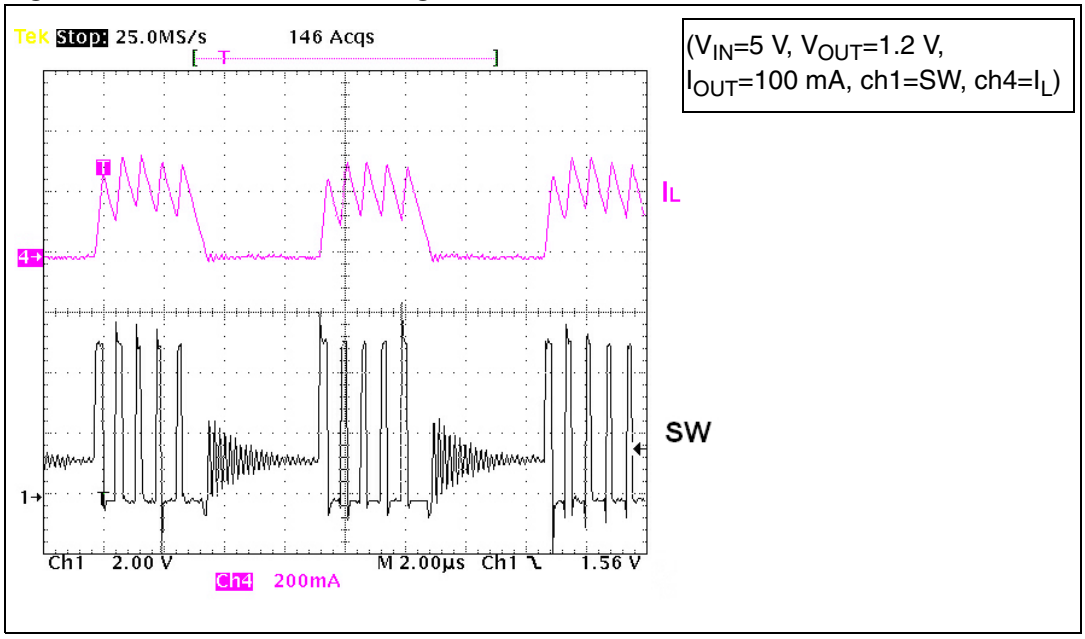


Figure 3. Output voltage ripple at light load

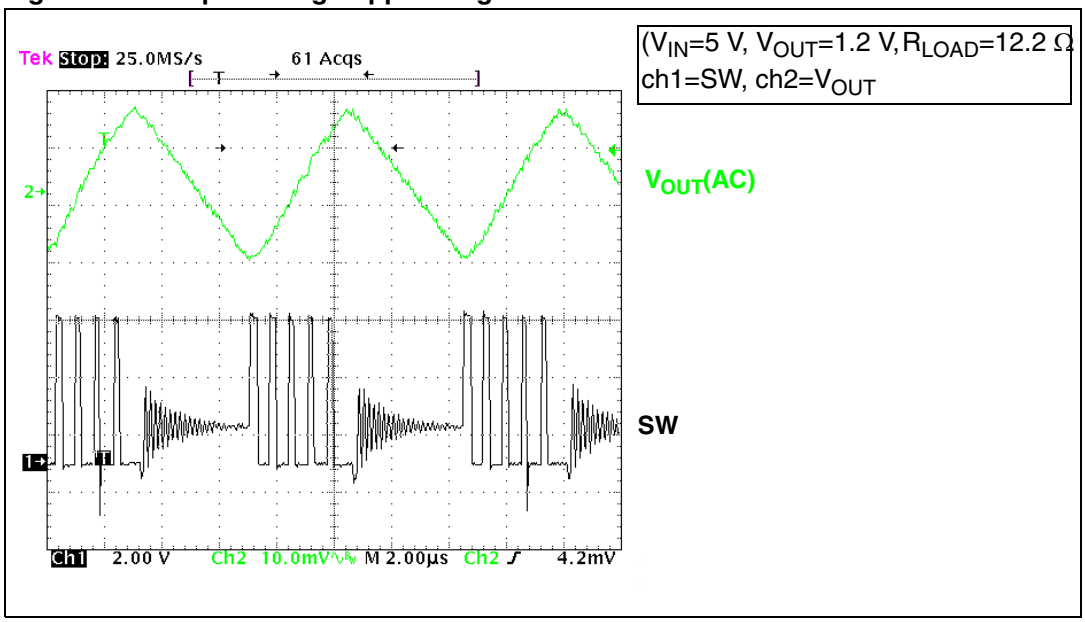


Figure 4. Inductor current in PWM

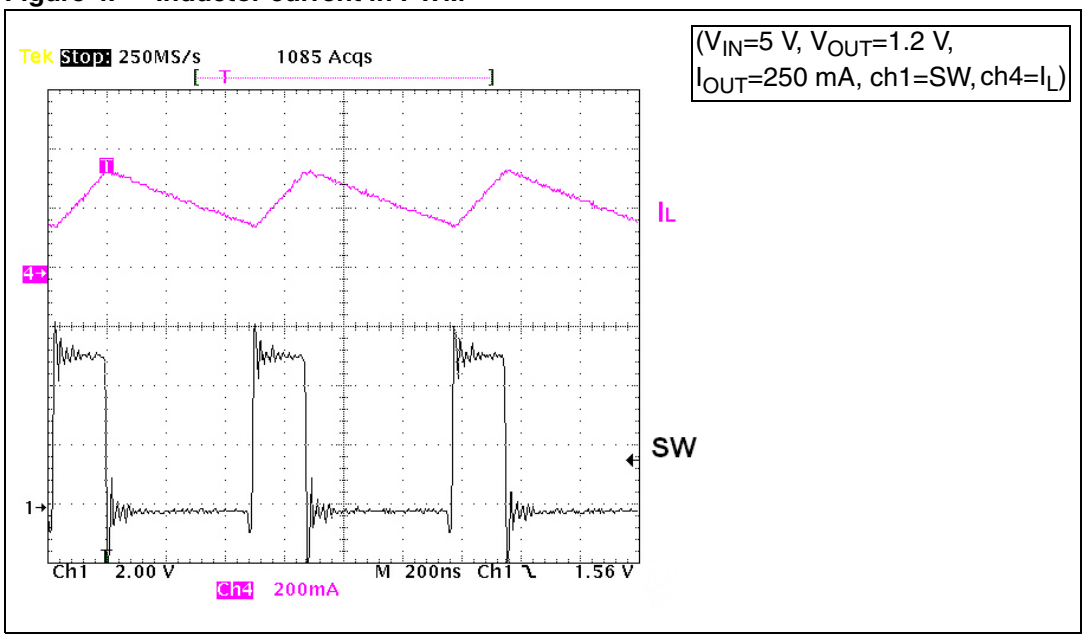
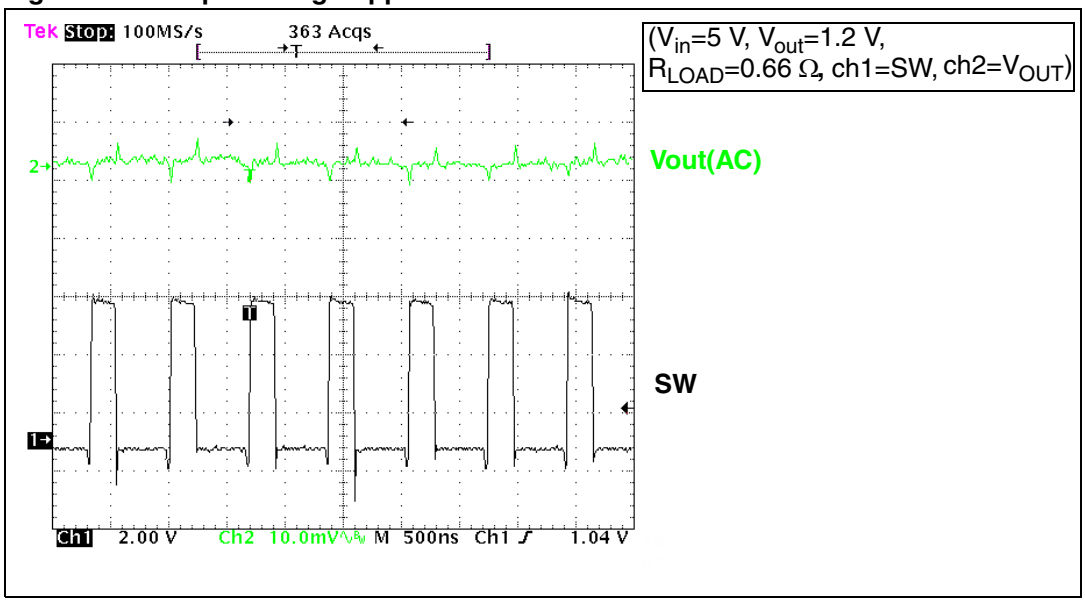


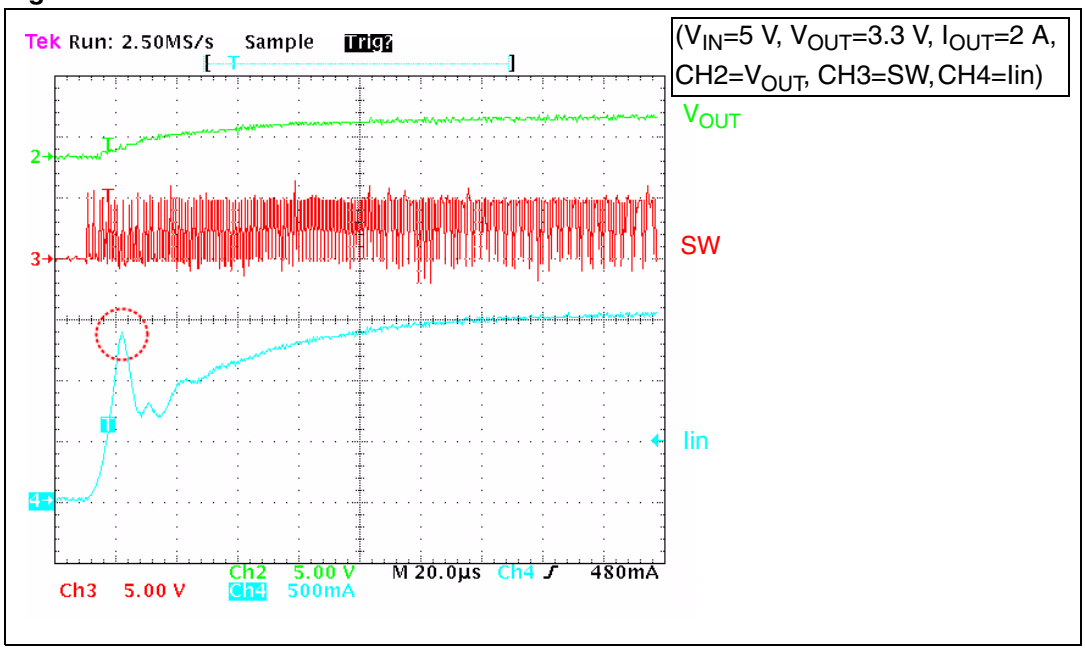
Figure 5. Output voltage ripple in PWM



To clamp the error amplifier reference voltage, a soft start control block generating a voltage ramp is implemented. When switching on the power supply, it allows control of the inrush current value (*Figure 6*). When the input voltage is below 3.7 V (typ.), the under-voltage lock out maintains the ST1S09 in shut down (this function is not available in the ST1S09I).

Other protection circuits in the device are: the Thermal Shut down block which turns off the regulator when the junction temperature exceeds 150°C, and the cycle-by-cycle current limiting that provides protection against shorted outputs.

Figure 6. Inrush current



As an adjustable regulator, the output voltage of the ST1S09 is determined by an external resistor divider. The desired value is given by the following equation:

Equation 1

$$V_{OUT} = V_{FB} \cdot \left[1 + \frac{R1}{R2}\right]$$

Few components are required for operation of the device: an inductor, two capacitors and the resistor divider. The chosen inductor must be capable of withstanding peak current level without saturating. The inductor value can be selected taking into consideration that a large inductor value increases the efficiency at low output current and reduces output voltage ripple, while a smaller inductor can be chosen when it is important to reduce package size and total application cost. Moreover, the ST1S09 family has been designed to function properly with X5R or X7R SMD ceramic capacitors both at the input and at the output. This type of capacitor minimizes the output voltage ripple, thanks to its very low series resistance (ESR). Other low ESR capacitors can be used based on application requirements without compromising the correct functioning of the device.

Due to the high switching frequency and peak current, it is important to optimize the application environment by reducing the length of the PCB traces and placing all external components in close proximity to the device.

1.1 Inhibit function (ST1S09I only)

The ST1S09I features an Inhibit function (pin6). When the INH voltage is higher than 1.3 V the device is ON, and if it is lower than 0.4 V the device is OFF. In shutdown mode, consumption is lower than 1 µA.

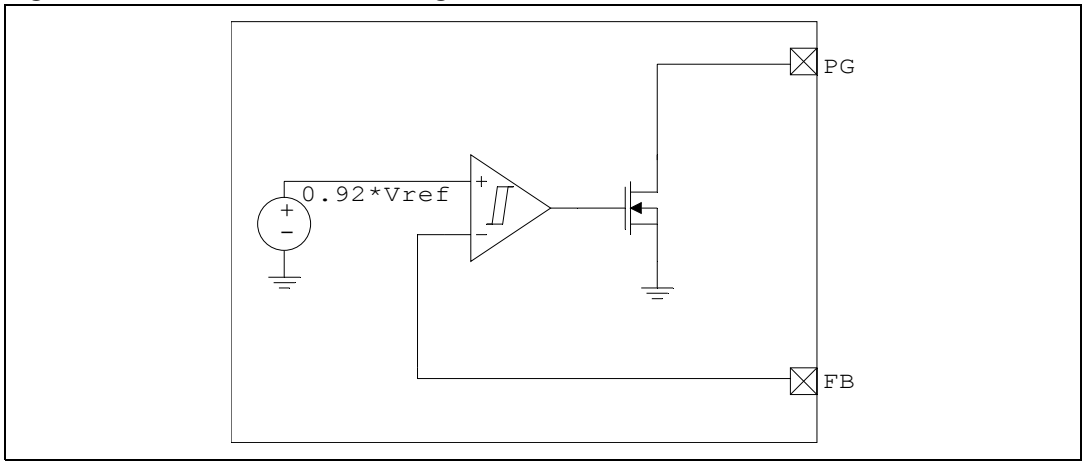
The INH pin does not have an internal pull-up, which means that the Inhibit pin cannot be left floating.

If Inhibit function is not used, the INH pin must be connected to V_{IN}.

1.2 Power Good function (ST1S09 only)

Most ODD applications require a flag showing that the output voltage is in the correct range. The Power Good threshold depends on the feedback voltage. When the feedback is higher than 0.92* V_{FB}, the Power Good (PG) pin goes to high impedance. If the feedback is below 0.92*V_{FB} the PG pin goes in low impedance. If the device is working well, V_{FB} is higher than 0.736 V (PG threshold, 0.92* 0.8 V) and the Power Good pin is at high impedance.

Figure 7. Power Good block diagram

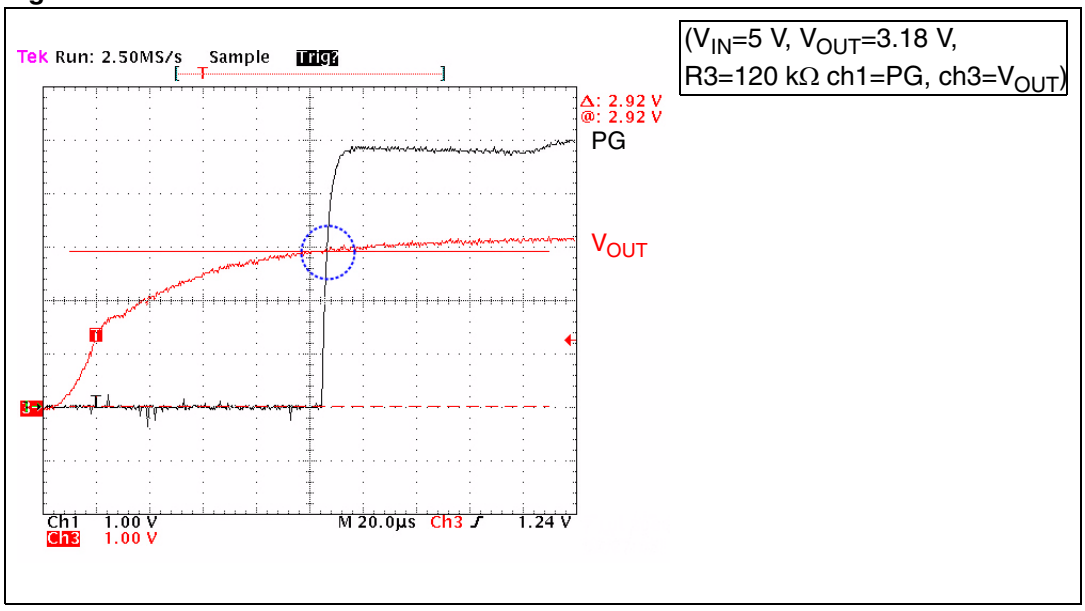


If the output voltage is fixed using an external or internal resistor divider, the Power Good threshold is 0.92*V_{OUT}.

The use of the Power Good function requires an external pull-up resistor, which must be connected between the PG pin and V_{IN} or V_{OUT}. The typical current capability of the PG pin is up to 6 mA. The use of a pull-up resistor for PG in the range of 100 kΩ to 1 MΩ is recommended. If the Power Good function is not used, the PG pin must remain floating in the board.

In the application board, R3 is used to pull up the PG pin to V_{IN} and R4 to pull up the PG pin to V_{OUT}. The Power Good pin can be connected only to V_{IN} or V_{OUT}.

Figure 8. Power Good



1.3 Over voltage protection

When output voltage is over 10% of the nominal value, a small NMOS is turned on to discharge the output. The limitation of the clamping current is about 300 mA.

When the output voltage drops below 1.05*V_{out}, the device returns to normal closed loop switching operation.

1.4 Short circuit protection

In over-current protection mode, when the peak current reaches the current limit, the device reduces the T_{ON} down to its minimum value. In these conditions, the duty cycle is strongly reduced and, in most applications, this is enough to limit the current to I_{lim}.

In cases of heavy short circuit at the output (V_{OUT} = 0 V) and depending on the application conditions (V_{IN} value and parasitic effect of external components) the current peak could reach values higher than I_{lim}. This can be understood by considering the inductor current ripple during the ON and OFF phases:

- ON phase

Equation 2

$$\Delta I_L = \frac{V_{IN} - V_{OUT} - DCR_L \cdot I}{L} \cdot T_{ON}$$

- OFF phase

Equation 3

$$\Delta I_L = \frac{V_D + V_{OUT} + DCR_L \cdot I}{L} \cdot T_{OFF}$$

Where V_D is the voltage drop across the internal NDMOS and DCR_L is the series resistance of the inductor. In short-circuit conditions V_{OUT} is negligible. So, during the T_{OFF}, the voltage applied to the inductor is very small and it is possible that the current ripple in this phase will not compensate for the current ripple during the T_{ON}. The maximum current peak can be easily measured through the inductor with V_{OUT} = 0 V (short-circuit) and $V_{IN} = V_{INmax}$. If the application is required to sustain the short-circuit condition for an extended period, the external components (mainly the inductor) must be selected based on this value.

2 Selecting components for the application

This section provides information to assist in the selection of the most appropriate components for the intended application.

2.1 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current. Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb switching current that can be as high as the load current divided by two (in the worst case, with a duty cycle of 50%). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thus improving system reliability and efficiency.

The critical parameter is usually the RMS current rating, which must be higher than the RMS input current. The maximum RMS input current (flowing through the input capacitor) is:

Equation 4

$$I_{RMS} = I_{OUT} \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta}}$$

where η is the expected system efficiency, D is the duty cycle and I_{OUT} the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_{OUT} divided by 2 (considering η= 1). The maximum and minimum duty cycles are:

Equation 5

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 6

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

where V_F it is the voltage drop across the internal NMOS and V_{SW} the voltage drop across the internal PMOS. Considering the range D_{MIN} to D_{MAX} it is possible to determine the maximum I_{RMS} flowing through the input capacitor.

Capacitors to consider are:

- Ceramic capacitors. These capacitors usually have a high RMS current rating for a given physical dimension (due to the very low ESR). The drawback is the substantially higher cost for larger value capacitors.
- Electrolytic capacitors. Very good tantalum capacitors are becoming available, featuring very low ESR and small size. However they are subject to thermal damage if subjected to very high current during charge. So, it is better to avoid this type of capacitor for the input filter of the device. Aluminum capacitors are not the best choice due to their high ESR.

2.2 Output capacitor

The output capacitor is very important to satisfy the output voltage ripple requirement. Using a small inductor value is useful to reduce the size of the coil, but this increases the current ripple. Therefore, to reduce the output voltage ripple a low ESR capacitor is required. The output voltage ripple (V_{OUT_RIPPLE}), in continuous mode, is:

Equation 7

$$V_{OUT\_RIPPLE} = \Delta I \cdot \left(ESR + \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}} \right)$$

where ΔI is the ripple current and F_{SW} is the switching frequency.

2.3 Inductor

The inductor value is very important because it fixes the ripple current flowing through output capacitor. The ripple current is usually fixed at 20-40% of I_{out_max}, which is 0.4-0.8 A with I_{out_max} = 2 A. The approximate inductor value is obtained using the following formula:

Equation 8

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \cdot T_{ON}$$

where T_{ON} is the ON time of the internal switch, given by D · T.

For example, with V_{OUT} = 3.3 V, V_{IN} = 5 V and ΔI_{OUT} = 0.45 A, the inductor value is around 2.8 µH. The peak current thought the inductor is given by:

Equation 9

$$I_{PK} = I_{OUT} + \frac{\Delta I}{2}$$

It can be observed that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. So, for fixed peak current protection, a higher value of the inductor permits a higher value for the output current.

3 Thermal considerations

The dissipated power of the device is determined by three separate factors:

- Switching losses due to the $R_{DS(ON)}$. These are equal to:

Equation 10

$$P_{ON\_P} = R_{DSON\_P} \cdot I^2_{OUT} \cdot D$$

and

Equation 11

$$P_{ON\_N} = R_{DSON\_N} \cdot I^2_{OUT} \cdot (1 - D)$$

where D is the duty cycle of the application.

Note: the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but in practice it is significantly higher than this value to compensate for the losses of the overall application. For this reason, the switching losses related to the $R_{DS(ON)}$ increase compared to an ideal case.

- On and OFF switching losses. These are given by the following relation:

Equation 12

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{ON} + T_{OFF})}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

where T_{ON} and T_{OFF} are the overlap times of the voltage across the power switch and the current flowing into it during the turn on and turn off phases. T_{SW} is the equivalent switching time.

- Quiescent current losses:

Equation 13

$$P_Q = V_{IN} \cdot I_Q$$

where I_Q is the quiescent current.

Example: V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 1.5 A

The $R_{DS(ON)}$ has a typical value of 0.12 Ω @ 25 °C and increases up to a maximum value of 0.16 Ω @ 150 °C. Considering a value of 0.15 Ω, T_{SW} is approximately 20 ns and I_Q has a typical value of 1.5 mA @ V_{IN} = 5 V. The overall losses are:

Equation 14

$$P_{TOT} = R_{DSON\_P} \cdot I^2_{OUT} \cdot D + R_{DSON\_N} \cdot I^2_{OUT} \cdot (1 - D) + V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW} + V_{IN} \cdot I_Q =$$
$$= 0.15 \cdot 1.5^2 \cdot 0.73 + 0.12 \cdot 1.5^2 \cdot (1 - 0.73) + 5 \cdot 1.5 \cdot 20 \cdot 10^{-9} \cdot 1.5 \cdot 10^6 + 5 \cdot 1.5 \cdot 10^{-3} \cong 0.552W$$

The junction temperature of the device will be:

Equation 15

$$T_J = T_A + Rth_{J-A} \cdot P_{TOT}$$

where T_A is the ambient temperature and Rth_{J-A} is the junction to ambient thermal resistance.

Considering that the device, mounted on the board with a good ground plane, has a thermal resistance junction to ambient (Rth_{J-A}) of about 55°C/W and considering an ambient temperature of about 85°C, the junction temperature is:

Equation 16

$$T_J = 85 + 0.552 \cdot 55 = 115°C$$

4 Recommendations on board usage

The board shown in *Figure 9* is provided with kelvin connection, which means that two lines are available for each pin, one used for supplying or sinking current and the other used to perform the necessary measurements.

The ST1S09 Inhibit pin does not have an internal pull up, meaning that the Inhibit pin cannot be left floating.

Figure 9. ST1S09 board illustration

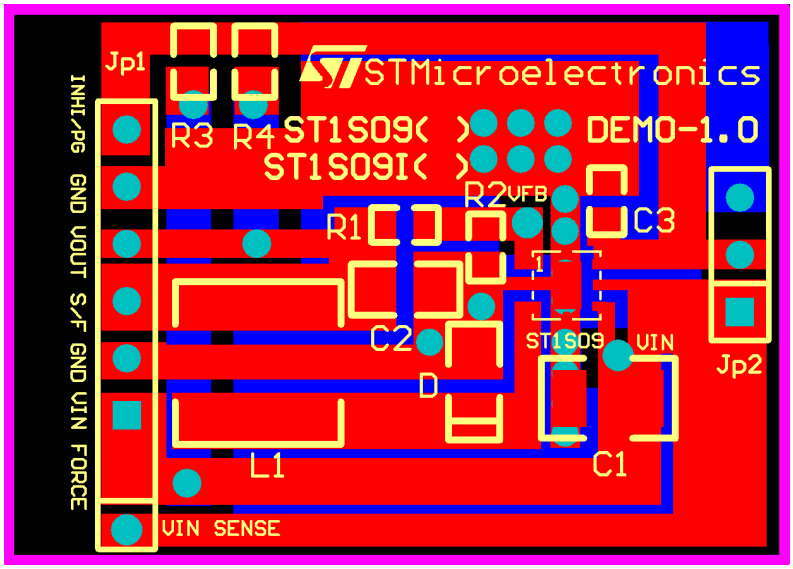
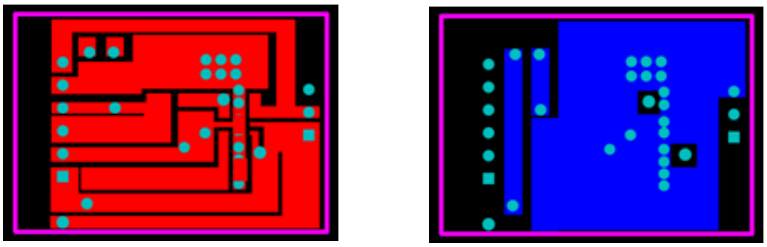


Figure 10. Board layers



Top layer **Bottom layer**

The board has two available Inhibit pins. One is located on the right side of the board and allows a connection to GND or V_{IN}, via a jumper, to turn the device OFF or ON. The other Inhibit pin, located on the top left of the board, can be used to supply an external voltage greater than 1.3 V to turn ON the device, or lower than 0.4 V to turn OFF the device.

4.1 External component selection

Figure 11 and *Figure 12* show the typical application schematics.

Figure 11. ST1S09 application schematic

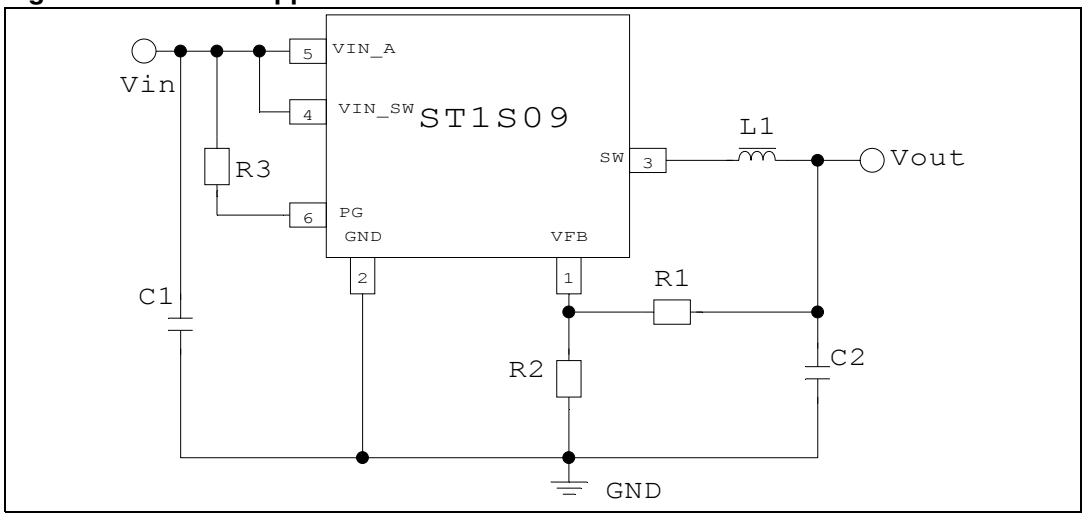
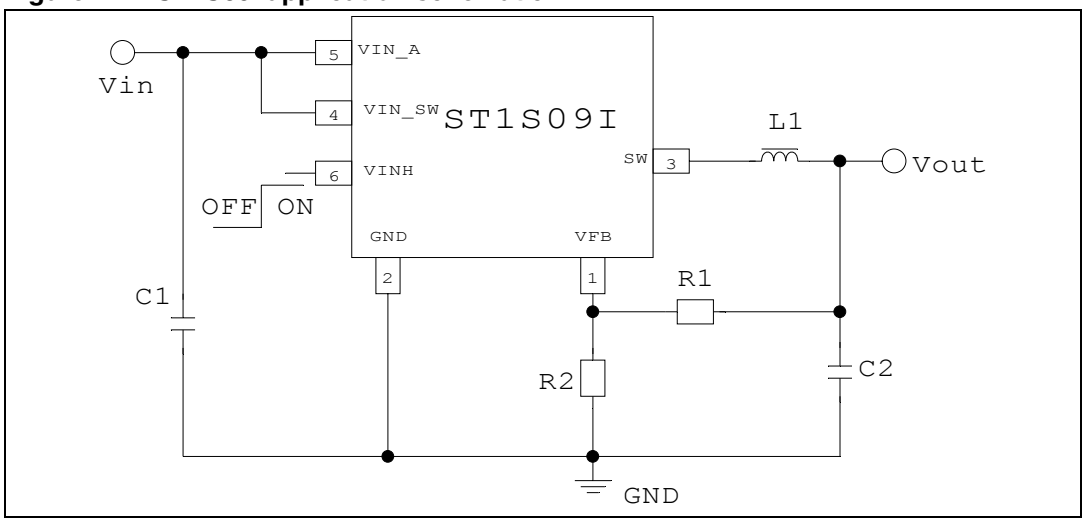


Figure 12. ST1S09I application schematic



In order to obtain the needed output voltage, the resistor divider must be selected in accordance with the following formula:

Equation 17

$$V_{OUT} = V_{FB} \cdot \left[1 + \frac{R1}{R2}\right] \quad \text{with} \quad V_{FB} = 0.8V$$

Table 1. Recommended resistor divider

V_{OUT}	R1	R2
1.2 V	27 kΩ	47 kΩ
3.3 V	47 kΩ	15 kΩ

The resistors in *Table 1* provide a suitable compromise in terms of current consumption and minimum output voltage. For output voltages close to the feedback voltage, we suggest to add a very small capacitor in parallel with R1 in the range of 10 pF. Or, as an alternative, we suggest to increase the current in the resistor divider by decreasing the R1 and R2 value.

4.1.1 Inductor selection

Due to the high frequency (1.5 MHz) it is possible to use very small inductor values. In this board the device was tested with inductors in the range of 1 µH to 10 µH, with very good efficiency results (see below plot).

As the device is able to provide an operative output current of 2 A, The use of inductors capable of managing at least 3 A is strongly recommended.

4.1.2 Capacitor selection

It is possible to use any X5R or X7R ceramic capacitor:

- C1 = 4.7 µF (ceramic) or higher.
- C2 = 22 µF (ceramic) or higher. It is possible to put several capacitors in parallel in order to reduce the equivalent series resistance and improve the ripple present in the output voltage.

4.2 Layout considerations

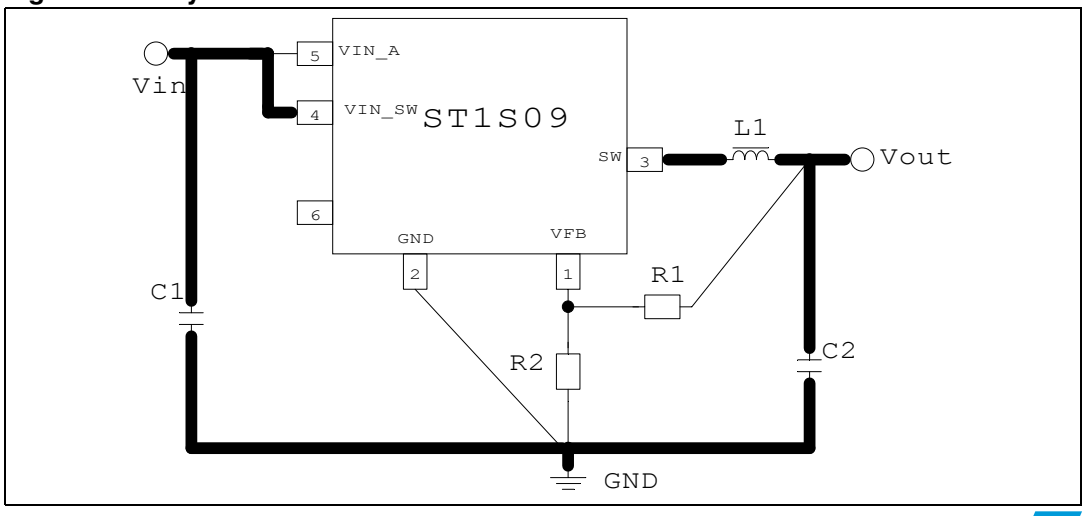
Due to the high switching frequency and peak current, the layout is an important design step for all switching power supplies. If the layout is not done carefully, important parameters such as efficiency and output voltage ripple could be compromised.

Short, wide traces must be implemented for main current and for power ground paths as showed in bold in *Figure 13*. The input capacitor must be placed as close as possible to the device pins as well as the inductor and output capacitor.

It is very important to connect the two input pins 4 mm far from the device, it avoids noise inside the control circuit, coming from the power switch, as shown in *Figure 9*.

A common ground node minimizes ground noise, as shown in *Figure 13*. The exposed pad of the package must be connected to common ground node.

Figure 13. Layout considerations



5 Typical performance characteristics

Figure 14. Feedback voltage vs. temperature

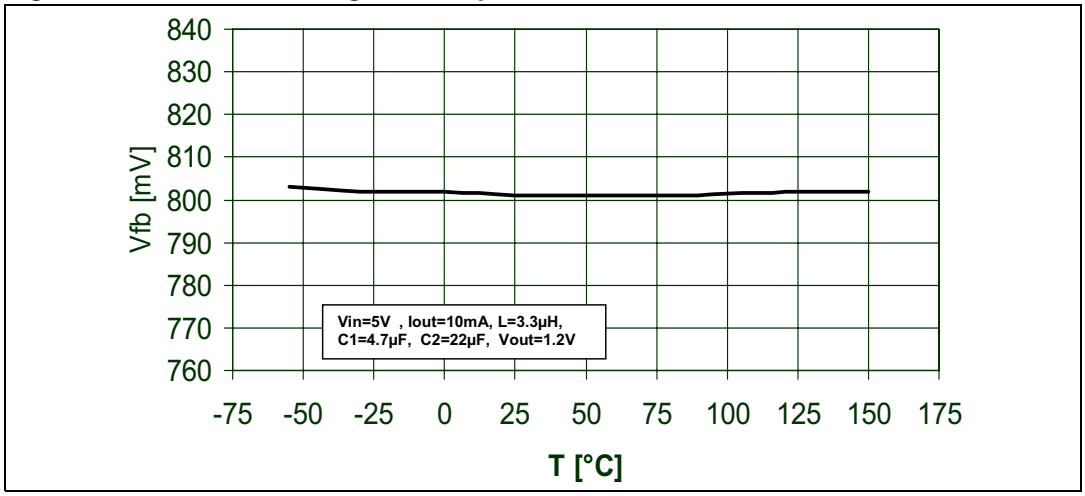


Figure 15. Output voltage vs. input voltage

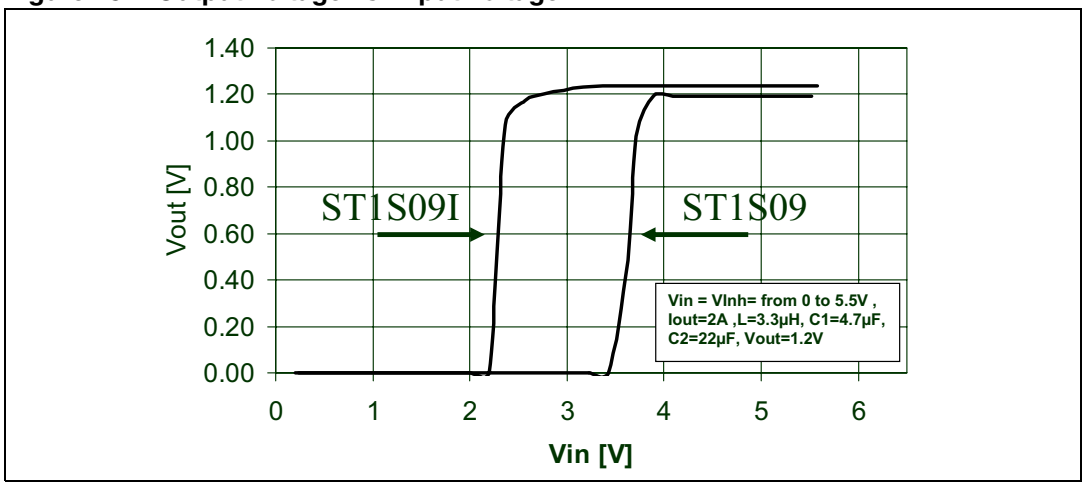


Figure 16. Over voltage protection vs. temperature

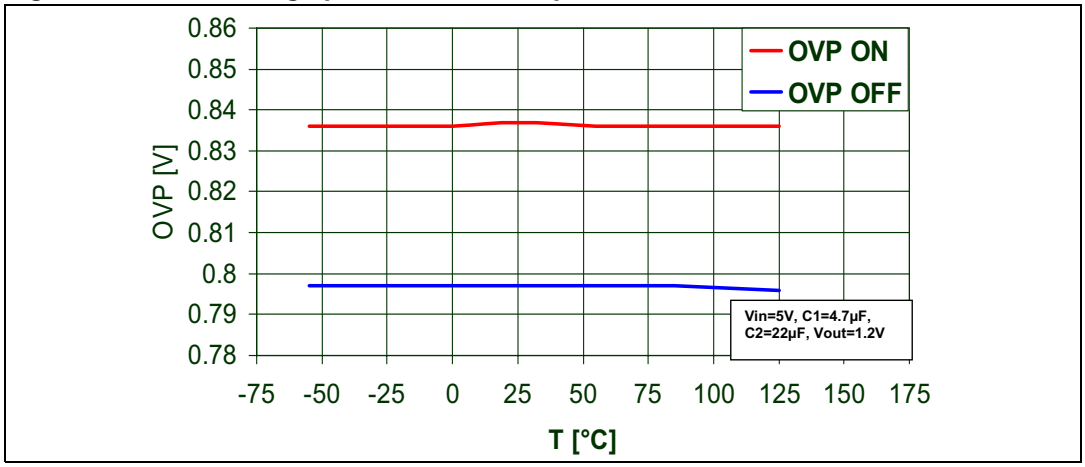


Figure 17. Inhibit voltage vs. temperature

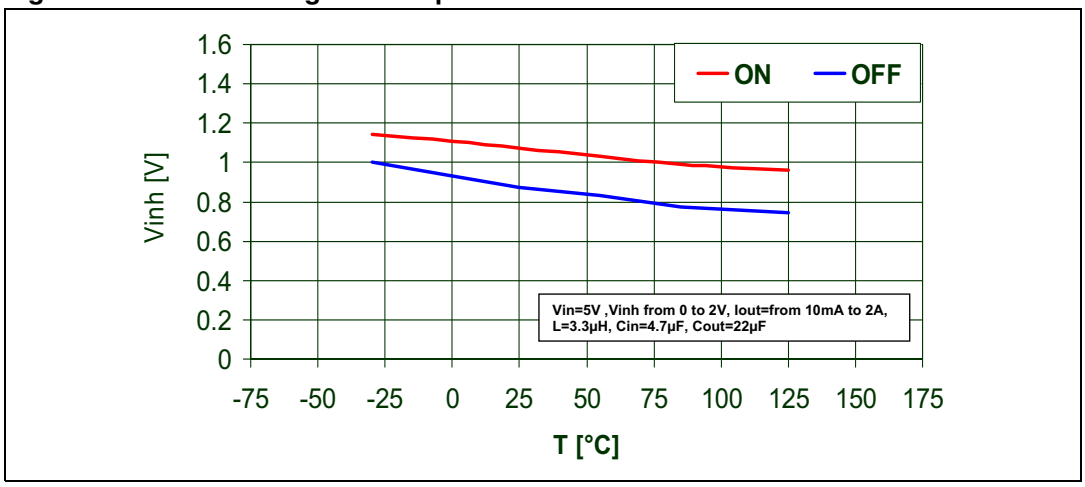


Figure 18. Efficiency vs. output current

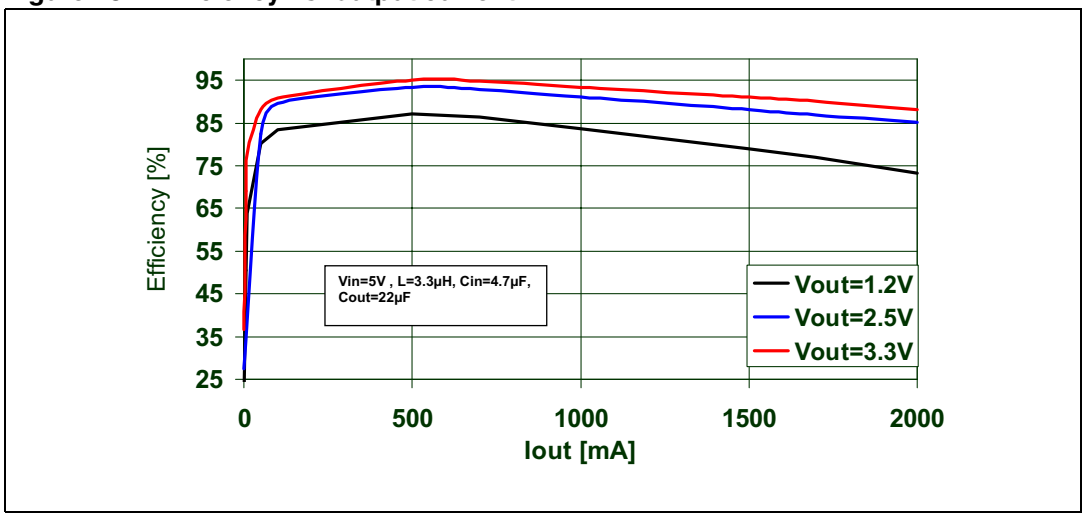


Figure 19. Efficiency vs. output voltage

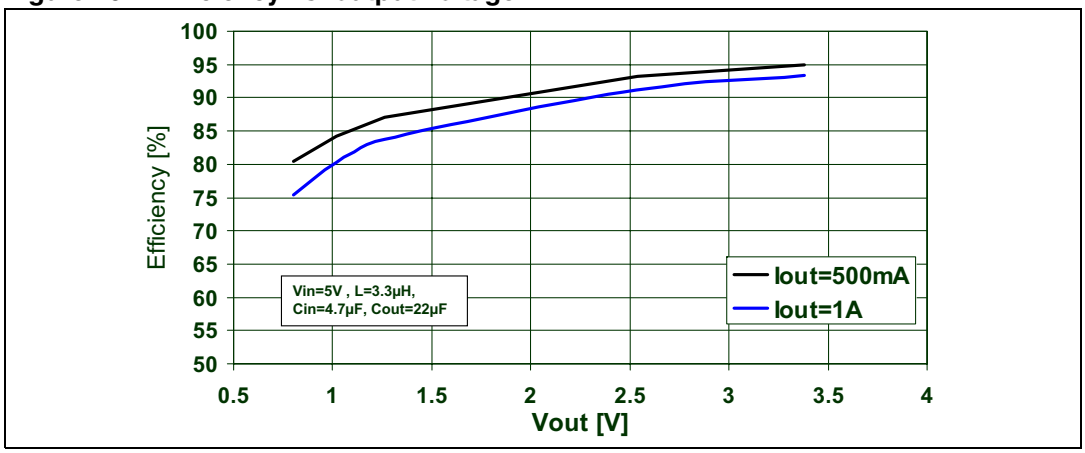
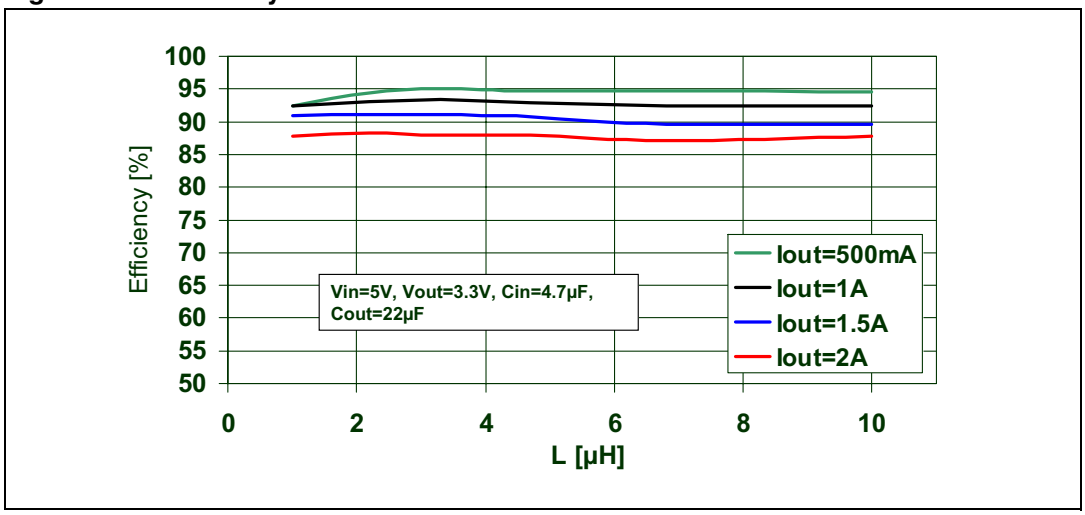


Figure 20. Efficiency vs. inductor



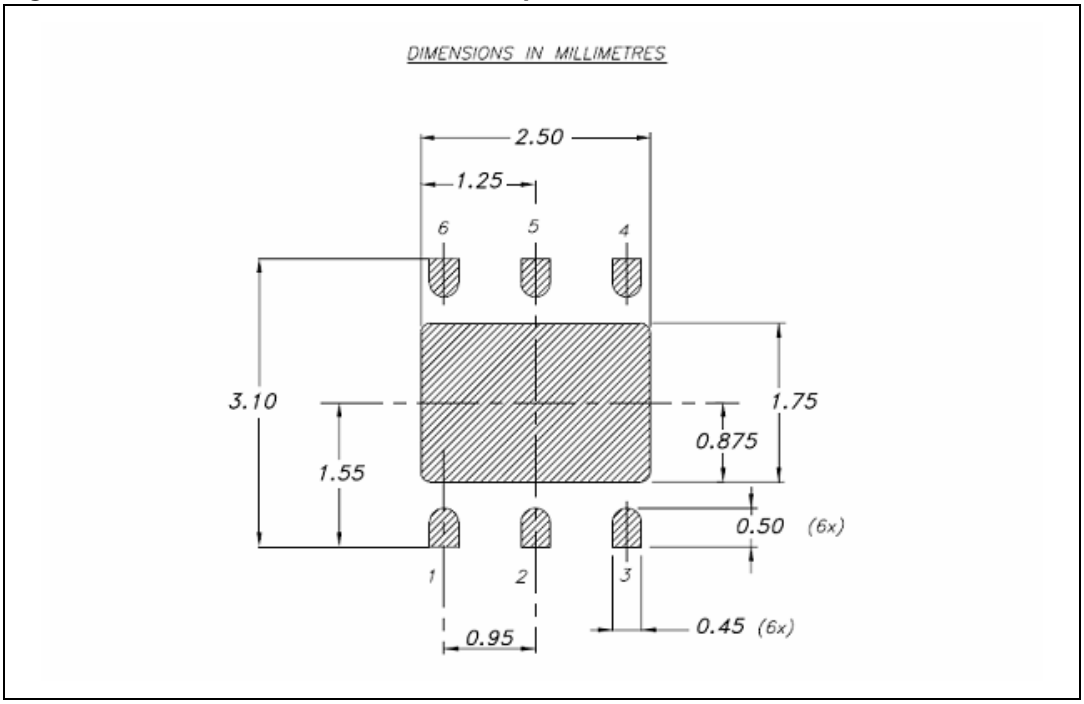
6 Bill of materials

Table 2. BOM with most common components

Name	Value	Material	Manufacturer	Part number
C1	4.7 µF	Ceramic	Murata	GRM21BR61E475KA12B
		Ceramic	TDK	C3216X7R1C475K
C2	22 µF	Ceramic	Murata	GRM32ER61E226KE15B
		Ceramic	TDK	C3225X7R1C226M
C3				Not mounted
D				Not mounted
L1	3.3 µH		TDK	RLF7030T-3R3M4R1
	4.7 µH		CoilTronics	DR73-4R7
R3/R4	120 kΩ			

7 Recommended footprint

Figure 21. DFN6 3x3 recommended footprint



8 Revision history

Table 3. Document revision history

Date	Revision	Changes
17-Sep-2007	1	Initial release
29-Oct-2008	2	Modified: *Section 1.2* and *4.2*
23-Feb-2011	3	Modified: *Table 2 on page 20*