ULTRA- LOW ON RESISTANCE, 6-A DUAL LOAD SWITCH WITH CONTROLLED TURN-ON

FEATURES

- Integrated dual channel load switch
- Input Voltage Range: 0.8V to 5.5V
- Ultra-low ON-Resistance, R_{ON} = 20mΩ per channel
- 6A Maximum Continuous Current per channel
- Low Threshold Control Input
- Adjustable Rise Time
- Quick Output Discharge Transistor
- RoHS Compliant and Halogen Free Product

APPLICATIONS

- Telecom Systems
- Industrial Systems
- Set-Top-Box
- Consumer Electronics
- Notebooks / Netbooks

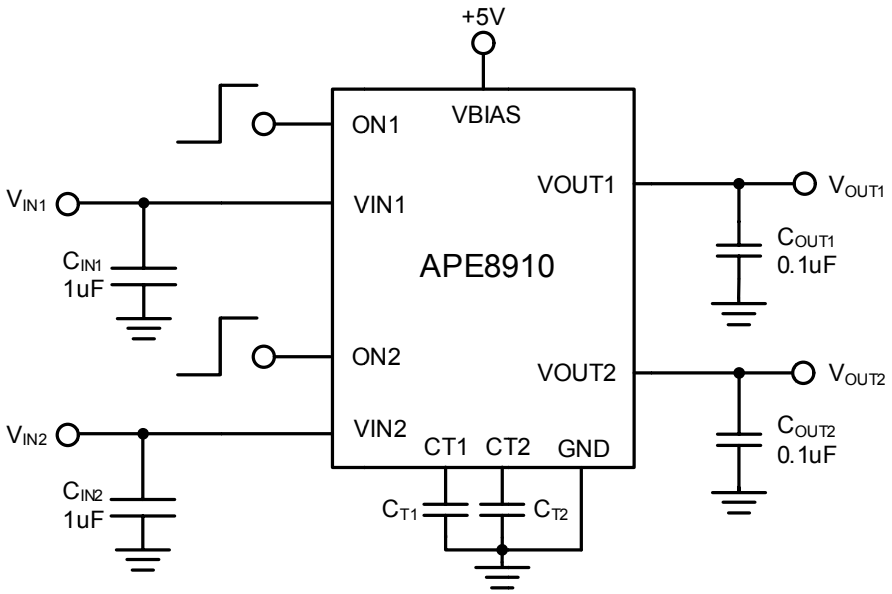
DESCRIPTION

The APE8910 is a small, ultra-low R_{ON} dual load switch with controlled turn on. It contains two N-channel MOSFETs that can operate over an input voltage range of 0.8V to 5.5V and support maximum continuous current up to 6A each. Each load switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

Additional features include a 250Ω on-chip load resistor for output quick discharge when switch is turned off, in order to avoid inrush current, the rise time is adjustable by an external ceramic capacitor on the CTx pin.

The APE8910 is available in an ultra-small, space saving 3mmx2mm 14-pin DFN package with thermal pad.

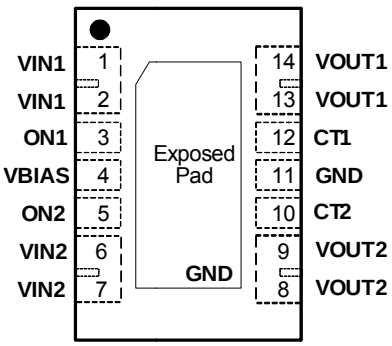
TYPICAL APPLICATION



ORDERING / PACKAGE INFORMATION

APE8910X
└ Package Type
GN3B: DFN 3x2-14L

Top View
DFN3x2-14L



ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

VIN1, VIN2	-0.3V to 6V
VOUT1, VOUT2	VIN+0.3V
VON1, VON2	-0.3V to 6V
VBIAS	-0.3+6V
I_{MAX}	6A
Storage Temperature Range (T_{ST})	-65 to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Ambient ($R\theta_{JA}$)	
DFN-14L (3mmX2mm)	65°C/W

RECOMMENDED OPERATING CONDITIONS

VIN1,2	0.8V to 5.5V
VBIAS	2.5V to 5.5V (VBIAS ≧ VIN)
VON1,2	0V to 5.5V
VOUT1,2	VIN1,2
CIN1,2	≧0.1uF
Junction Temperature (T_J)	125°C
Operating Temperature Range	-40°C to 85°C

ELECTRICAL SPECIFICATIONS

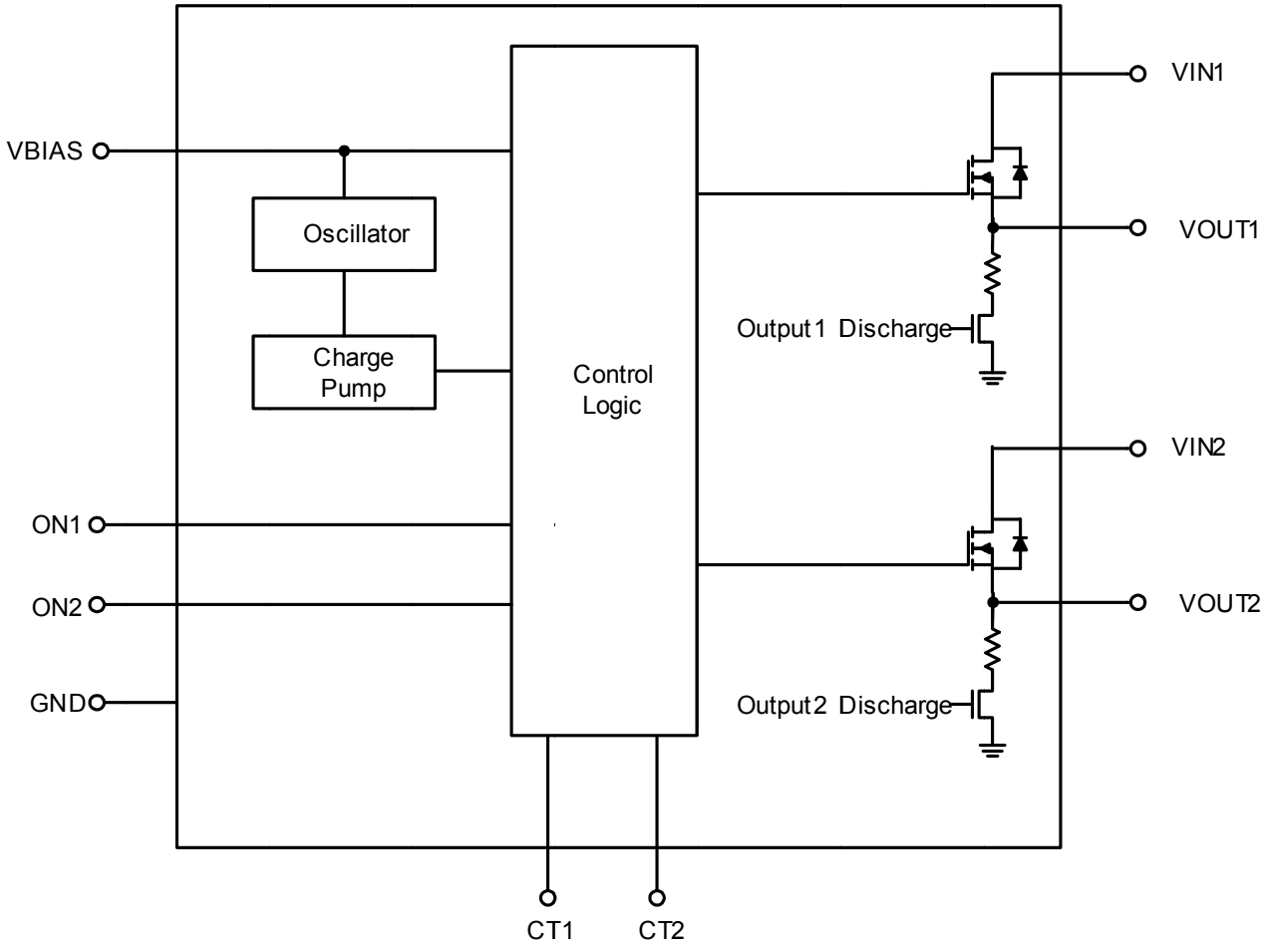
(VIN1, 2=0.8 to 5.5V, VBIAS=5V, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Quiescent Current	I_{BIAS}	VIN1=VIN2=VON1=VON2=5V IOUT1=IOUT2=0A		80	120	uA
Shutdown Current	I_{SD}	VON1=VON2=GND, VOUT1=VOUT2=0			1	uA
ON Resistance (each switch)	R_{ON}	VINx=5V, VBIAS=5V, IOUTx=-200mA, T_A=25°C		20	28	mΩ
		VINx=5V, VBIAS=5V, IOUTx=-200mA, -40°C < T_A < 85°C			35	mΩ
		VINx=3.3V, VBIAS=5V, IOUTx=-200mA, T_A=25°C		20	28	mΩ
		VINx=3.3V, VBIAS=5V, IOUTx=-200mA, -40°C < T_A < 85°C			35	mΩ
		VINx=1.8V, VBIAS=5V, IOUTx=-200mA, T_A=25°C		20	28	mΩ
		VINx=1.8V, VBIAS=5V, IOUTx=-200mA, -40°C < T_A < 85°C			35	mΩ
		VINx=1.5V, VBIAS=5V, IOUTx=-200mA, T_A=25°C		20	28	mΩ
		VINx=1.5V, VBIAS=5V, IOUTx=-200mA, -40°C < T_A < 85°C			35	mΩ
		VINx=1.2V, VBIAS=5V, IOUTx=-200mA, T_A=25°C		20	28	mΩ
		VINx=1.2V, VBIAS=5V, IOUTx=-200mA, -40°C < T_A < 85°C			35	mΩ
		VINx=0.8V, VBIAS=5V, IOUTx=-200mA, T_A=25°C		20	28	mΩ
		VINx=0.8V, VBIAS=5V, IOUTx=-200mA, -40°C < T_A < 85°C			35	mΩ
Output Pull Down Resistance	R_{OPD}	VBIAS=5V, VONx=0V		250	350	Ω
ONx Input Leakage Current	I_{ON}	VONx=5V or GND			1	uA
ONx Logic High	V_{IH}	VBIAS= 2.5V to 5.5V		1.2	5.5	V
ONx Logic Low	V_{IL}	VBIAS= 2.5V to 5.5V		0	0.4	V

PIN DESCRIPTIONS

PIN No.	PIN SYMBOL	PIN DESCRIPTION
1, 2	VIN1	Channel 1 input, bypass this input with a ceramic capacitor to ground.
3	ON1	Channel 1 enable control input, active high. Do not leave floating.
4	VBIAS	5V bias voltage.
5	ON2	Channel 2 enable control input, active high. Do not leave floating.
6,7	VIN2	Channel 2 input, bypass this input with a ceramic capacitor to ground.
8,9	VOUT2	Channel 2 output.
10	CT2	A capacitor to ground set the rise time of VOUT2.
11	GND	Ground.
12	CT1	A capacitor to ground set the rise time of VOUT1.
13,14	VOUT1	Channel 1 output.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

VBIAS=5V, VIN1=VIN2, ON1=ON2, I_{OUTX}=0A, CTx=1nF, C_{INX}=1μF, C_{OUTX}=0.1μF,

ch1:ONx, ch2:VOUT1, ch3: VOUT2

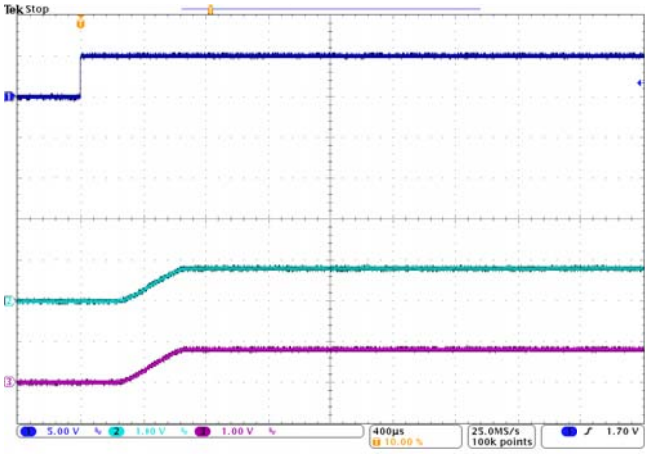


Fig.1 Turn-on Response, VINx=0.8V

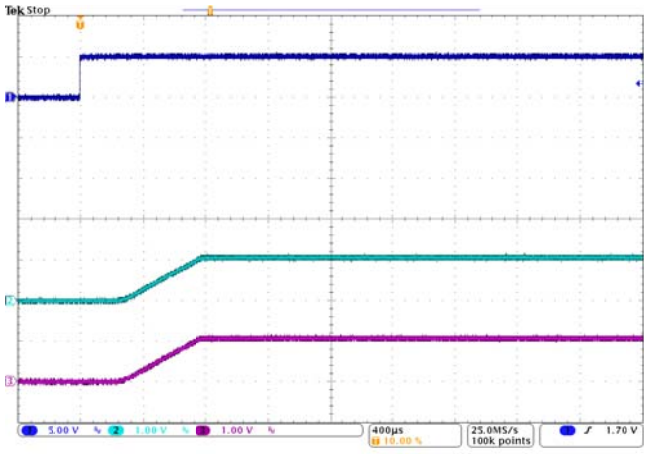


Fig.2 Turn-on Response, VINx=1.05V

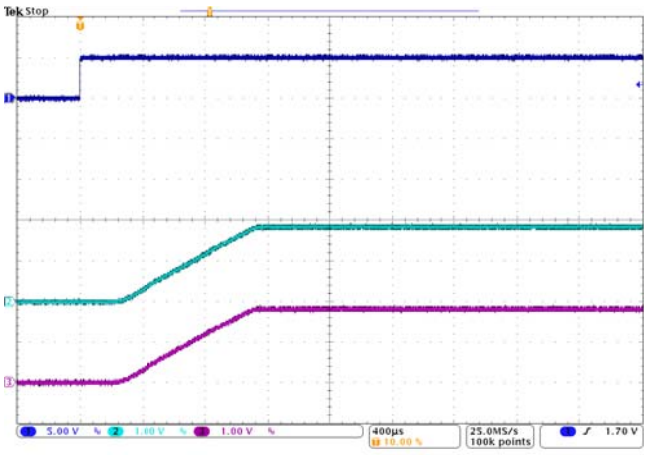


Fig.3 Turn-on Response, VINx=1.8V

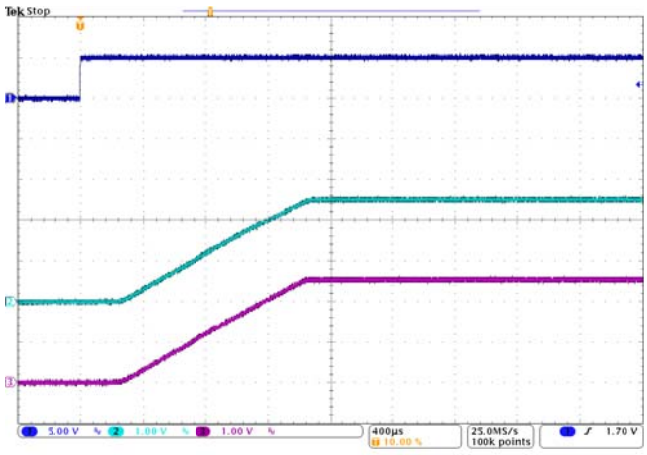


Fig.4 Turn-on Response, VINx=2.5V

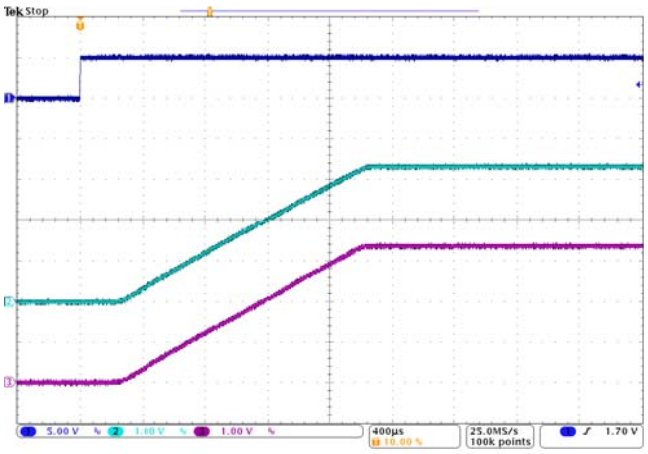


Fig.5 Turn-on Response, VINx=3.3V

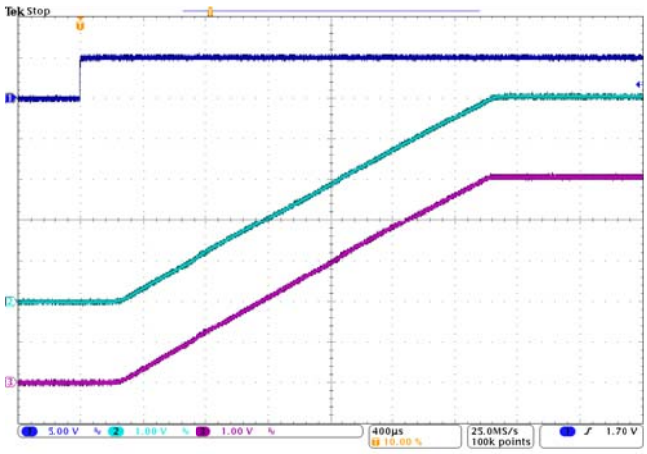


Fig.6 Turn-on Response, VINx=5.0V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

VBIAS=5V, VIN1=VIN2, ON1=ON2, I_{OUTX}=0A, CTx=1nF, C_{INX}=1μF, C_{OUTX}=0.1μF,

ch1:ONx, ch2:VOUT1, ch3: VOUT2

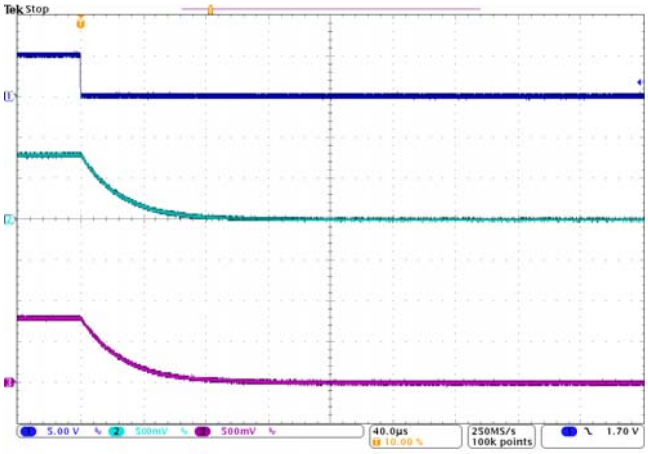


Fig.7 Turn-off Response, VIN=0.8V

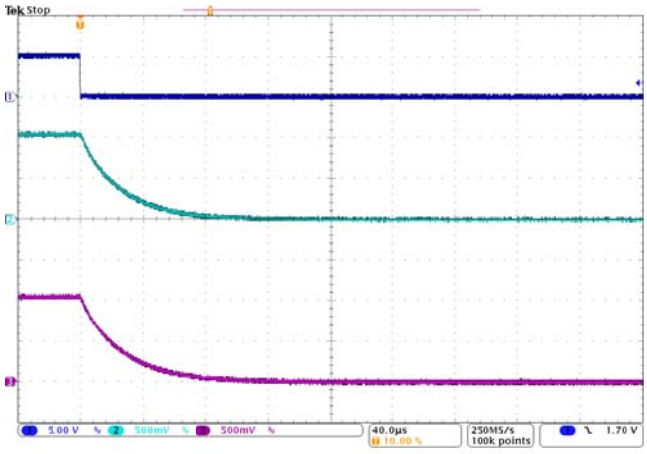


Fig.8 Turn-off Response, VIN=1.05V

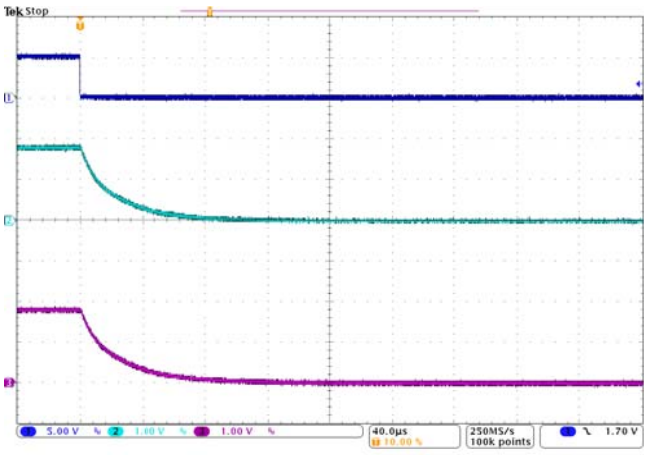


Fig.9 Turn-off Response, VIN=1.8V

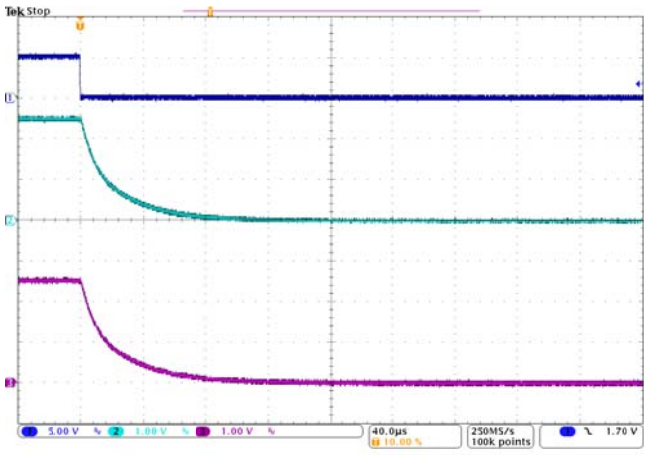


Fig.10 Turn-off Response, VIN=2.5V

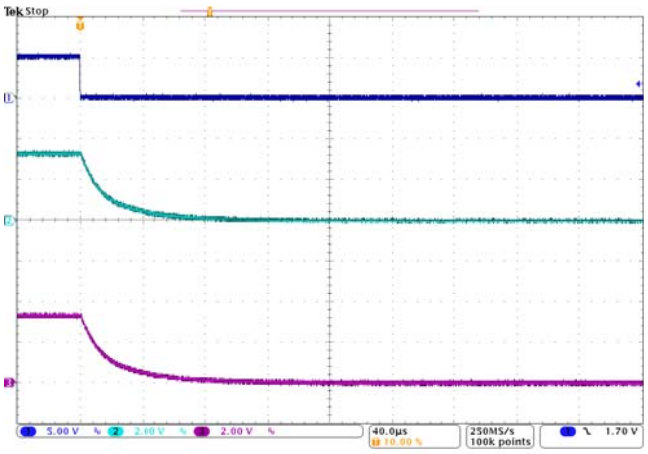


Fig.11 Turn-off Response, VIN=3.3V

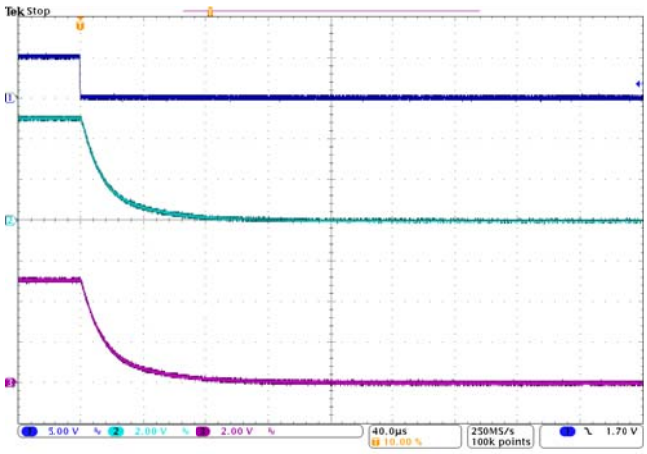


Fig.12 Turn-off Response, VIN=5.0V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

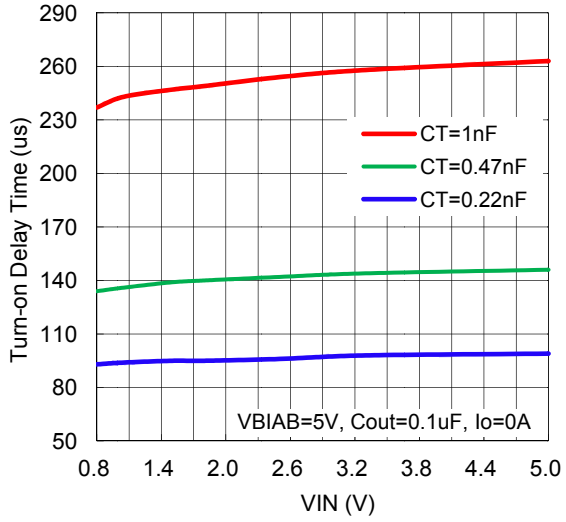


Fig.13 t_{D-ON} vs. VIN

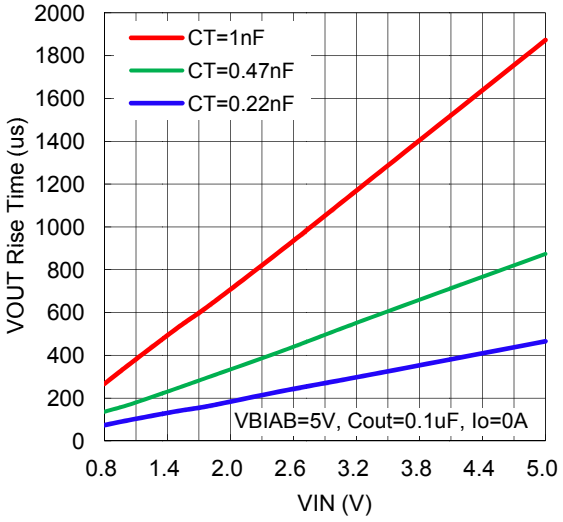


Fig.14 t_R vs. VIN

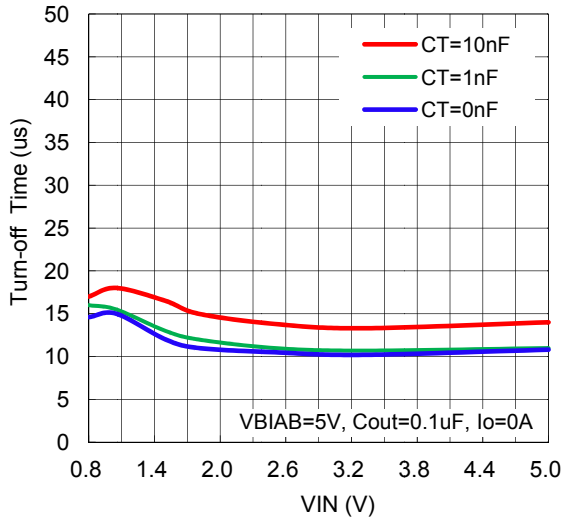


Fig.15 t_{OFF} vs. VIN

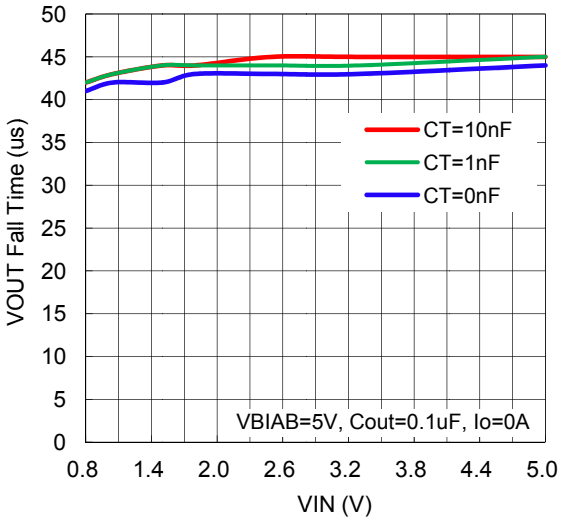


Fig.16 t_F vs. VIN

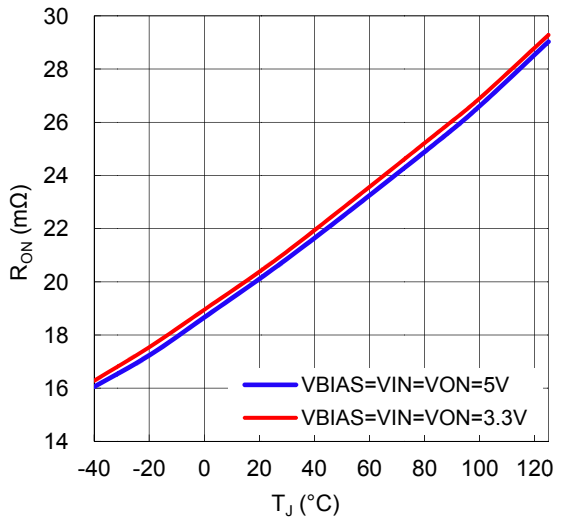


Fig.17 R_{ON} vs. Temperature

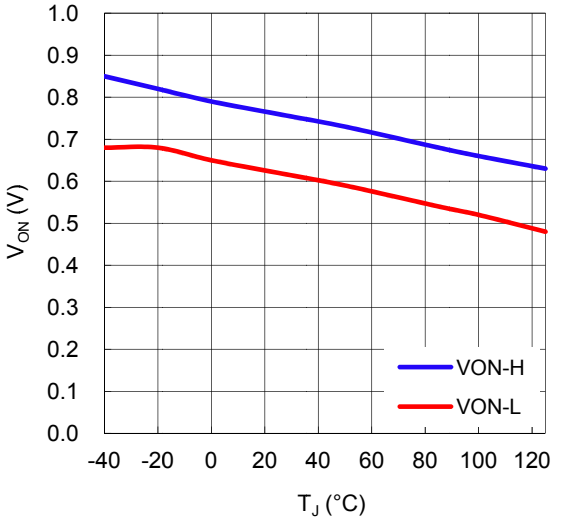


Fig.18 ON Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

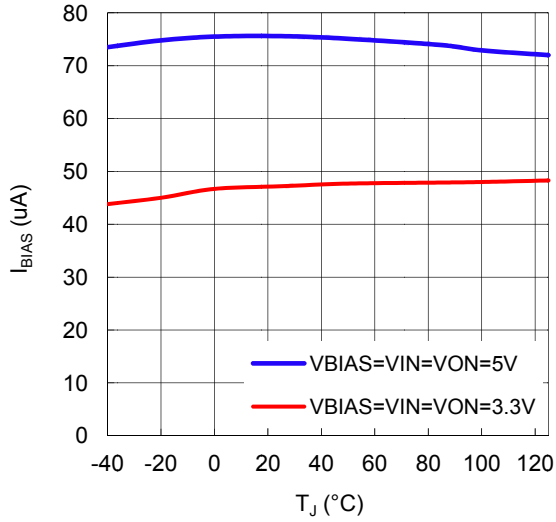


Fig.19 Quiescent Current (VBIAS) vs. Temperature

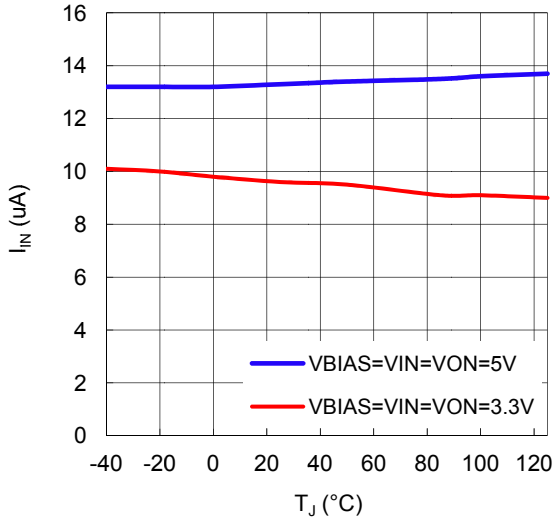


Fig.20 Quiescent Current (VIN) vs. Temperature

APPLICATION INFORMATION

On/Off Control

The load switch is controlled by the ON pin. The ONx pin is active high and has a low threshold making it capable of interfacing with low voltage signals. The ONx pin can be used with standard 1.2V, 1.8V, 2.5V or 3.3V GPIO logic threshold. Do not leave the ONx pin float.

The Figure 21 show the VOUTx turn-on/off waveform.

t_D: VOUT Turn On Delay Time

ton: VOUT Turn On Time

t_R: VOUT Rise Time

t_{OFF}: VOUT Turn Off Time

t_F: VOUT Fall Time

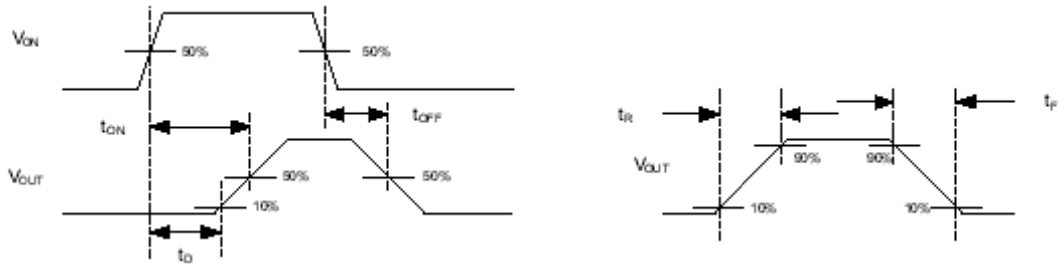


Fig.21 ON/OFF Waveform

Output Rise Time Control

The rise time of each VOUTx is adjustable by an external capacitor on the CTx pin. The rise time shows on below Table 1 are typical measured value. Please refer it for determined rise time.

CT (nF)	Rise Time, t_R (μs),10%~90%, C_{OUT}=0.1μF,C_{IN}=1uF							
	VIN=0.8V	VIN=1.05V	VIN=1.2V	VIN=1.5V	VIN=1.8V	VIN=2.5V	VIN=3.3V	VIN=5V
0	27	31	34	38	40	48	59	75
0.22	72	93	107	131	158	220	284	418
0.47	126	159	178	233	280	400	520	776
1	250	327	378	485	584	780	1045	1657
2.2	509	725	827	1027	1235	1777	2391	3593
4.7	1012	1387	1699	1898	2269	3451	4670	7418
10	2008	2865	3425	4328	5203	7491	10142	15409

<Table 1>

APPLICATION INFORMATION (Continued)

Input Capacitor

An input capacitor is recommended to be placed between VINx and GND to limit the voltage drop on the input supply during high current application.

Output Capacitor

Setting a C_{IN} greater than the C_{OUT} is highly recommended. Since the internal body diode is in the NMOS switch, this prevents the current flows through the body diode from VOUTx to VINx when the system supply is removed.

Layout Considerations

The Figure 22 shows the reference layout for APE8910. Below lists help start layout.

1. The current loop of two load switch should be separated and symmetrized to each other.
2. Keep the high current paths (VIN, VOUT and GND; blue circle) wide and short to obtain the best effect.
3. The input and output capacitors should be close to the device as possible to minimize the parasitic trace inductances.
4. Place the thermal vias under the exposed pad of the device (green circle). This help for thermal diffusion away from the device.

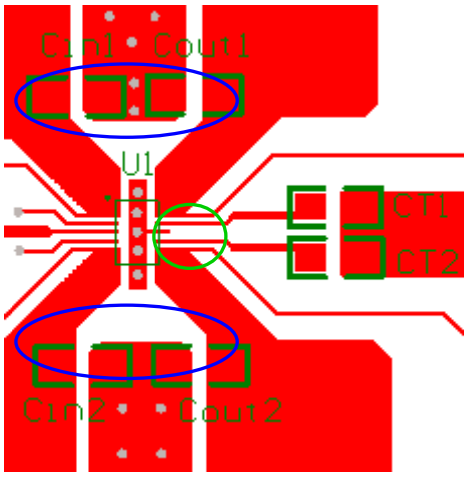


Fig.22 APE8910 Reference Layout

MARKING INFORMATION

DFN 3x2-14L