GENERAL DESCRIPTION

The MC3610 is an ultra-low power, low-noise, integrated digital output 3-axis accelerometer with a feature set optimized for wearables and consumer product motion sensing. Applications include wearable consumer products, IoT devices, user interface control, gaming motion input, electronic compass tilt compensation for cell phones, game controllers, remote controls and portable media products.

Low noise and low power are inherent in the monolithic fabrication approach, where the MEMS accelerometer is integrated in a single-chip with the electronics integrated circuit.

In the MC3610 the internal sample rate can be set from 14 to 370 samples / second. Specific tap or sample acquisition conditions can trigger an interrupt to a remote MCU. Alternatively, the device supports the reading of sample and event status via polling.

FEATURES

Range, Sampling & Power

- ±2,4,8,12 or 16g ranges
- 8, 10 or 12-bit resolution with FIFO
  - 14-bit single samples
- 14 - 370 samples/sec
- Ultra-Low Power with FIFO
  - 0.6 µA typical sniff current
  - 5 µA typical current @ 50Hz
  - 14 µA @ 370Hz

Simple System Integration

- I2C interface, up to 400 kHz
- SPI Interface, up to 2 MHz
- 2 × 2 × 0.94 mm 12-pin package
- Single-chip 3D silicon MEMS
- Low noise to 2.3mgRMS @ 53Hz

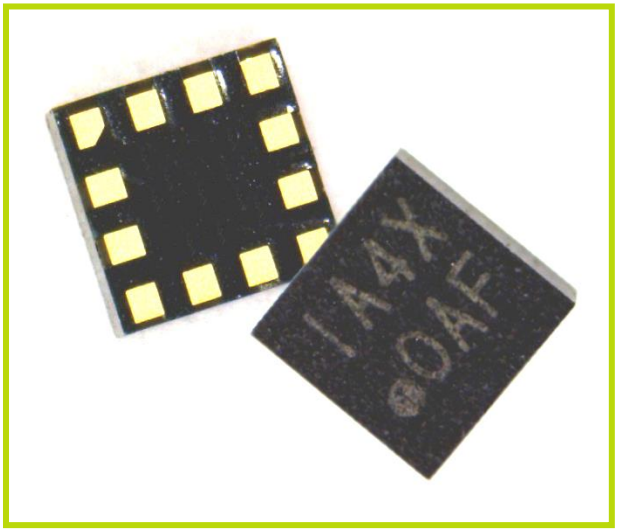


TABLE OF CONTENTS

1 ORDER INFORMATION

Part Number	Resolution	Order Number	Package	Shipping
MC3610	8 to 14-bit	MC3610	VLGA-12	Tape & Reel, 5Ku

Table 1. Order Information

2 FUNCTIONAL BLOCK DIAGRAM

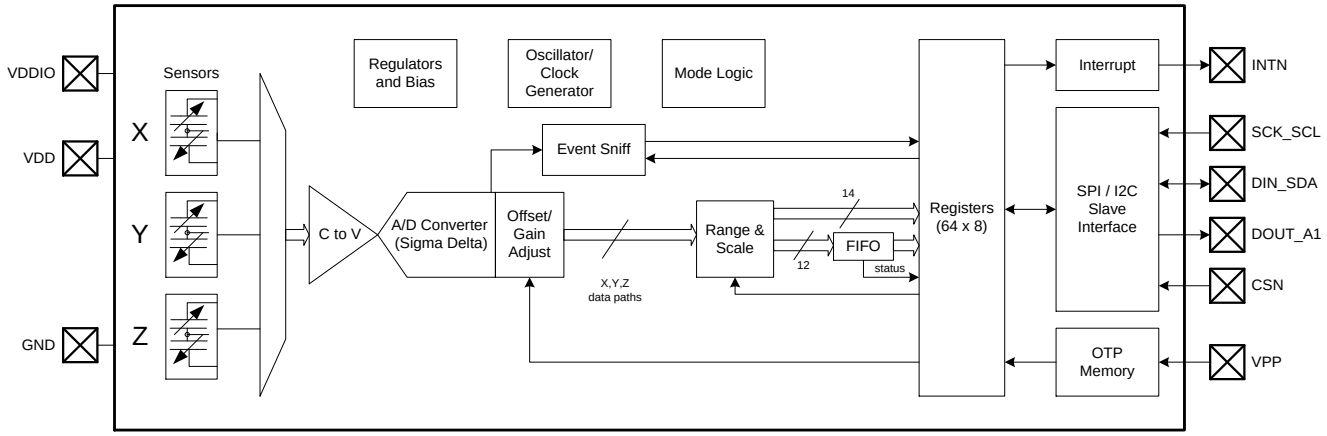
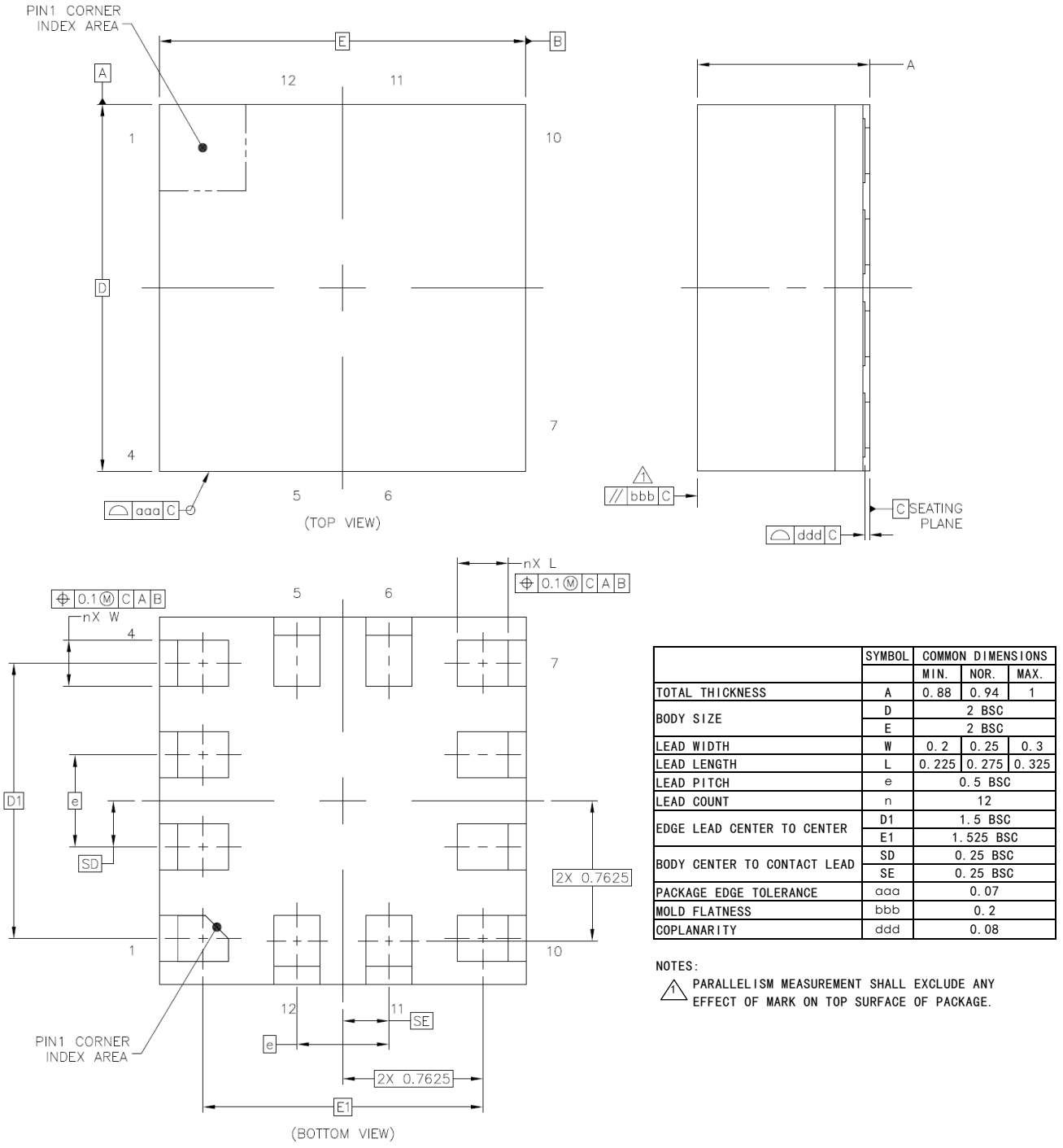


Figure 1. Block Diagram

3 PACKAGING AND PIN DESCRIPTION

3.1 PACKAGE OUTLINE



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	0.88	0.94	1
BODY SIZE	D	2 BSC		
	E	2 BSC		
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.225	0.275	0.325
LEAD PITCH	e	0.5 BSC		
LEAD COUNT	n	12		
EDGE LEAD CENTER TO CENTER	D1	1.5 BSC		
	E1	1.525 BSC		
BODY CENTER TO CONTACT LEAD	SD	0.25 BSC		
	SE	0.25 BSC		
PACKAGE EDGE TOLERANCE	aaa	0.07		
MOLD FLATNESS	bbb	0.2		
COPLANARITY	ddd	0.08		

NOTES:
1. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 2. Package Outline and Mechanical Dimensions

3.2 Package Orientation

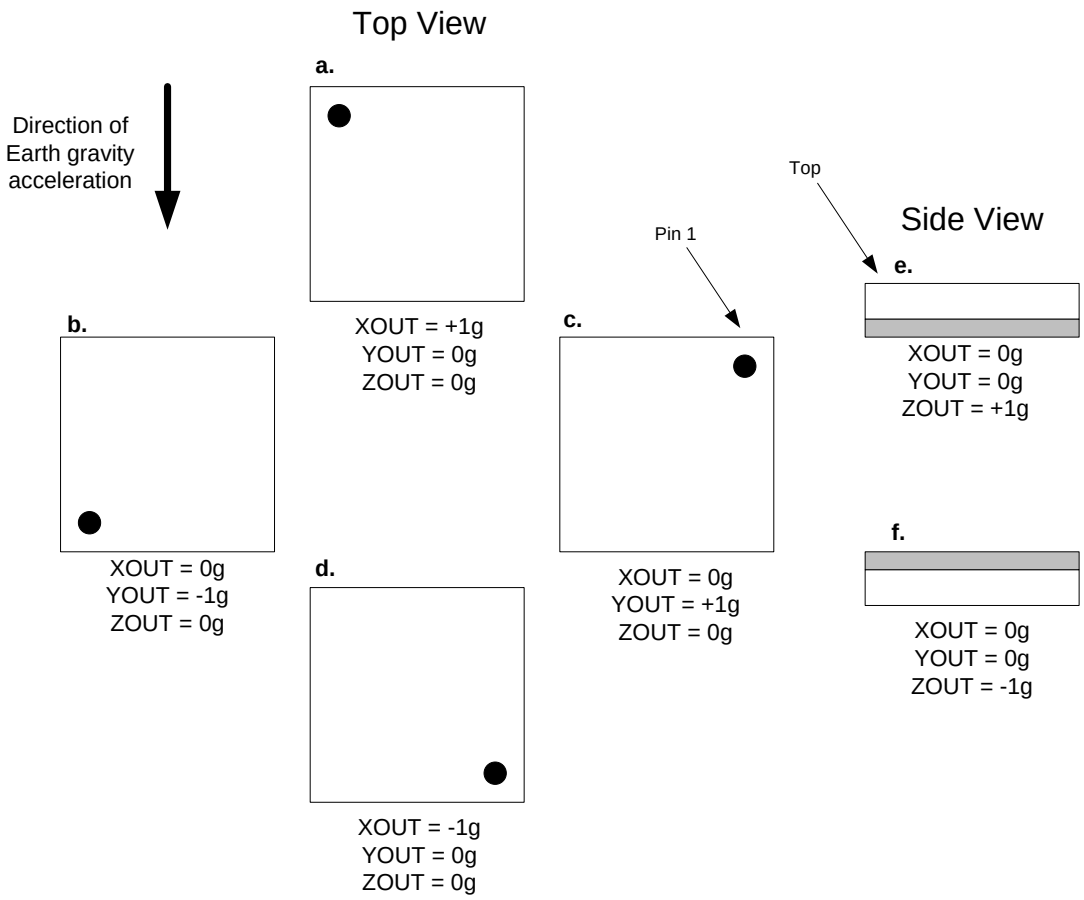


Figure 3. Package Orientation

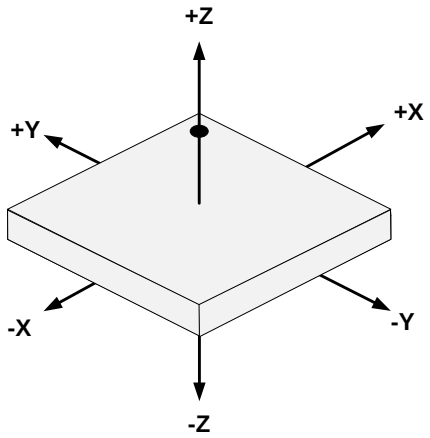


Figure 4. Package Axis Reference

3.3 Pin Description

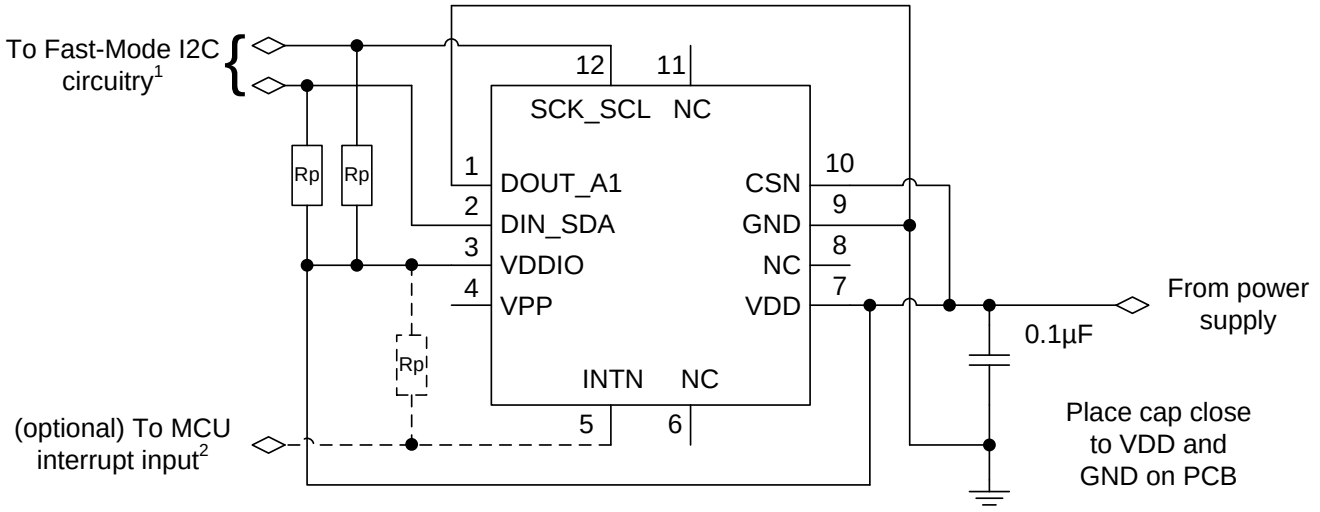
Pin	Name	Function
1	DOUT_A1	SPI data output I2C address bit 1
2	DIN_SDA [1]	SPI data In I2C serial data input/output
3	VDDIO	Power supply for interface
4	VPP	Connect to GND
5	INTN [2]	Interrupt active LOW [3]
6	NC	No connect
7	VDD	Power supply for internal
8	NC	No connect
9	GND	Ground
10	CSN	SPI chip select
11	NC	No connect
12	SCK_SCL [1]	SPI Clock I2C serial clock input

Table 2. Pin Description

Notes:

1) This pin requires a pull-up resistor, typically 4.7kΩ to pin VDDIO. Refer to I2C Specification for Fast-Mode devices. Higher resistance values can be used (typically done to reduce current leakage) but such applications are outside the scope of this datasheet.
2) This pin can be configured by software to operate either as an open-drain output or push-pull output. If set to open-drain, then it requires a pull-up resistor, typically 4.7kΩ to pin VDDIO.
3) INTN pin polarity is programmable in the (0x17) Interrupt Control Register.

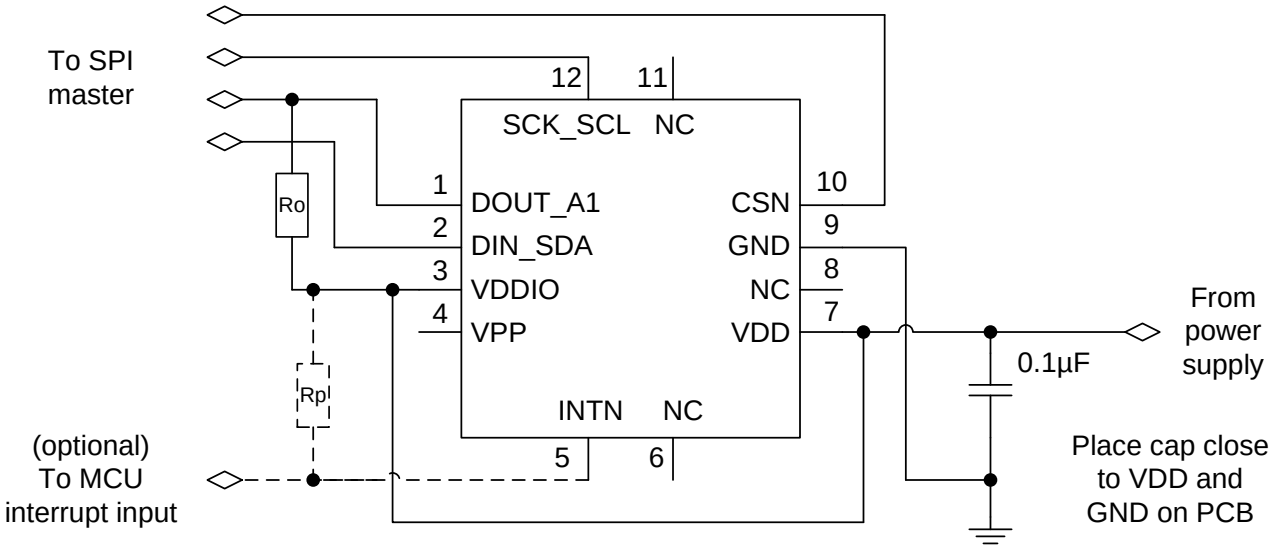
3.4 Typical Application Circuits



NOTE[1]: Rp are typically 4.7kΩ pullup resistors to VDDIO, per I2C specification. When VDDIO is powered down, DIN_SDA and SCK_SCL will be driven low by internal ESD diodes.
NOTE[2]: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

Figure 5. Typical I2C Application Circuit

In typical applications, the interface power supply may contain significant noise from external sources and other circuits which should be kept away from the device. Therefore, for some applications a lower-noise power supply might be desirable to power the device.

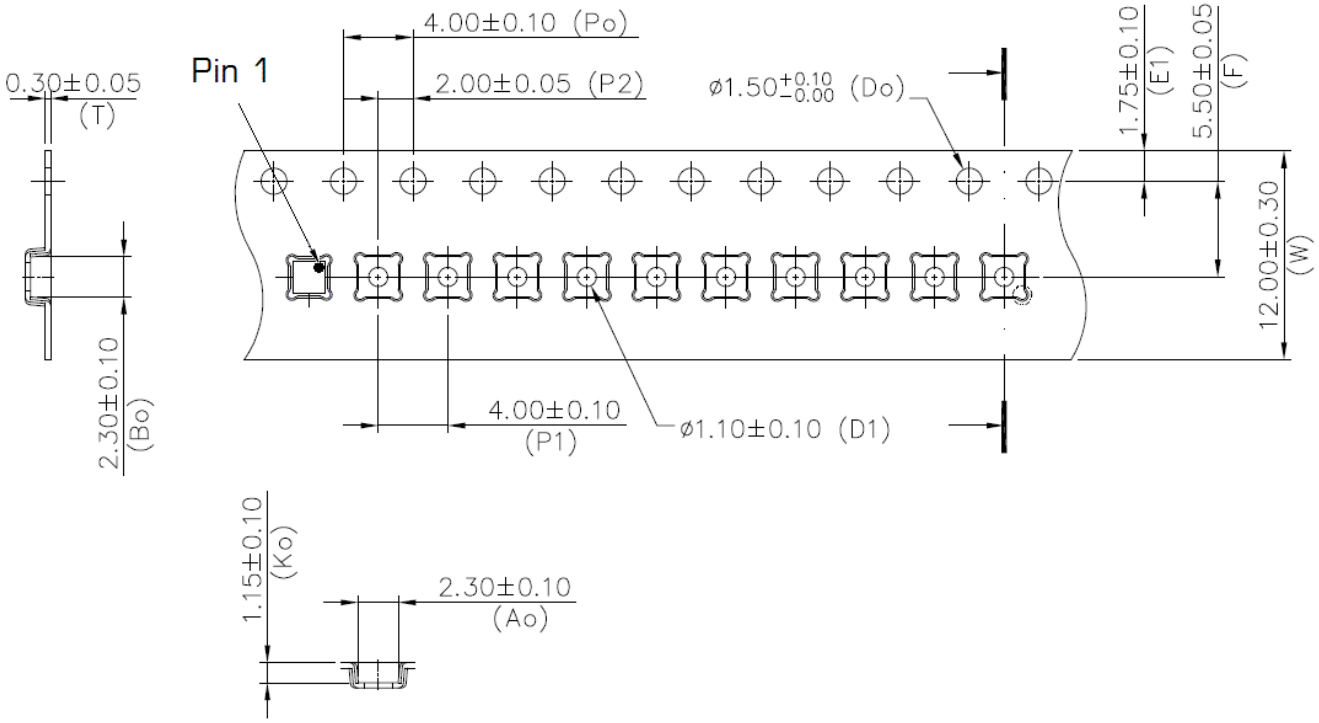


NOTE Rp: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.
NOTE Ro: DOUT_A1 requires a pullup depending upon SPI speed: 2MHz ~ 1KΩ. 1MHz ~ 4.7KΩ.

Figure 6. Typical SPI Application Circuit

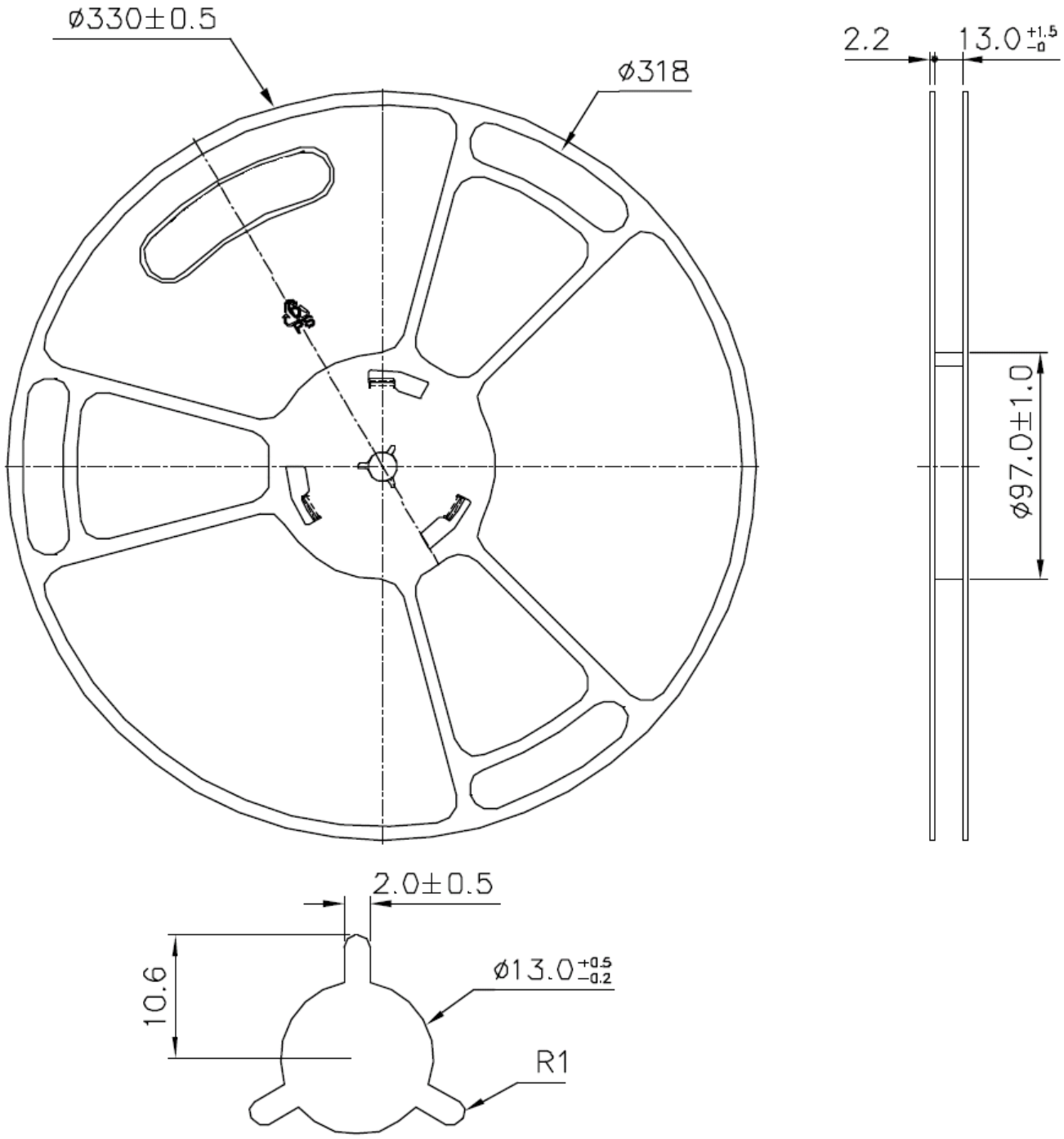
3.5 Tape and Reel

Devices are shipped in reels, in standard cardboard box packaging. See Figure 7. MC3610 Tape Dimensions and Figure 8. MC3610 Reel Dimensions.



- Dimensions in mm.
- 10 sprocket hole pitch cumulative tolerance ±0.2
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 7. MC3610 Tape Dimensions



- Dimensions in mm.

Figure 8. MC3610 Reel Dimensions

4 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Parameters exceeding the Absolute Maximum Ratings may permanently damage the device.

Rating	Symbol	Minimum / Maximum Value	Unit
Supply Voltages	Pins VDD, VDDIO	-0.3 / +3.6	V
Acceleration, any axis, 100 µs	g_{MAX}	10000	g
Ambient operating temperature	T_{OP}	-40 / +85	^{0}C
Storage temperature	T_{STG}	-40 / +125	^{0}C
ESD human body model	HBM	± 2000	V
Input voltage to non-power pin	Pins CSN, DIN_SDA, DOUT_A1, INTN, and SCK_SCL	-0.3 / (VDD + 0.3) or 3.6 whichever is lower	V

Table 3. Absolute Maximum Ratings

4.2 Sensor Characteristics

VDD = 1.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Acceleration range	Resolution and range set in the (0x15) Range and Resolution Control Register		±2 ±4 ±8 ±12 ±16		g
Sensitivity	Depends on settings in the (0x15) Range and Resolution Control Register	8		4096	LSB/g
Sensitivity Temperature Coefficient [1]			0.15		%/^{0}C
Zero-g Offset	Post-board mount		± 40		mg
Zero-g Offset Temperature Coefficient [1]			± 1		mg/^{0}C
Noise Density [1]	Ultra-Low Power 46Hz, Avg X&Y&Z: Low Power, 50Hz, Avg X&Y&Z: Precision, 53Hz, Avg X&Y&Z:		9.8 4.4 2.3		mg RMS
Nonlinearity [1]			1		% FS
Cross-axis Sensitivity [1]	Between any two axes		2		%

Table 4. Sensor Characteristics

[1] Values are based on device characterization, not tested in production.

4.3 Electrical and Timing Characteristics

4.3.1 ELECTRICAL POWER AND INTERNAL CHARACTERISTICS

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Internal voltage [2]	Pin VDD Rise-time < 40mSec	VDD	1.7	1.8	3.6	V
I/O voltage	Pin VDDIO Rise-time < 40mSec	VDDIO	1.7	1.8	3.6	V
Sample Rate Tolerance [3]		Tclock	-30	± 5	30	%

Test condition: VDD = 1.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Sleep current		I_{ddslp}		0.3		µA
Sniff current		I_{ddsnf}		0.7		µA
Selected wake supply current (see (0x11) Rate Register 1 for more options)	Ultra-Low Power, 11Hz, FIFO off / on:	$I_{dd11ulp}$		0.7 / 0.9		µA
	Precision, 14Hz, FIFO off / on:	I_{dd14p}		3 / 5		
	Ultra-Low Power, 23Hz, FIFO off / on:	$I_{dd23ulp}$		0.9 / 1.3		
	Precision, 26Hz, FIFO off / on:	I_{dd26p}		6 / 9		
	Low Power, 50Hz, FIFO off / on:	I_{dd50lp}		3 / 5		
	Low Power, 100Hz, FIFO off / on:	$I_{dd100lp}$		6 / 9		
	Ultra-Low Power, 190Hz, FIFO off / on:	$I_{dd190ulp}$		7 / 11		
	Ultra-Low Power, 370Hz, FIFO off / on:	$I_{dd370ulp}$		9 / 14		
Pad Leakage	Per I/O pad	I_{pad}		0.01		µA

Table 5. Electrical Characteristics – Voltage and Current

[2] Min and Max limits are hard limits without additional tolerance.

[3] Values are based on device characterization, not tested in production.

4.3.2 ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
LOW level input voltage	VIL	-0.5	0.3*VDD	V
HIGH level input voltage	VIH	0.7*VDD	-	V
Hysteresis of Schmitt trigger inputs	Vhys	0.05*VDD	-	V
Output voltage, pin INTN, Iol ≤ 2 mA	Vol Voh	0 0	0.4 0.9*VDD	V V
Output voltage, pin DIN_SDA (open drain), Iol ≤ 1 mA	Vols	-	0.1*VDD	V
Input current, pins DIN_SDA and SCK_SCL (input voltage between 0.1*VDD and 0.9*VDD max)	Ii	-10	10	µA
Capacitance, pins DIN_SDA and SCK_SCL [4]	Ci	-	10	pF

Table 6. Electrical Characteristics – Interface

NOTES:

- If multiple slaves are connected to the I2C signals in addition to this device, only 1 pull-up resistor on each of SDA and SCL should exist. Also, care must be taken to not violate the I2C specification for capacitive loading.
- When pin VDDIO is not powered and set to 0V, INTN, DIN_SDA and SCK_SCL will be held to VDDIO plus the forward voltage of the internal static protection diodes, typically about 0.6V.
- When pin VDDIO is disconnected from power or ground (e.g. Hi-Z), the device may become inadvertently powered up through the ESD diodes present on other powered signals.

[4] Values are based on device characterization, not tested in production.

4.3.3 I2C TIMING CHARACTERISTICS

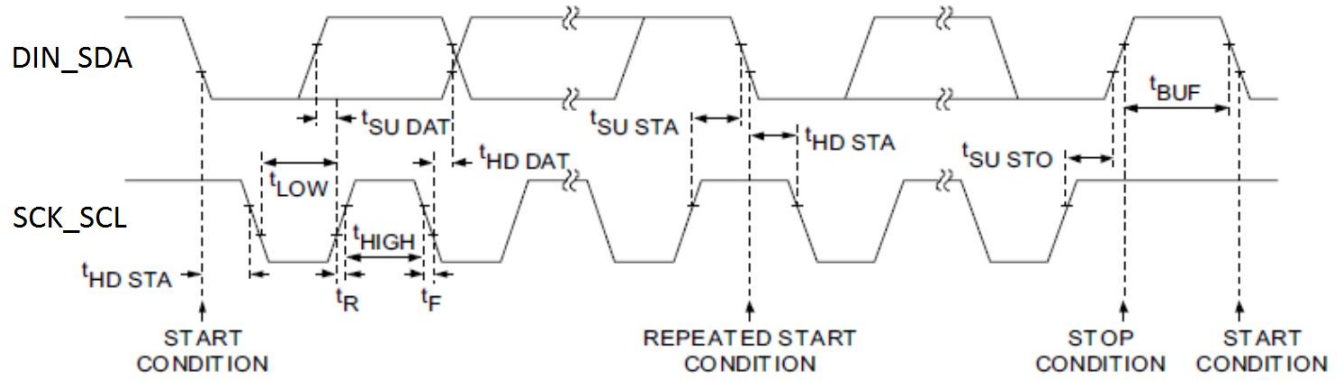


Figure 9. I2C Interface Timing

Parameter	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time	5.0	-	-	-	µs
$t_{SU;DAT}$	Data set-up time	250	-	100	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a STOP and START	4.7	-	1.3	-	µs

Table 7. I2C Timing Characteristics

NOTE: Values are based on I2C Specification requirements, not tested in production.

See also Section 7.4 I2C Message Format.

4.3.4 SPI TIMING CHARACTERISTICS

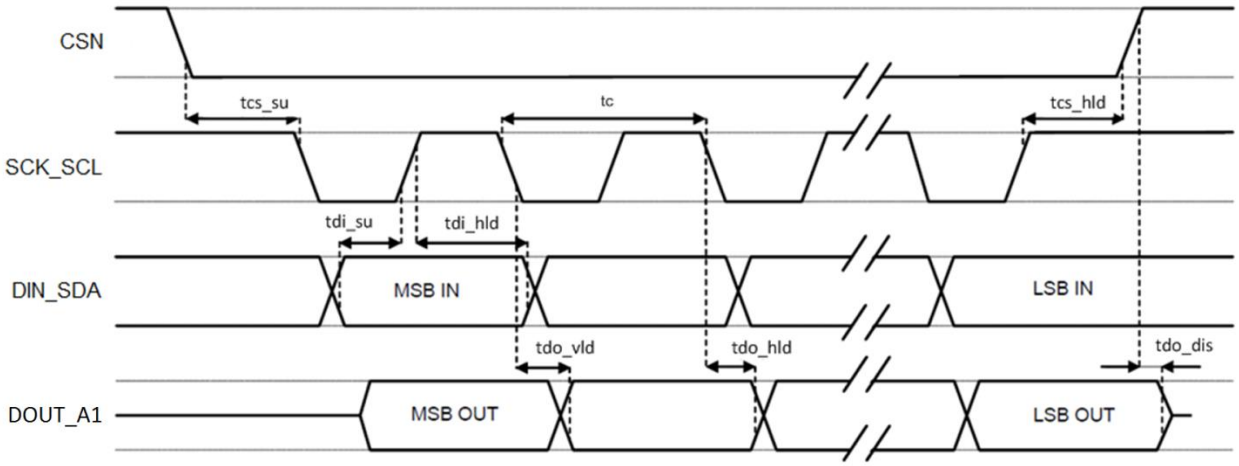


Figure 10. SPI Interface Timing Waveform

Symbol	Parameter	Value		Units
		Min	Max	
tc	SPI SCK_SCL Clock Cycle	500		ns
fc	SPI SCK_SCL Clock Frequency		2	MHz
tcs_su	SPI CSN Setup Time	6		ns
tcs_hld	SPI CSN Hold Time	8		ns
tdi_su	SPI DIN_SDA Input Setup Time	5		ns
tdi_hld	SPI DIN_SDA Input Hold Time	15		ns
tdo_vld	SPI DOUT_A1 Valid Output Time		50	ns
tdo_hld	SPI DOUT_A1 Output Hold Time	9		ns
tdo_dis	SPI DOUT_A1 Output Disable Time		50	ns

Table 8. SPI Interface Timing Parameters

5 GENERAL OPERATION

The device supports the reading of samples and device status upon interrupt or via polling. It contains a 12-bit 32 sample FIFO with programmable watermark. The device is internally clocked but also includes a manual trigger mode. It can be put into several low power modes, depending upon the desired sensing application. The device can run in full-featured mode from its fast internal clock or from a slower heartbeat clock, with limited functionality and at lower power. The device can connect as a slave to either a SPI (2 MHz) or I2C master (400 KHz).

5.1 SENSOR SAMPLING

X, Y and Z accelerometer data is stored in registers XOUT, YOUT, and ZOUT registers. The data is represented as 2's complement format.

The desired resolution and full scale acceleration range are set in the RANGE_C register.

5.2 OFFSET AND GAIN CALIBRATION

The default digital offset and gain calibration data can be read from the device, if necessary, in order to reduce the effects of post-assembly influences and stresses which may cause the sensor readings to be offset from their factory values.

5.3 RESET

The device can be completely reset via an I2C or SPI instruction. Writing register 0x24 with 0x40 (bit 6) causes a power-on reset operation to execute. No attempt should be made to access registers within 1mSec after issuing this operation. The device must be placed in STANDBY mode before executing the reset.

The pin DOUT_A1 is sampled for the purposes of setting the I2C device address after this reset operation.

5.4 RELOAD

The device registers can be reloaded from OTP via an I2C or SPI instruction. Writing register 0x24 with 0x80 (bit 7) causes a reload operation to execute. The contents of OTP are reloaded into the register set. However any non-loaded register locations will not be affected. No attempt should be made to access registers within 1mSec after issuing this operation. The device must be placed in STANDBY mode before executing the reset.

The pin DOUT_A1 is sampled for the purposes of setting the I2C device address after this reload operation.

5.5 Operational Modes

The device has various modes of operation as described below:

Mode	Description and Comments
SLEEP	SLEEP is the lowest power mode. The DVDD regulator is enabled, but there are no clock activity, and much of the chip is disabled. The SLEEP mode is the default POR mode. This command holds the MODE state machine in a reset condition. This command is available at any time, although it will not "activate" until the current I2C or SPI transaction has returned to idle.
STANDBY	STANDBY is a low power mode. AVDD and DVDD are enabled, and internal main and heartbeat clocks are enabled. The default STANDBY frequency for the heartbeat clock is ~500 Hz. TRIG mode operation must be executed from this mode. **Software must change the mode to STANDBY in register 0x10 before writing to any other register.**
SNIFF	SNIFF is a lower power, limited activity detection mode; Sniff circuitry is enabled, there is no sampling, no FIFO operations, and hardware will automatically transition to CWAKE mode upon activity detection.
CWAKE	CWAKE or continuous wake uses a slower clock speed and the entire sampling period to run the SDM/ADC. Sample data is written to the output registers or the FIFO when enabled.
TRIG	Processes a fixed number of samples, between 1 and 255. This mode ignores the setting in the ODR, but uses the STB_RATE[2:0] clock setting as the sampling rate.

Table 9. Operational Modes

5.6 Mode State Machine Flow

Figure 11. Mode Operational Flow shows the operational mode flow for the device. The device defaults to SLEEP mode following power-on. Mode transitions occur at an approximate rate of ~500Hz. Depending on the operation, the MODE State Machine may trigger events that auto-clear or set the MCTRL[2:0] bits in register 0x10 after a particular command is chosen.

For details on the Sniff Setup Steps, refer to the ENTER SNIFF API in the Programming Guide.

For details on the Sniff Cleanup Steps, refer to the Interrupt Handler in the Programming Guide.

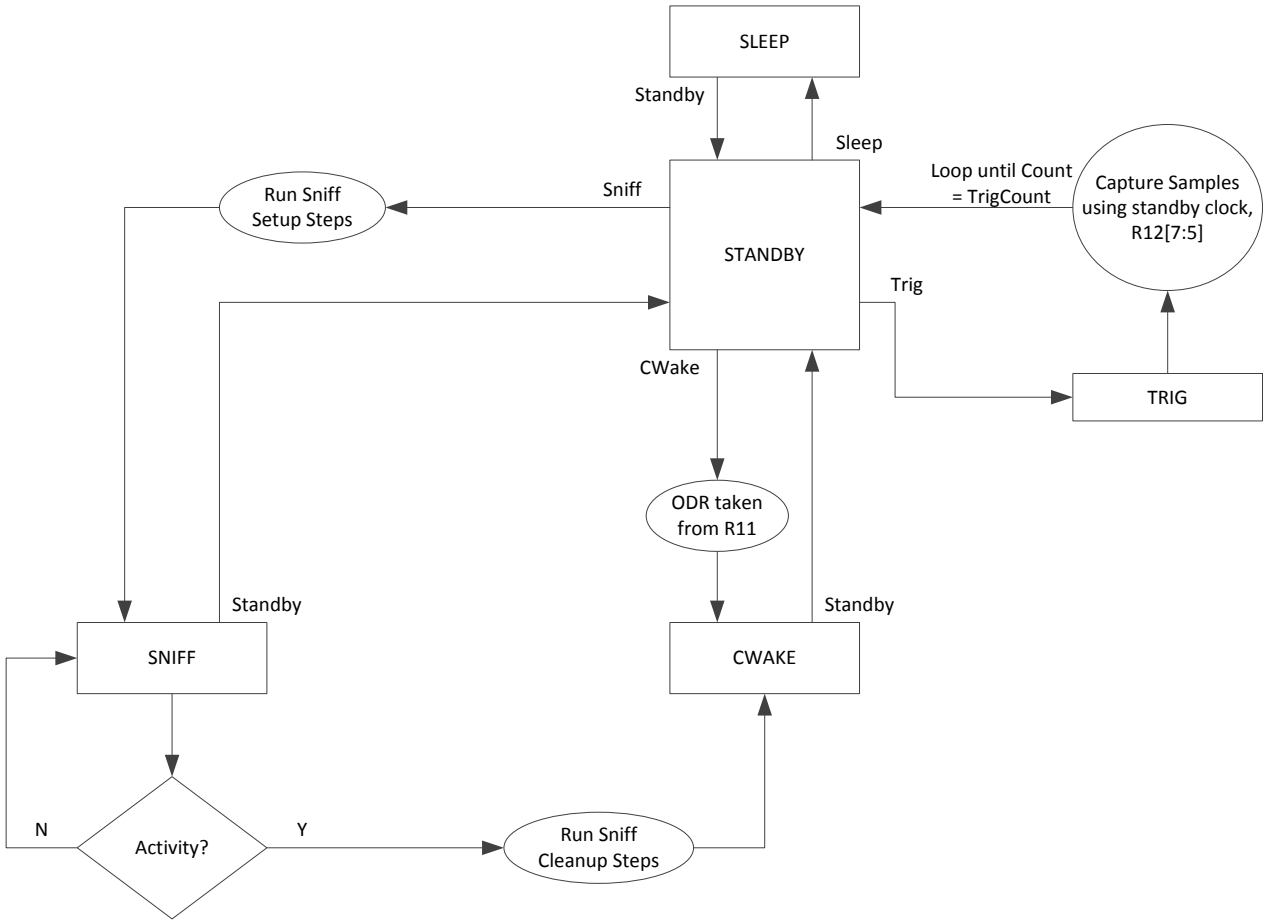


Figure 11. Mode Operational Flow

6 INTERRUPTS

6.1 INTERRUPT BLOCK

The interrupt block contains the logic for the sample acquisition, FIFO, WAKE and SNIFF interrupts. Optionally, an interrupt can trigger an external signal. When Status Register 2 is read, the interrupt flag register, all pending interrupts will be cleared.

6.2 FLAG BITS AND ENABLES

Interrupts are enabled and disabled using Register 0x17. Interrupt status is read from Register 0x08 and Register 0x09. The INT_PEND (interrupt pending) flag in Register 0x08 is set by the device if any of the interrupt bits are set in register 0x09. All flags and enable bits are active high.

6.3 INTERRUPT ON WAKE (INT_WAKE)

Interrupt on WAKE is the primary interrupt used to signal that activity has been detected during SNIFF, and that a transition to CWAKE is in process. Servicing the INT_WAKE interrupt is not required, and will not prevent the device from automatically moving to CWAKE mode, acquiring sample data, and writing it to the FIFO (if enabled). Reading register 0x09 will clear this interrupt. Register 0x17 bit 3 must be ‘1’ for this interrupt to be enabled.

6.4 INTERRUPT ON SAMPLE (INT_ACQ)

The NEW_DATA flag bit in Register 0x08 bit 3 is always enabled; there is no way to disable it. The bit is cleared each time register 0x08 is read. This flag generates an interrupt only if the INT_ACQ bit in Register 0x09 bit 3 is ‘1’. Each new sample generates a new interrupt only if register 0x09 is read to clear the flag and rearm the interrupt. This interrupt is only active in CWAKE and TRIG modes. Register 0x17 bit 3 must be ‘1’ for this interrupt to be enabled.

6.5 INTERRUPT ON FIFO EMPTY (INT_FIFO_EMPTY)

The FIFO is always empty following a POR, reset, or FIFO reset condition. After the device initialized the FIFO_EMPTY flag in register 0x08 bit 4 will be ‘1’. Reading register 0x08 has no effect on this flag. The INT_FIFO_EMPTY interrupt flag in register 0x09 bit 4 will transition high each time a new empty condition is detected. For example, if the FIFO is empty and INT_FIFO_EMPTY at register 0x09 bit 4 is ‘1’, the FIFO empty condition must be negated (e.g. the FIFO must become ‘not’ empty), and then empty again for the INT_FIFO_EMPTY flag to retrigger. Internally the FIFO compares the write and read pointers; if they are at the same address, then the empty condition exists. Register 0x17 bit 4 must be ‘1’ for this interrupt to be enabled.

6.6 INTERRUPT ON FIFO FULL (INT_FIFO_FULL)

The FIFO_FULL flag at register 0x08 bit 5 is set to ‘1’ when the FIFO contains the maximum of 32 samples. The INT_FIFO_FULL interrupt flag in register 0x09 bit 5 will transition high each

time a new full condition is detected. Register 0x17 bit 5 must be ‘1’ for this interrupt to be enabled.

6.7 INTERRUPT ON FIFO THRESHOLD (INT_FIFO_THRESH)

The FIFO_THRESH flag at register 0x08 bit 6 is set to ‘1’ when the number of samples in the FIFO is the same or greater than the threshold level specified in the FIFO Control Register 0x16 bits [4:0]. This condition will generate an interrupt when register 0x09 bit 6 is set to ‘1’. Register 0x17 bit 6 must be ‘1’ for this interrupt to be enabled.

6.8 SERVICING

Register 0x17 (Interrupt Control Register) determines which events generate interrupts. When an event is detected, it is masked with the appropriate interrupt enable bit in register 0x17. The corresponding status bit then is set in register 0x09. Multiple interrupt events may be reported at the same time in the STATUS_2 register, so software must interpret and prioritize the results. If register 0x09 is not read frequently enough, multiple flags and interrupt events will accumulate in the register.

7 INTERFACES

7.1 SPI VS I2C OPERATION MODES

The device contains both I2C and SPI slave interfaces which share common pins. However, only one interface can be active for correct device operation. Once the device completes POR or a hard reset, both interfaces are active.

After power-up and any reset of the device, the first transaction to the device must be writing to the selected enable bit, either "I2C_MODE_EN" at register 0x13 bit 7, or "SPI_MODE_EN" at register 0x14 bit 7. The situation where bits are set at the same time must be avoided or unstable device operation could occur.

To keep the "disabled" interface from interfering in future transactions, the corresponding "enable" bit must be set in the register set. For example, if the SPI interface is to be active, writing to register 0x14 bit 7, the "SPI_MODE_EN" bit is required.

7.2 I2C PHYSICAL INTERFACE

The I2C slave interface operates at a maximum speed of 400 kHz. The SDA (data) is an open-drain, bi-directional pin and the SCL (clock) is an input pin.

The device always operates as an I2C slave.

An I2C master initiates all communication and data transfers and generates the SCK_SCL clock that synchronizes the data transfer. The I2C device address depends upon the state of pin DOUT_A1 during power-up as shown in the table below.

7-bit Device ID	8-bit Address – Write	8-bit Address – Read	DOUT_A1 level upon power-up
0x4C (0b1001100)	0x98	0x99	GND
0x6C (0b1101100)	0xD8	0xD9	VDD

Table 10. I2C Address Selection

The I2C interface remains active as long as power is applied to the VDDIO pin. In STANDBY mode the device responds to I2C read and write cycles, but interrupts cannot be serviced or cleared. All registers can be written in the STANDBY mode, but in CWAKE only the (0x10) Mode Control Register can be modified.

Internally, the registers which are used to store samples are clocked by the sample clock gated by I2C activity. Therefore, in order to allow the device to collect and present samples in the sample registers at least one I2C STOP condition must be present between samples.

Refer to the I2C specification for a detailed discussion of the protocol. Per I2C requirements, when the I2C interface is enabled, DIN_SDA is an open drain, bi-directional pin. Pins SCK_SCL and DIN_SDA each require an external pull-up resistor, typically 4.7kΩ.

7.3 I2C Timing

See Section 4.3.3 I2C Timing Characteristics for I2C timing requirements.

7.4 I2C MESSAGE FORMAT

Note that at least one I2C STOP condition must be present between samples in order for the device to update the sample data registers.

The device uses the following general format for writing to the internal registers. The I2C master generates a START condition, and then supplies the 7-bit device ID. The 8th bit is the R/W# flag (write cycle = 0). The device pulls DIN_SDA low during the 9th clock cycle indicating a positive ACK.

The second byte is the 8-bit register address of the device to access, and the last byte is the data to write.

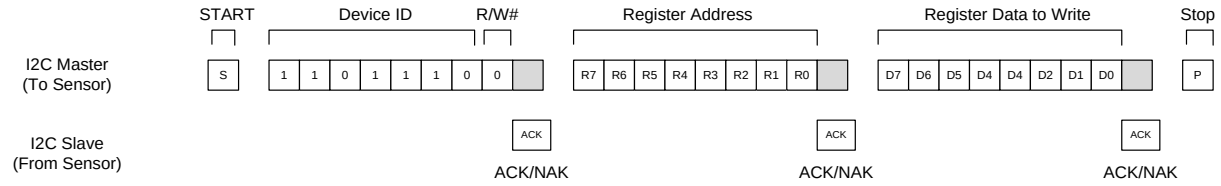


Figure 12. I2C Message Format, Write Cycle, Single Register Write

In a read cycle, the I2C master writes the device ID (R/W#=0) and register address to be read. The master issues a RESTART condition and then writes the device ID with the R/W# flag set to '1'. The device shifts out the contents of the register address.

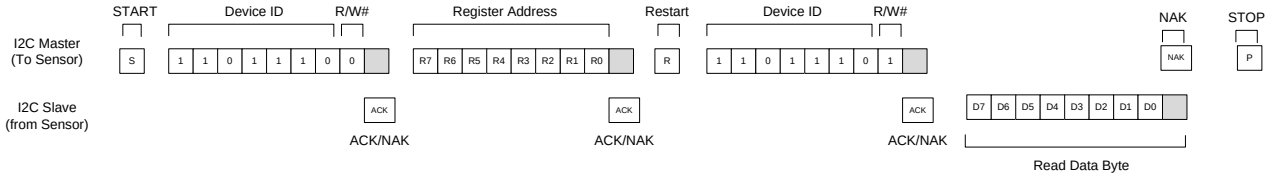


Figure 13. I2C Message Format, Read Cycle, Single Register Read

The I2C master may write or read consecutive register addresses by writing or reading additional bytes after the first access. The device will internally increment the register address.

If an I2C burst read operation reads past register address 0x0F the internal address pointer "wraps" to address 0x02.

7.5 SPI PHYSICAL INTERFACE

The SPI slave interface operates at a speed of up to 2 MHz.

The device always operates as an SPI slave. An SPI master must initiate all communication and data transfers and generate the clock that synchronizes the data transfer. The SPI interface operates in four-wire mode.

Pin	Function	Direction	Default Level	Comments
SCK_SCL	SPI clock pin	Input Only	Logic ‘1’ (Idle)	2 MHz max speed
DIN_SDA	SPI serial data in	Input Only	X (Don’t care)	
CSN	SPI chip select	Input Only	Logic ‘1’ (Idle)	Active low during SPI bus activity
DOUT_A1	SPI serial data out	Output Only	X (Don’t care)	

Table 11. SPI Physical Interface

7.6 SPI PROTOCOL

The general protocol for the SPI interface is shown in the figure below. Each read or write transaction always requires a minimum of 24 cycles of the SCK_SCL. The falling edge of CSN initiates the start of the SPI bus cycle. When the SPI master is writing data via the DIN_SDA pin, data may change when the SCK_SCL is low, and must be stable on the rising edge. Similarly, output data written to the SPI master is shifted out on the DOUT_A1 pin on the falling edge of SCK_SCL and can be latched by the master on the rising edge of SCK_SCL. Serial data in or out of the device is always MSB first.

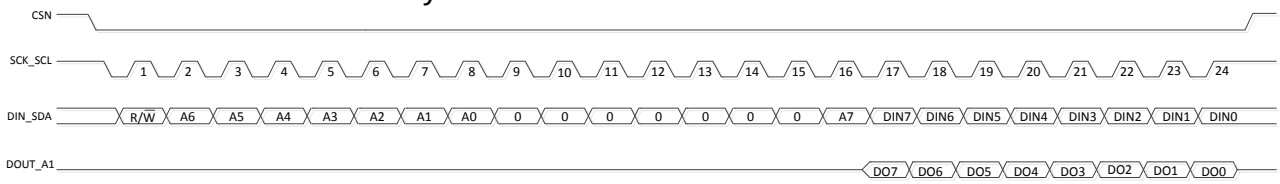


Figure 14. General SPI Protocol

7.7 SPI REGISTER ADDRESSING

The total available register address space is 128 locations, so a total of 7-address bits are required for each SPI bus cycle. The first byte of the transaction is the command/address byte. During clock ‘1’, the R/W# bit is set to ‘0’ for a write cycle or ‘1’ for a read cycle. Clocks 2 to 8 specify the address to be written to or read from. Note that during clocks 2 and 3, and 9-16, these bits must be driven to ‘0’ for the address to be correctly decoded.

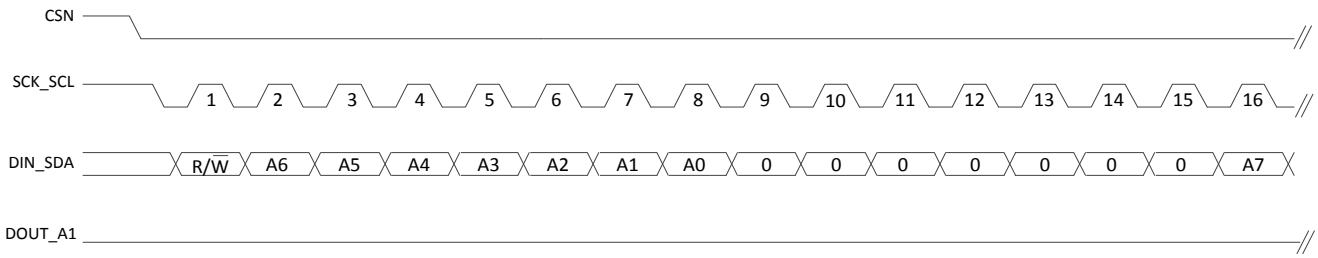


Figure 15. SPI Registers Addressing

7.8 SPI SINGLE REGISTER WRITE CYCLE

A single register write consists of a 24 clock transaction. As described above, the first bit is set to ‘0’ indicating a register write followed by the register address.

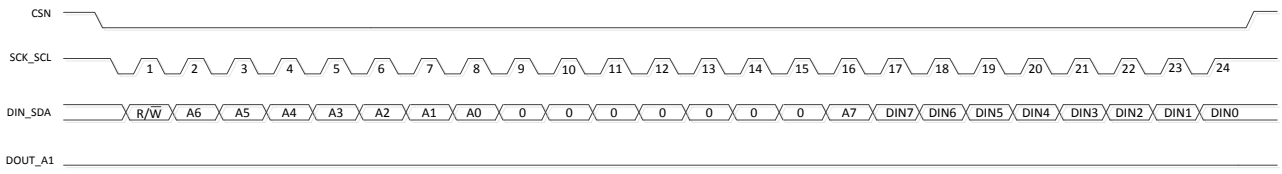


Figure 16. SPI Single Register Write Cycle

7.9 SPI SINGLE REGISTER READ CYCLE

A single register write consists of a 24 clock transaction. As described above, the first bit is set to ‘1’ indicating a register write followed by the register address.

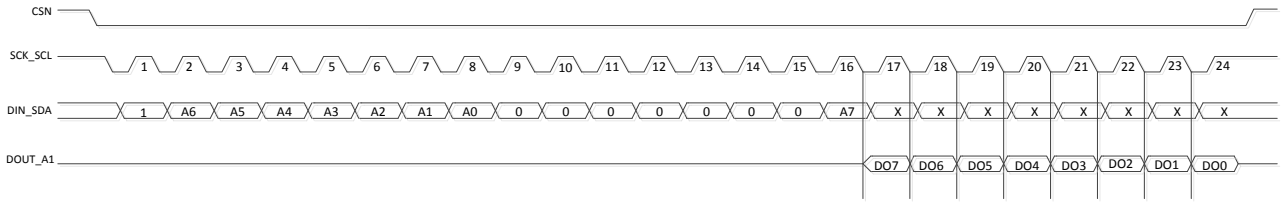


Figure 17. SPI Single Register Read Cycle

7.10 SPI BURST REGISTER READ CYCLE FROM ADDRESS 0X02

Note: Burst reads on the SPI interface must start at register address 0x02 for the internal address pointer to correctly increment. Burst reads starting from other

addresses will result in the same address being read (i.e. the internal address pointer will not increment).

If an SPI burst read operation reads past register address 0x0F the internal address pointer "wraps" to address 0x02.

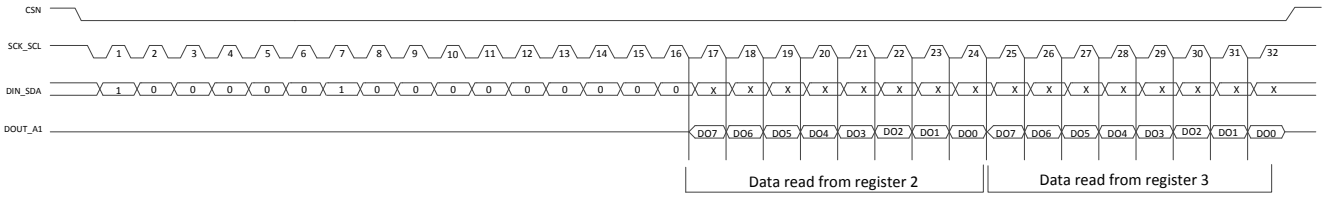


Figure 18. SPI Burst Register Read Cycle (2 Registers from address 0x02)

8 REGISTER INTERFACE

The device has a simple register interface which allows an SPI or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, bit 0 is the least significant bit (LSB) of a byte register.

8.1 Register Summary

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W[5]
0x00	EXT_STAT_1	Extended Status Register 1	RESV	RESV	RESV	RESV	I2C_AD0	RESV	RESV	RESV	0x00	R
0x01	EXT_STAT_2	Extended Status Register 2	SNIFF_ DETECT	SNIFF_EN	OTP_EN	RESV	RESV	1	PD_CLK_ STAT	OVR_ DATA	0x04	R
0x02	XOUT_LSB	XOUT_LSB	XOUT[7]	XOUT[6]	XOUT[5]	XOUT[4]	XOUT[3]	XOUT[2]	XOUT[1]	XOUT[0]	0x00	R
0x03	XOUT_MSB	XOUT_MSB	XOUT[15]	XOUT[14]	XOUT[13]	XOUT[12]	XOUT[11]	XOUT[10]	XOUT[9]	XOUT[8]	0x00	R
0x04	YOUT_LSB	YOUT_LSB	YOUT[7]	YOUT[6]	YOUT[5]	YOUT[4]	YOUT[3]	YOUT[2]	YOUT[1]	YOUT[0]	0x00	R
0x05	YOUT_MSB	YOUT_MSB	YOUT[15]	YOUT[14]	YOUT[13]	YOUT[12]	YOUT[11]	YOUT[10]	YOUT[9]	YOUT[8]	0x00	R
0x06	ZOUT_LSB	ZOUT_LSB	ZOUT[7]	ZOUT[6]	ZOUT[5]	ZOUT[4]	ZOUT[3]	ZOUT[2]	ZOUT[1]	ZOUT[0]	0x00	R
0x07	ZOUT_MSB	ZOUT_MSB	ZOUT[15]	ZOUT[14]	ZOUT[13]	ZOUT[12]	ZOUT[11]	ZOUT[10]	ZOUT[9]	ZOUT[8]	0x00	R
0x08	STATUS_1	Status Register 1	INT_PEND	FIFO_ THRESH	FIFO_FULL	FIFO_ EMPTY	NEW_ DATA	MODE[2]	MODE[1]	MODE[0]	0x00	R
0x09	STATUS_2	Status Register 2	RESV	INT_FIFO_ THRESH	INT_FIFO_ FULL	INT_FIFO_ EMPTY	INT_ACQ	INT_WAKE	RESV	RESV	0x00	R
0x0A – 0x0F		RESERVED										
0x10	MODE_C	Mode Control	TRIG	Z_AXIS_PD	Y_AXIS_PD	X_AXIS_PD	RESV	MCTRL[2]	MCTRL[1]	MCTRL[0]	0x00	W
0x11	Rate Register 1	Rate Control 1	RR[7]	RR[6]	RR[5]	RR[4]	RR[3]	RR[2]	RR[1]	RR[0]	0x00	W
0x12	SNIFF_C	Sniff Control	STB_RATE [2]	STB_RATE [1]	STB_RATE [0]	0[6]	SNIFF_SR [3]	SNIFF_SR [2]	SNIFF_SR [1]	SNIFF_SR [0]	0x00	W
0x13	SNIFFTH_C	Sniff Threshold Control	I2C_ MODE_EN	RESV	RESV	SNIFF_TH_ P[4]	SNIFF_TH_ P[3]	SNIFF_TH_ P[2]	SNIFF_TH_ P[1]	SNIFF_TH_ P[0]	0x00	W
0x14	IO_C	IO Control	SPI_ MODE_EN	RESV	RESV	RESV	RESV	RESV	RESV	RESV	0x00	W
0x15	RANGE_C	Range Resolution Control	RESV	RANGE [2]	RANGE [1]	RANGE [0]	RESV	RES[2]	RES[1]	RES[0]	0x00	W
0x16	FIFO_C	FIFO Control	FIFO_ RESET	FIFO_EN	FIFO_ MODE	FIFO_TH[4]	FIFO_TH[3]	FIFO_TH[2]	FIFO_TH[1]	FIFO_TH[0]	0x00	W
0x17	INTR_C	Interrupt Control	RESV	INT_FIFO_ THRESH	INT_FIFO_ FULL	INT_FIFO_ EMPTY	INT_ACQ	INT_ WAKE	IAH	IPP	0x00	R
0x18-0x1F		RESERVED										
0x20	DMX	Drive Motion X	RESV	RESV	RESV	RESV	DNX	DPX	RESV	RESV	0x00	W

[5] 'R' registers are read-only, via external I2C or SPI access. 'W' registers are read-write, via external I2C or SPI access.
[6] Software must always write a '0' to this bit.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W[5]
0x21	DMY	Drive Motion Y	RESV	RESV	RESV	RESV	DNY	DPY	RESV	RESV	0x00	W
0x22	DMZ	Drive Motion Z	RESV	RESV	RESV	RESV	DNZ	DPZ	RESV	RESV	0x00	W
0x23-0x24		RESERVED										
0x25	PMC	Precision Mode Control	RESV	RESV	RESV	RESV	RESV	RESV	RESV	RESV	0x00	W
0x26-0x29		RESERVED										
0x2A	XOFFL	X-Offset LSB Register	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]	Per chip	W
0x2B	XOFFH	X-Offset MSB Register	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x2C	YOFFL	Y-Offset LSB Register	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]	Per chip	W
0x2D	YOFFH	Y-Offset MSB Register	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x2E	ZOFFL	Z-Offset LSB Register	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Per chip	W
0x2F	ZOFFH	Z-Offset MSB Register	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x30	XGAIN	X Gain Register	XGAIN[7]	XGAIN[6]	XGAIN[5]	XGAIN[4]	XGAIN[3]	XGAIN[2]	XGAIN[1]	XGAIN[0]	Per chip	W
0x31	YGAIN	Y Gain Register	YGAIN[7]	YGAIN[6]	YGAIN[5]	YGAIN[4]	YGAIN[3]	YGAIN[2]	YGAIN[1]	YGAIN[0]	Per chip	W
0x32	ZGAIN	Z Gain Register	ZGAIN[7]	ZGAIN[6]	ZGAIN[5]	ZGAIN[4]	ZGAIN[3]	ZGAIN[2]	ZGAIN[1]	ZGAIN[0]	Per chip	W
0x33 to 0x34		RESERVED										
0x35	FEPX	X-Front End LSB Register	FEPX[7]	FEPX[6]	FEPX[5]	FEPX[4]	FEPX[3]	FEPX[2]	FEPX[1]	FEPX[0]	Per chip	R
0x36	FENX	X- Front End MSB Register	FENX[7]	FENX[6]	FENX[5]	FENX[4]	FENX[3]	FENX[2]	FENX[1]	FENX[0]	Per chip	R
0x37	FEPY	Y- Front End LSB Register	FEPY[7]	FEPY[6]	FEPY[5]	FEPY[4]	FEPY[3]	FEPY[2]	FEPY[1]	FEPY[0]	Per chip	R
0x38	FENY	Y- Front End MSB Register	FENY[7]	FENY[6]	FENY[5]	FENY[4]	FENY[3]	FENY[2]	FENY[1]	FENY[0]	Per chip	R
0x39	FEPZ	Z- Front End LSB Register	FEPZ[7]	FEPZ[6]	FEPZ[5]	FEPZ[4]	FEPZ[3]	FEPZ[2]	FEPZ[1]	FEPZ[0]	Per chip	R
0x3A	FENZ	Z- Front End MSB Register	FENZ[7]	FENZ[6]	FENZ[5]	FENZ[4]	FENZ[3]	FENZ[2]	FENZ[1]	FENZ[0]	Per chip	R
0x3B	MS	Mode Setting Register	MS[7]	MS[6]	MS[5]	MS[4]	MS[3]	MS[2]	MS[1]	MS[0]	Per chip	R
0x3C to 0x7F		RESERVED										

Table 12. Register Summary[7]

[7] No registers are updated with new event status or samples while a SPI cycle (pin CSN low) or I2C cycle is in process.

8.2 (0x00) Extended Status Register 1

This register contains status for the I2C address of the device.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x00	EXT_STAT_1	RESV	RESV	RESV	RESV	I2C_AD0	RESV	RESV	RESV	00000000	R

Bit	Name	Description
2:0	RESV	Reserved
3	I2C_AD0_BIT	Value of I2C slave address obtained from reading the DOUT_A1 pin at POR. If this bit is '1', the 7-bit base address of the I2C slave changes from 0x4C to 0x6C.
7:4	RESV	Reserved

Table 13. Extended Status Register 1

8.3 (0x01) Extended Status Register 2

The device status register reports various conditions of the device data, clock and sniff circuitry.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x01	EXT_STAT_2	SNIFF_ DETECT	SNIFF_EN	OTP_EN	RESV	RESV	1	PD_CLK_ STAT	OVR_ DATA	00000100	RO

Bit	Name	Description
0	OVR_DATA	0: Previous acceleration sample has not been overwritten before read by host 1: Previous acceleration sample was not read by host and has been overwritten.
1	PD_CLK_STAT	Returns the power-down status of the clocks. 0: Clocks are enabled. 1: Clocks are disabled.
2	RESV	Always returns 1.
4:3	RESV	Reserved
5	OTP_EN	OTP VDD status bit: 0: OTP_VDD supply is not enabled, OTP is powered down. 1: OTP_VDD supply is enabled, OTP is powered.
6	SNIFF_EN	SNIFF mode enable flag: 0: SNIFF mode is not active. 1: SNIFF mode is active.
7	SNIFF_DETECT	SNIFF wakeup or detect flag: 0: No sniff event detected. 1: Sniff event detected, move to CWAKE mode.

Table 14. Extended Status Register 2

8.4 (0x02 – 0x07) XOUT, YOUT & ZOUT Data Output Registers

The measurements from sensors for the 3-axes are available in these 3 registers. The most-significant bit of the value is the sign bit, and is sign extended to the higher bits.

Software must set only one of these two bits to '1', depending upon if the I2C or SPI interface will be used for external communications. No data will appear in XOUT, YOUT and ZOUT registers if both the I2C_MODE_EN bit and SPI_MODE_EN bit are set to 0 (default).

When the FIFO is enabled, the output of the FIFO is mapped to registers 0x02 to 0x07, and the data has a maximum resolution of 12-bits.

During FIFO reads, software must start a read at address 0x02 and complete a read to address 0x07 for the FIFO pointers to increment correctly.

Once an I2C start bit has been recognized by the device, registers will not be updated until an I2C stop bit has occurred. Therefore, if software desires to read the low and high byte registers 'atomically', knowing that the values have not been changed, it should do so by issuing a start bit, reading one register, then reading the other register then issuing a stop bit. Note that all 6 registers may be read in one burst with the same effect.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x02	XOUT_LSB	XOUT LSB Register	XOUT [7]	XOUT [6]	XOUT [5]	XOUT [4]	XOUT [3]	XOUT [2]	XOUT [1]	XOUT [0]	0x00	R
0x03	XOUT_MSB	XOUT MSB Register	XOUT [15]	XOUT [14]	XOUT [13]	XOUT [12]	XOUT [11]	XOUT [10]	XOUT [9]	XOUT [8]	0x00	R
0x04	YOUT_LSB	YOUT LSB Register	YOUT [7]	YOUT [6]	YOUT [5]	YOUT [4]	YOUT [3]	YOUT [2]	YOUT [1]	YOUT [0]	0x00	R
0x05	YOUT_MSB	YOUT MSB Register	YOUT [15]	YOUT [14]	YOUT [13]	YOUT [12]	YOUT [11]	YOUT [10]	YOUT [9]	YOUT [8]	0x00	R
0x06	ZOUT_LSB	ZOUT LSB Register	ZOUT [7]	ZOUT [6]	ZOUT [5]	ZOUT [4]	ZOUT [3]	ZOUT [2]	ZOUT [1]	ZOUT [0]	0x00	R
0x07	ZOUT_MSB	ZOUT MSB Register	ZOUT [15]	ZOUT [14]	ZOUT [13]	ZOUT [12]	ZOUT [11]	ZOUT [10]	ZOUT [9]	ZOUT [8]	0x00	R

Table 15. XOUT, YOUT, ZOUT Data Output Registers

8.5 (0x08) Status Register 1

This register reports the operational mode of the device. Note that the lower 3-bits, the MODE[2:0] field, do not immediately change once a command is written to the MODE register, but may take up to 3 transitions of the heartbeat clock.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x08	STATUS_1	INT_PEND	FIFO_ THRESH	FIFO_FULL	FIFO_ EMPTY	NEW_ DATA	MODE[2]	MODE[1]	MODE[0]	00000000	RO

Bit	Name	Description		
2:0	MODE[2:0]	**Decode**	**Mode**	**Comments**
		000	SLEEP	Lowest power mode, regulators on, no clock activity, partial chip power-down.
		001	STANDBY (SLEEP)	Low power mode, no sampling, clocks active. (Device may show STANDBY mode as it transitions from STANDBY to SLEEP).
		010	SNIFF	Sniff activity detection mode, sniff enabled, no sampling, no FIFO operations, automatically transition to CWAKE mode upon activity detection.
		011	RESV	Reserved
		100	RESV	Reserved
		101	CWAKE	Continuous wake, use entire sampling period to run ADC.
		110	Reserved	Reserved

		111	TRIG	Trigger mode, 1 to 255 samples, return to SLEEP or STANDBY upon completion.
3	NEW_DATA	0: No new sample data has arrived since last read. 1: New sample data has arrived and has been written to FIFO/registers.		
4	FIFO_EMPTY	0: FIFO has one or more samples in storage (level) 1: FIFO is empty (level)		
5	FIFO_FULL	0: FIFO has space or 1 or more samples (up to 32) (level). 1: FIFO is full, all 32 samples are used (level).		
6	FIFO_THRESH	0: Amount of data in FIFO is less than the threshold (level) 1: Amount of data in FIFO is equal to or greater than the threshold (level)		
7	INT_PEND	0: No interrupt flags pending in register 0x09 (level) 1: One or more interrupt flags pending in register 0x09 (logical OR) (level).		

Table 16. Status Register 1

8.6 (0x09) Status Register 2

This register reports the state of the interrupts. A interrupt flag bit in this register will only transition if the corresponding interrupt enable is set to '1' in the Interrupt Control Register. Reading this register will clear any pending interrupts that are waiting for servicing.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x09	STATUS_2	RESV	INT_FIFO_THRESH	INT_FIFO_FULL	INT_FIFO_EMPTY	INT_ACQ	INT_WAKE	RESV	RESV	00000000	RO

Bit	Name	Description
1:0	Reserved	Reserved.
2	INT_WAKE	This interrupt will transition when the accelerometer automatically moves from SNIFF to CWAKE. Once cleared, another SNIFF to CWAKE event must take place to retrigger it.
3	INT_ACQ	This interrupt will transition when a new sample is acquired. This flag stays high upon the first sample acquired and will not rearm unless serviced.
4	INT_FIFO_EMPTY	This interrupt will transition when the FIFO is empty. This flag stays high upon the first empty condition and will not rearm unless serviced.
5	INT_FIFO_FULL	This interrupt will transition when the FIFO is full. This flag stays high upon the first empty condition and will not rearm unless serviced.
6	INT_FIFO_THRESHOLD	This interrupt will transition when the FIFO sample count is equal to or greater than the threshold count. This flag stays high upon the first threshold condition and will not rearm unless serviced.
7	RESV	Reserved

Table 17. Status Register 2

8.7 (0x10) Mode Control Register

This register is the primary control register for the accelerometer. The operational mode of the device, X/Y/Z axis enables, and the TRIG one shot mode can be written through this register. Most of the mode transitions controlled by this register may take up to 3 transitions of the heartbeat clock. Depending on the operation, the lower 3-bits (MCTRL[2:0]) may be automatically set or cleared by hardware if auto-triggered events are executed.

In general, when software sets an operational mode using the MCTRL [2:0] bits, there might be a delay time of 2 to 10 mSec before the operational mode is reflected by the MODE[2:0] bits in Status Register 1, address 0x08.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x10	MODE_C	Mode Control	TRIG	Z_AXIS_PD	Y_AXIS_PD	X_AXIS_PD	RESV	MCTRL[2]	MCTRL[1]	MCTRL[0]	0x00	W

Bit	Name	Description		
2:0	MCTRL[2:0]	**Decode**	**Mode**	**Comments**
		000	SLEEP	Lowest power mode, regulators on, no clock activity, partial chip power-down.
		001	STANDBY	Low power mode, no sampling, clocks active.
		010	SNIFF	Sniff activity detection mode, sniff enabled, no sampling, no FIFO operations, automatically transition to CWAKE mode upon activity detection.
		011	Reserved	Reserved
		100	Reserved	Reserved
		101	CWAKE	Continuous wake.
		110	Reserved	Reserved
		111	TRIG	Trigger mode, 1 to 255 samples, return to SLEEP upon completion.

3	RESV	Reserved
4	X_AXIS_PD	0: X-axis is enabled. 1: X-axis is disabled.
5	Y_AXIS_PD	0: Y-axis is enabled. 1: Y-axis is disabled.
6	Z_AXIS_PD	0: Z-axis is enabled. 1: Z-axis is disabled.
7	TRIG	Setting this bit will execute the trigger mode where 1 to 255 samples are acquired. The number of samples is specified by the TRIG_COUNT in register 0x29. The starting mode for TRIG mode must be STANDBY. Once the number of samples is complete, the device will return to STANDBY mode.

Table 18. Mode Control Register Settings

8.8 (0x11) Rate Register 1

This register, along with Register 0x12, configures the sample rates for wake modes. The rates also depend upon the value in register 0x3B. The device has several power modes which can be adjusted to achieve a desired power consumption at a certain ODR. The tradeoff for lower power is either higher noise or lower ODR. See the table below.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x11	Rate Register 1	RR[7]	RR[6]	RR[5]	RR[4]	RR[3]	RR[2]	RR[1]	RR[0]	00000000	RW

Ultra-Low Power (0x3B=>0x03)			Low Power (0x3B=>0x00)			Precision (0x3B=>0x02)		
CWAKE ODR (Hz)	Registers	Current (µA) (FIFO off / on)	CWAKE ODR (Hz)	Registers	Current (µA) (FIFO off / on)	CWAKE ODR (Hz)	Registers	Current (µA) (FIFO off / on)
11	0x11=>0x05	0.7 / 0.9	13	0x11=>0x05	0.9 / 1.3	14	0x11=>0x82 0x12=>0x08	3 / 5
23	0x11=>0x06	0.9 / 1.3	25	0x11=>0x82 0x12=>0x0C	2 / 3	26	0x11=>0x06	6 / 9
46	0x11=>0x82 0x12=>0x08	2 / 4	50	0x11=>0x82 0x12=>0x08	3 / 5	53	0x11=>0x07	9 / 14
90	0x11=>0x08	3 / 6	100	0x11=>0x08	6 / 9	n/a		
190	0x11=>0x09	7 / 11	200	0x11=>0x09	9 / 14	n/a		
370	0x11=>0x0A	9 / 14	n/a			n/a		

Table 19. Rate Register 1 Settings

8.9 (0x12) Sniff Control Register

This register selects the sample rate for SNIFF mode, the clock rate for STANDBY mode, and which CWAKE mode is selected when hardware detects an event in SNIFF mode.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x12	SNIFF_C	STB_RATE[2]	STB_RATE[1]	STB_RATE[0]	0	SNIFF_SR[3]	SNIFF_SR[2]	SNIFF_SR[1]	SNIFF_SR[0]	00000000	RW

NOTE: Software must always write 0 to bit 4.

Bit	Name	Description	
3:0	SNIFF_SR[3:0]	**Sample Rate Select**	**Sample Rate**
		0100	6 Hz
		Others	Reserved
4	0	**Software must always write 0 to this bit.**	
7:5	STB_RATE[2:0]	**Rate Select**	**Clock Rate**
		000	Default, 0.4Hz
		001	1.5 Hz
		010	3 Hz
		011	6 Hz
		100	13 Hz
		101	25 Hz
		110	50 Hz
		111	100 Hz

Table 20. Sniff Control Register Settings

8.10 (0x13) Sniff Threshold Control Register

This register sets the threshold the SNIFF logic compares the combined acceleration of X, Y, and Z to for activity detection.

The mode will transition from SNIFF to CWAKE when the condition below is met, comparing one sample to the next:

$$\Delta(X + Y + Z) > \text{Selection of SNIFF\_TH\_P[4:0]}$$

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x13	SNIFFTH_C	I2C_MODE_EN	RESV	RESV	SNIFF_TH_P [4]	SNIFF_TH_P [3]	SNIFF_TH_P [2]	SNIFF_TH_P [1]	SNIFF_TH_P [0]	00000000	RW

Bit	Name	Description
4:0	SNIFF_TH_P[4:0]	[00111]: Sniff threshold of ~1g [ALL OTHER CODES]: Reserved
6:5	RESV	Reserved
7	I2C_MODE_EN	0: Device interface is still defined as it was at power-up but no data will appear in XOUT, YOUT and ZOUT registers if both this bit and SPI_MODE_EN are set to 0 (default). 1: Disables any SPI communications.

Table 21. Sniff Threshold Register Settings

8.11 (0x14) IO Control Register

Enabling the SPI_MODE_EN bit disables any possible I2C communications. For correct SPI operation, this bit must be set to '1' before any active sampling is enabled. Otherwise, sample data will not be written to the XOUT, YOUT and ZOUT output registers.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x14	IO_C	SPI_MODE_EN	RESV	RESV	RESV	RESV	RESV	RESV	RESV	00000000	RW

Bit	Name	Description
6:0	RESV	Reserved
7	SPI_MODE_EN	0: Device interface is still defined as it was at power-up but no data will appear in XOUT, YOUT and ZOUT registers if both this bit and I2C_MODE_EN are set to 0 (default). 1: Disables any I2C communications.

8.12 (0x15) Range and Resolution Control Register

The RANGE register sets the resolution and range options for the accelerometer. All numbers are sign-extended, 2's complement format. All results are reported in registers 0x02 to 0x07.

When the FIFO is enabled, only 6 to 12-bit resolutions are supported due to the 12-bit width of the FIFO.

Software must prevent the selections of binary 110 and 111 being written to the RES[2:0] bit-field.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x15	RANGE_C	RESV	RANGE[2]	RANGE[1]	RANGE[0]	RESV	RES[2]	RES[1]	RES[0]	00000000	RW

Bit	Name	Description	
2:0	RES[2:0]	**[2:0]**	**Bit Width of Accelerometer Data**
		000	6 bits
		001	7 bits
		010	8 bits
		011	10 bits
		100	12 bits
		101	14 bits (Do not select if FIFO enabled)
		110	Reserved (Do not select if FIFO enabled)
		111	Reserved (Do not select if FIFO enabled)
3	RESV	Reserved	
6:4	RANGE[2:0]	**[2:0]**	**G Range Selection**
		000	±2g
		001	±4g
		010	±8g

		011	±16g
		100	±12g
		101	Reserved
		110	Reserved
		111	Reserved
7	RESV	Reserved	

Table 22. Range and Resolution Control Register Settings

8.13 (0x16) FIFO Control Register

This register selects the FIFO threshold level, operation mode, FIFO reset and enable. With the exception of FIFO_RESET, the FIFO_EN bit must be '1' for any FIFO interrupts, thresholds, or modes to be enabled. The FIFO flags in register 0x08 will continue to report FIFO defaults even if the FIFO_EN is '0'.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x16	FIFO_C	FIFO_ RESET	FIFO_EN	FIFO_ MODE	FIFO_TH [4]	FIFO_TH [3]	FIFO_TH [2]	FIFO_TH [1]	FIFO_TH [0]	00000000	RW

Bit	Name	Description
4:0	FIFO_TH[4:0]	The FIFO threshold level selects the number of samples in the FIFO for different FIFO events. The threshold value may be 1 to 31 (00001 to 11111).
5	FIFO_MODE	0: Normal operation, the FIFO continues to accept new sample data as long as there is space remaining (default) 1: Watermark, once the amount of samples in the FIFO reaches or exceeds the threshold level, the FIFO stops accepting new sample data. Any additional sample data is "dropped".
6	FIFO_EN	FIFO enable control. All FIFO operations are gated by this bit. 0: No FIFO operation, sample data written directly to output registers. 1: FIFO enabled, all sample data written to FIFO write port if there is room. The FIFO write clock is controlled by this enable, resulting in higher dynamic power.
7	FIFO_RESET	Asynchronous FIFO reset. 0: FIFO reset is disabled, normal operation (default) 1: FIFO read and write pointers are cleared, FIFO contents returned to 0

Table 23. FIFO Control Register Settings

8.14 (0x17) Interrupt Control Register

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x17	INTR_C	RESV	INT_FIFO_ THRESH	INT_FIFO_ FULL	INT_FIFO_ EMPTY	INT_ACQ	INT_ WAKE	IAH	IPP	00000000	RW

Bit	Name	Description
0	IPP	INTN pin interrupt pin mode control. 0: INTN pin is configured for open-drain mode (external pullup to VDDIO required). 1: INTN pin is configured for active drive or “push-pull” mode. Drive level is to VDDIO.
1	IAH	Interrupt level control, sets the active drive level of the INTN pin. 0: Interrupt request is active low (default). 1: Interrupt request is active high.
2	INT_WAKE	WAKE interrupt (SNIFF to WAKE) enable 0: No interrupt is generated when SNIFF activity is detected and the device auto-transitions to CWAKE mode. 1: Generate an interrupt when activity is detected in SNIFF mode and the device auto-transitions to CWAKE mode.
3	INT_ACQ	Interrupt on sample or acquisition enable 0: No interrupt generated when new sample data is acquired. 1: Generate an interrupt when new sample data is acquired (applies to new data written to output registers or FIFO). This enable is paired with the NEW_DATA flag in register 0x08.
4	INT_FIFO_EMPTY	FIFO empty interrupt enable. 0: No interrupt is generated when the FIFO is empty or completely drained of sample data. 1: Generate an interrupt when the FIFO is empty. This interrupt is paired with the FIFO_EMPTY flag in register 0x08. Note that this interrupt is independent of the FIFO threshold level, and will only activate when the FIFO sample count has reached a value of 0.

5	INT_FIFO_FULL	FIFO full interrupt enable. 0: No interrupt is generated when the FIFO is empty or completely filled of sample data. 1: Generate an interrupt when the FIFO is full. This interrupt is paired with the FIFO_FULL flag in register 0x08. Note that this interrupt is independent of the FIFO threshold level, and will only activate when the FIFO sample count has reached a value of 32.
6	INT_FIFO_THRESH	FIFO threshold interrupt enable. 0: No interrupt is generated when the FIFO threshold level is reached. 1: Generate an interrupt when the FIFO threshold level is reached.
7	RESV	Reserved

Table 24. Interrupt Control Register Settings

8.15 (0x20) Drive Motion X Register

This register controls the test mode which moves the sensor in the X axis direction.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x20	DMX	0	0	0	0	DNX	DPX	0	0	00000000	RW

Software must always write 0 to bits [7:4] and [1:0].

Bit	Name	Description
[1:0]	RESV	**Reserved. Always write 0 to these bits.**
2	DPX	0: Disabled (default) 1: Move the sensor in X Positive direction
3	DNX	0: Disabled (default) 1: Move the sensor in X Negative direction
[7:4]	RESV	**Reserved. Always write 0 to these bits.**

Table 25. Drive Motion X Register Settings

8.16 (0x21) Drive Motion Y Register

This register controls the test mode which moves the sensor in the Y axis direction.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x21	DMY	RESV	RESV	RESV	RESV	DNY	DPY	RESV	RESV	00000000	RW

Software must always write 0 to bits [7:4] and [1:0].

Bit	Name	Description
[1:0]	RESV	**Reserved. Always write 0 to these bits.**
2	DPY	0: Disabled (default) 1: Move the sensor in Y Positive direction
3	DNY	0: Disabled (default) 1: Move the sensor in Y Negative direction
[7:4]	RESV	**Reserved. Always write 0 to these bits.**

Table 26. Drive Motion Y Register Settings

8.17 (0x22) Drive Motion Z Register

This register controls the test mode which moves the sensor in the Z axis direction.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x22	DMZ	RESV	RESV	RESV	RESV	DNZ	DPZ	RESV	RESV	00000000	RW

Software must always write 0 to bits [7:4] and [1:0].

Bit	Name	Description
[1:0]	RESV	**Reserved. Always write 0 to these bits.**
2	DPZ	0: Disabled (default) 1: Move the sensor in Z Positive direction
3	DNZ	0: Disabled (default) 1: Move the sensor in Z Negative direction
[7:4]	RESV	**Reserved. Always write 0 to these bits.**

Table 27. Drive Motion Z Register Settings

8.18 (0x25) Precision Mode Control

Writing the PM sequence to this register sets the accelerometer into precision mode.

Addr	Name	Bit								POR Value	R/W
		7	6	5	4	3	2	1	0		
0x25	PMC	RESV	RESV	RESV	RESV	RESV	RESV	RESV	RESV	00000000	W

8.19 (0x2A – 0x2B) X-Axis Offset Registers

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the acceleration values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2A	XOFFL	**XOFF[7]**	**XOFF[6]**	**XOFF[5]**	**XOFF[4]**	**XOFF[3]**	**XOFF[2]**	**XOFF[1]**	**XOFF[0]**	Per chip	W
0x2B	XOFFH	XGAIN[8]	**XOFF[14]**	**XOFF[13]**	**XOFF[12]**	**XOFF[11]**	**XOFF[10]**	**XOFF[9]**	**XOFF[8]**	Per chip	W

8.20 (0x2C – 0x2D) Y-Axis Offset Registers

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the acceleration values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2C	YOFFL	**YOFF[7]**	**YOFF[6]**	**YOFF[5]**	**YOFF[4]**	**YOFF[3]**	**YOFF[2]**	**YOFF[1]**	**YOFF[0]**	Per chip	W
0x2D	YOFFH	YGAIN[8]	**YOFF[14]**	**YOFF[13]**	**YOFF[12]**	**YOFF[11]**	**YOFF[10]**	**YOFF[9]**	**YOFF[8]**	Per chip	W

8.21 (0x2E – 0x2F) Z-Axis Offset Registers

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the acceleration values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2E	ZOFFL	**ZOFF[7]**	**ZOFF[6]**	**ZOFF[5]**	**ZOFF[4]**	**ZOFF[3]**	**ZOFF[2]**	**ZOFF[1]**	**ZOFF[0]**	Per chip	W
0x2F	ZOFFH	ZGAIN[8]	**ZOFF[14]**	**ZOFF[13]**	**ZOFF[12]**	**ZOFF[11]**	**ZOFF[10]**	**ZOFF[9]**	**ZOFF[8]**	Per chip	W

8.22 (0x2B & 0x30) X-Axis Gain Registers

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2B	XOFFH	**XGAIN[8]**	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x30	XGAIN	**XGAIN[7]**	**XGAIN[6]**	**XGAIN[5]**	**XGAIN[4]**	**XGAIN[3]**	**XGAIN[2]**	**XGAIN[1]**	**XGAIN[0]**	Per chip	W

8.23 (0x2D & 0x31) Y-Axis Gain Registers

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2D	YOFFH	**YGAIN[8]**	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x31	YGAIN	**YGAIN[7]**	**YGAIN[6]**	**YGAIN[5]**	**YGAIN[4]**	**YGAIN[3]**	**YGAIN[2]**	**YGAIN[1]**	**YGAIN[0]**	Per chip	W

8.24 (0x2F & 0x32) Z-Axis Gain Registers

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2F	ZOFFH	**ZGAIN[8]**	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x32	ZGAIN	**ZGAIN[7]**	**ZGAIN[6]**	**ZGAIN[5]**	**ZGAIN[4]**	**ZGAIN[3]**	**ZGAIN[2]**	**ZGAIN[1]**	**ZGAIN[0]**	Per chip	W

8.25 (0x35 & 0x36) X-Axis Front End Registers

These registers show the front end factory settings for the X axis.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x35	FEPX	FEPX[7]	FEPX[6]	FEPX[5]	FEPX[4]	FEPX[3]	FEPX[2]	FEPX[1]	FEPX[0]	Per chip	R
0x36	FENX	FENX[7]	FENX[6]	FENX[5]	FENX[4]	FENX[3]	FENX[2]	FENX[1]	FENX[0]	Per chip	R

8.26 (0x37 & 0x38) Y-Axis Front End Registers

These registers show the front end factory settings for the Y axis.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x37	FEPY	FEPY[7]	FEPY[6]	FEPY[5]	FEPY[4]	FEPY[3]	FEPY[2]	FEPY[1]	FEPY[0]	Per chip	R
0x38	FENY	FENY[7]	FENY[6]	FENY[5]	FENY[4]	FENY[3]	FENY[2]	FENY[1]	FENY[0]	Per chip	R

8.27 (0x39 & 0x3A) Z-Axis Front End Registers

These registers show the front end factory settings for the Z axis.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x39	FEPZ	FEPZ[7]	FEPZ[6]	FEPZ[5]	FEPZ[4]	FEPZ[3]	FEPZ[2]	FEPZ[1]	FEPZ[0]	Per chip	R
0x3A	FENZ	FENZ[7]	FENZ[6]	FENZ[5]	FENZ[4]	FENZ[3]	FENZ[2]	FENZ[1]	FENZ[0]	Per chip	R

8.28 (0x3B) Mode Setting Register

This register controls the precision mode for the device.

NOTE: When modifying this register, software must perform a read-modify-write type of access to bits [7:2] to ensure that factory settings do not get changed inadvertently.

NOTE: The PM sequence must be written to register 0x25 before this register can be changed.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x3B	MS	**MS[7]**	**MS[6]**	**MS[5]**	**MS[4]**	**MS[3]**	**MS[2]**	MS[1]	MS[0]	Per chip	R

Bit	Name	Description
[1:0]	Mode Setting	00: Low Power Mode (nominal noise levels) 01: Reserved 10: Precision Mode (lowest noise levels) 11: Ultra-Low Power Mode (highest noise levels)
[7:2]	Factor Set	**Software must read and write back the original contents**

Table 28. Mode Setting Register Settings

9 INDEX OF TABLES

10 REVISION HISTORY

Date	Revision	Description
2015-01	APS-048-0042v1.0	First release.
2015-02	APS-048-0042v1.1	Updated Typical Application Circuits. Changed VDD and VDDIO rise time condition to <40mSec. Corrected level of 0x08[4]. Updated some reference text. Added detail to the SNIFFTH_C. Updated SPI speed and pin settings and diagram. Clarified sniff condition description.
2015-06	APS-048-0042v1.2	Updated Reg 0x08 STANDBY bit. Updated sample rate, power consumption and noise mode values. Corrected Sniff mode to single setting. Updated SPI typical circuit. Added Front End and PMC registers. Corrected some typos in waveforms.
2015-07	APS-048-0042v1.3	Edited Absolute Maximum table.
2015-07	APS-048-0042v1.4	Updated rate tolerance and ODRs, power consumption numbers in WAKE. Updated flow diagram. Added Mode Setting register. Updated register 0x11 description.
2015-08	APS-048-0042v1.5	Changed package drawing text to refer to leads. Updated Ultra-Low Power values.
2015-11	APS-048-0042v1.6	Updated Sensor Characteristic specs (noise, offset, current). Updated minimum ODR throughout.

11 LEGAL

1. M-CUBE reserves the right to make corrections, modifications, enhancements, improvements and other changes to its products and to this document at any time and discontinue any product without notice. The information contained in this document has been carefully checked and is believed to be accurate. However, M-CUBE shall assume no responsibilities for inaccuracies and make no commitment to update or to keep current the information contained in this document.

2. M-CUBE products are designed only for commercial and normal industrial applications and are not suitable for other purposes, such as: medical life support equipment; nuclear facilities; critical care equipment; military / aerospace; automotive; security or any other applications, the failure of which could lead to death, personal injury or environmental or property damage. Use of the products in unsuitable applications are at the customer's own risk and expense.

3. M-CUBE shall assume no liability for incidental, consequential or special damages or injury that may result from misapplication or improper use of operation of the product.

4. No license, express or implied, by estoppel or otherwise, to any intellectual property rights of M-CUBE or any third party is granted under this document.

5. M-CUBE makes no warranty or representation of non-infringement of intellectual property rights of any third party with respect to the products. M-CUBE specifically excludes any liability to the customers or any third party regarding infringement of any intellectual property rights, including the patent, copyright, trademark or trade secret rights of any third party, relating to any combination, machine, or process in which the M-CUBE products are used.

6. Examples of use described herein are provided solely to guide use of M-CUBE products and merely indicate targeted characteristics, performance and applications of products. M-CUBE shall assume no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein

7. Information described in this document including parameters, application circuits and its constants and calculation formulas, programs and control procedures are provided for the purpose of explaining typical operation and usage. "Typical" parameters that may be provided in M-CUBE data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including "Typicals," must be validated for each customer application by customer's technical experts. In no event shall the information described be regarded as a guarantee of conditions or characteristics of the products. Therefore, the customer should evaluate the design sufficiently as whole system under the consideration of various external or environmental conditions and determine their application at the customer's own risk. M-CUBE shall assume no responsibility or liability for claims, damages, costs and expenses caused by the customer or any third party, owing to the use of the above information.