To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

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MOS FIELD EFFECT TRANSISTOR
NP110N055PUG

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The NP110N055PUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

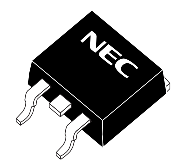
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP110N055PUG	TO-263 (MP-25ZP)

FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance
  $R_{DS(on)}$ = 2.4 mΩ MAX. (V_{GS} = 10 V, I_D = 55 A)
- Low C_{iss}: C_{iss} = 17100 pF TYP.

(TO-263)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	55	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±110	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±440	A
Total Power Dissipation (T_A = 25°C)	P_{T1}	1.8	W
Total Power Dissipation (T_C = 25°C)	P_{T2}	288	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current Note2	I_{AR}	66	A
Repetitive Avalanche Energy Note2	E_{AR}	435	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. T_{ch} ≤ 150°C, V_{DD} = 28 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.52	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

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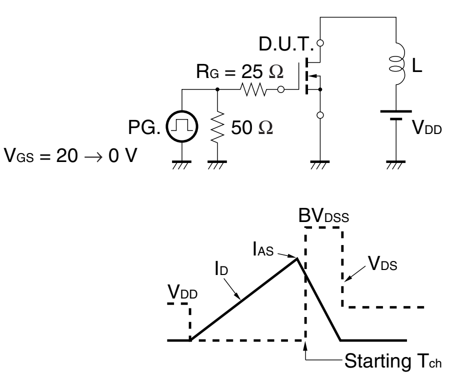
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

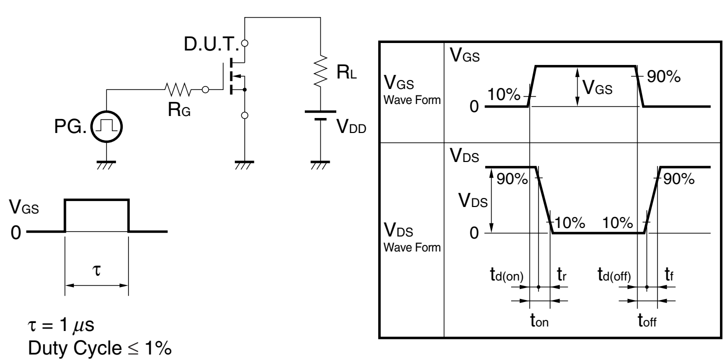
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55 V, V_{GS} = 0 V			1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage Note	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = 10 V, I_D = 55 A	42	83		S
Drain to Source On-state Resistance Note	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 55 A		1.9	2.4	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V		17100	25700	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		1120	1680	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		725	1310	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 28 V, I_D = 55 A		63	140	ns
Rise Time	t_r	V_{GS} = 10 V		201	510	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		131	270	ns
Fall Time	t_f			19	50	ns
Total Gate Charge	Q_G	V_{DD} = 44 V		251	380	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		63		nC
Gate to Drain Charge	Q_{GD}	I_D = 110 A		81		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 110 A, V_{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 110 A, V_{GS} = 0 V		58		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		87		nC

Note Pulsed

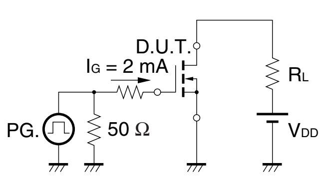
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

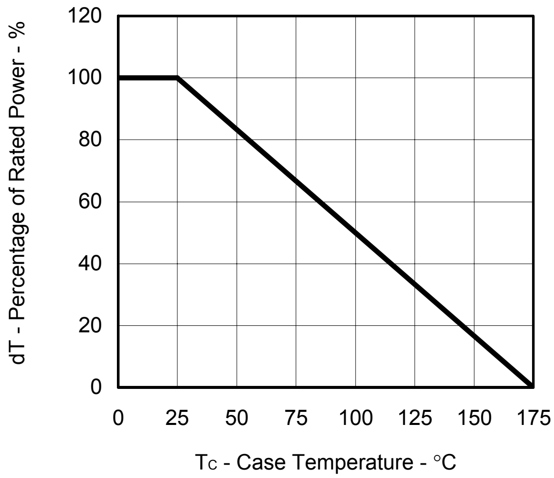


TEST CIRCUIT 3 GATE CHARGE

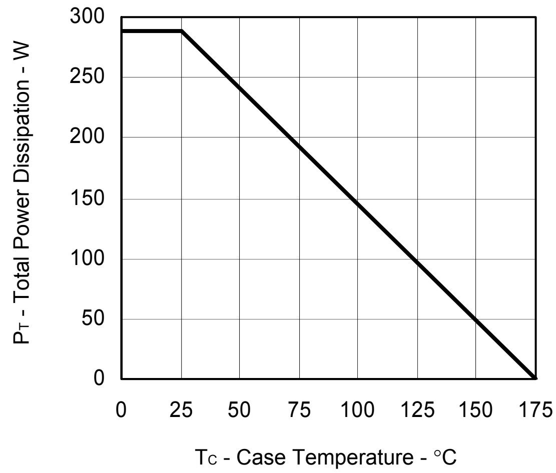


TYPICAL CHARACTERISTICS (T_A = 25°C)

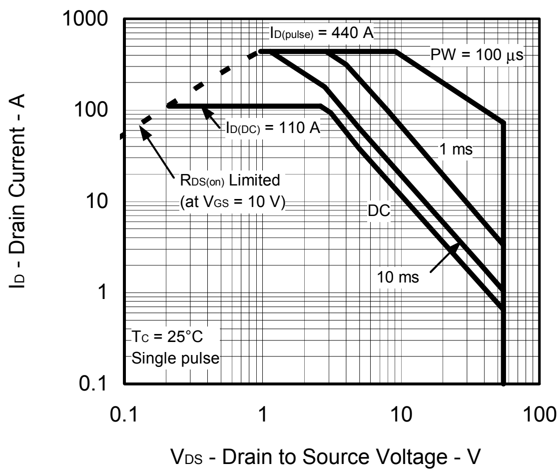
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



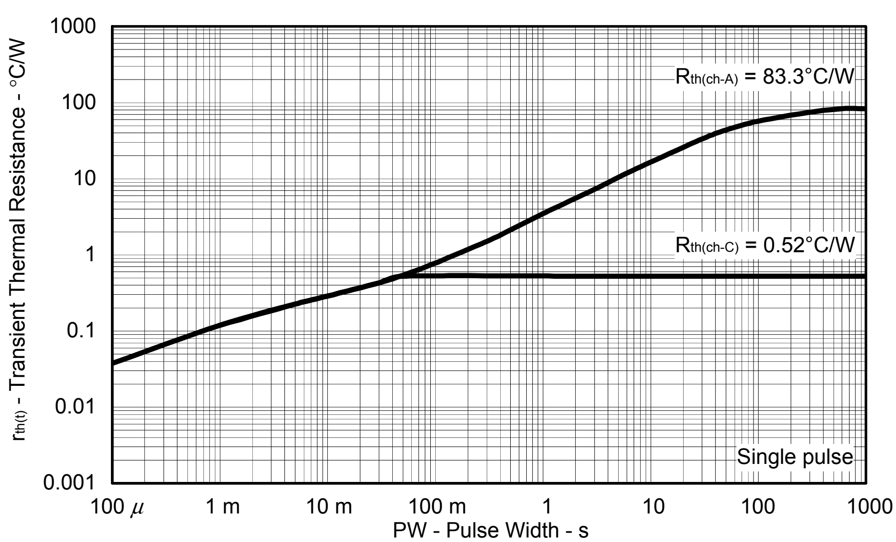
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



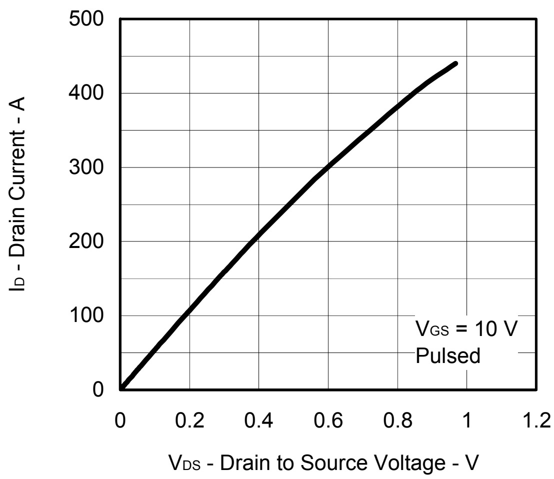
FORWARD BIAS SAFE OPERATING AREA



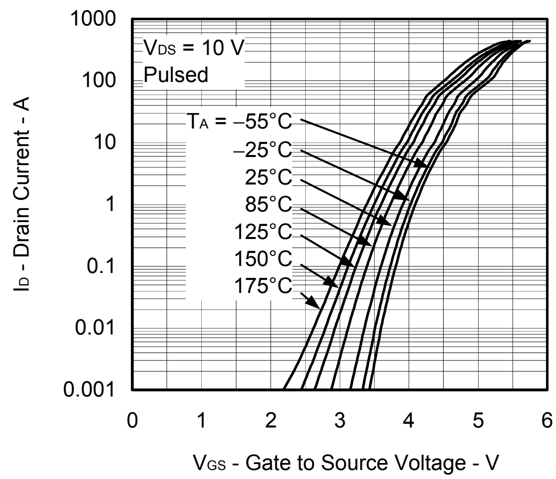
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



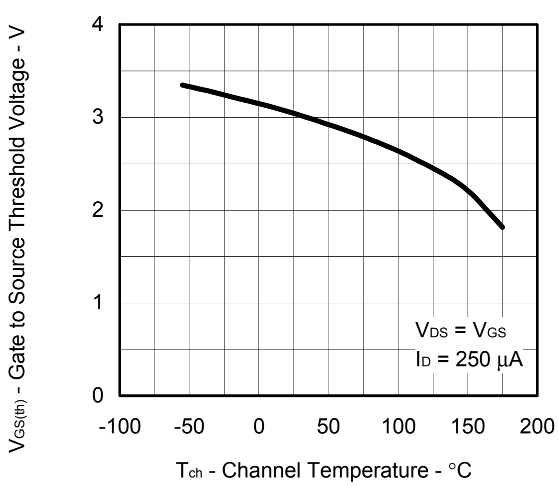
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



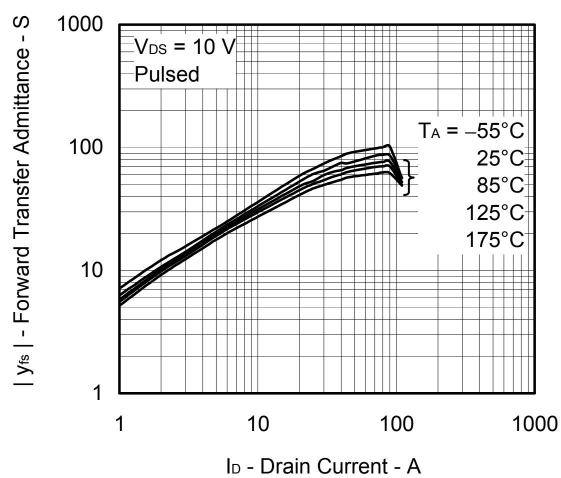
FORWARD TRANSFER CHARACTERISTICS



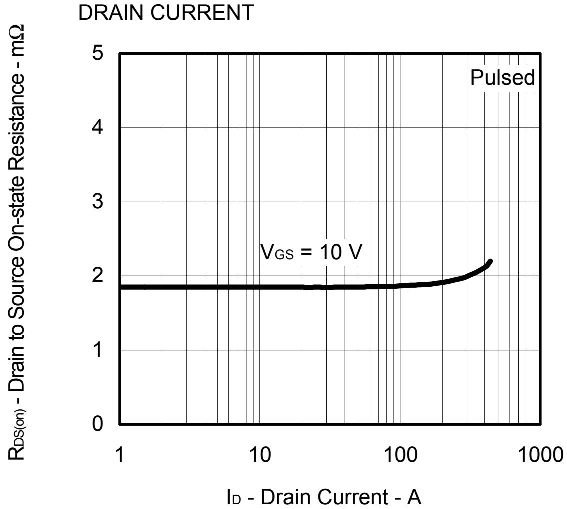
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



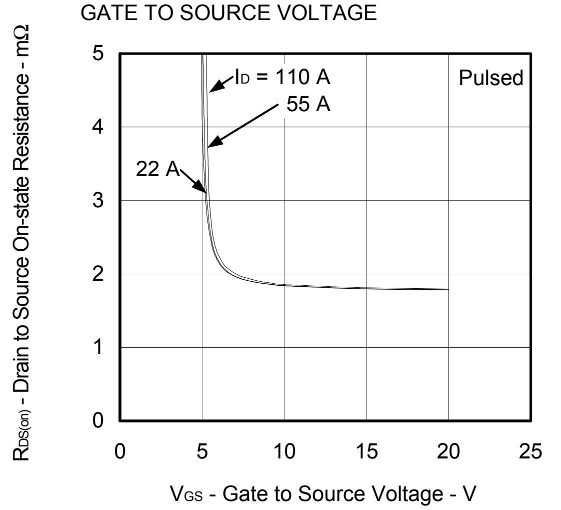
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



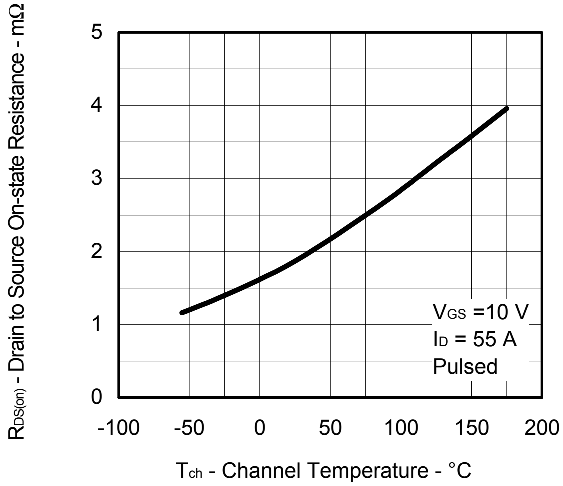
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



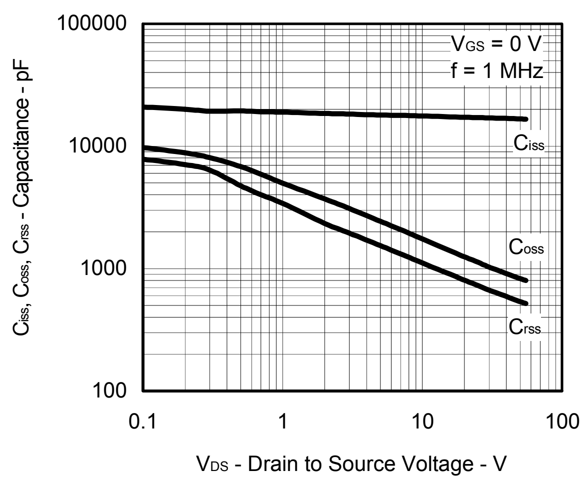
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



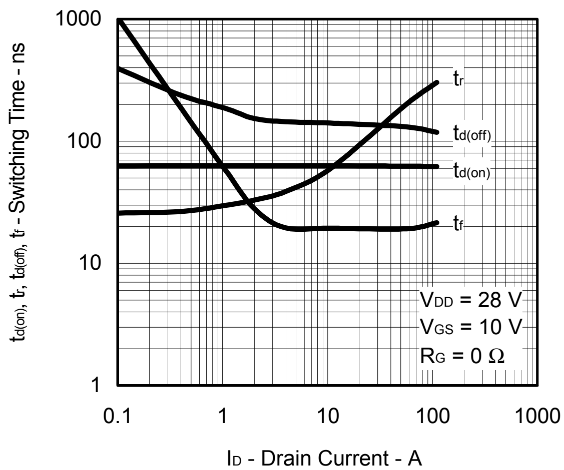
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



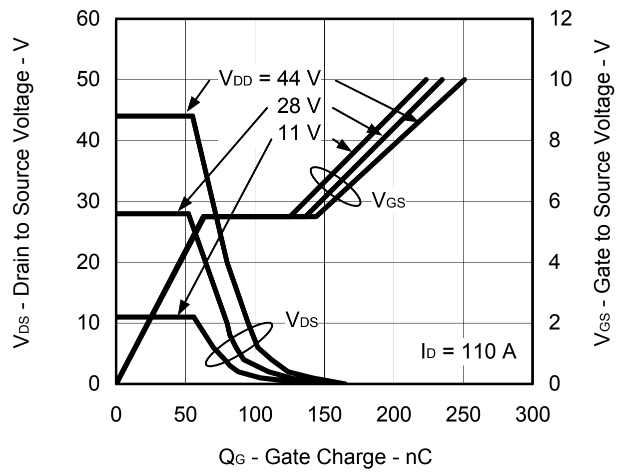
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



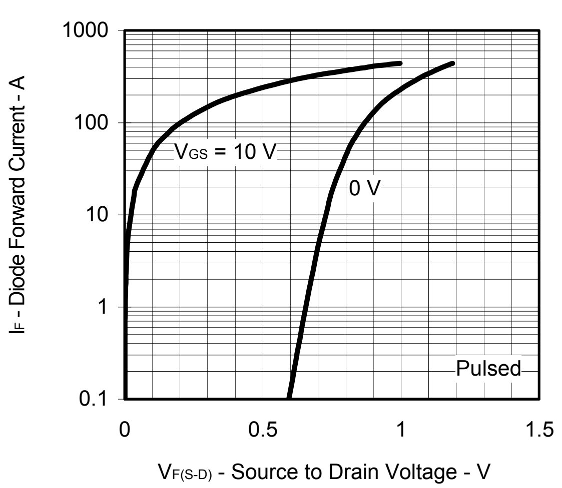
SWITCHING CHARACTERISTICS



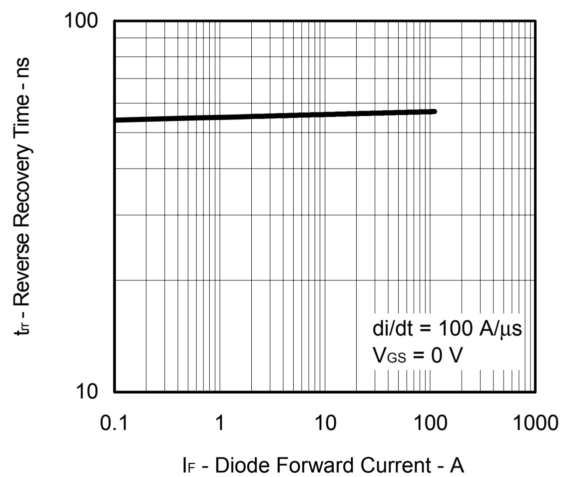
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

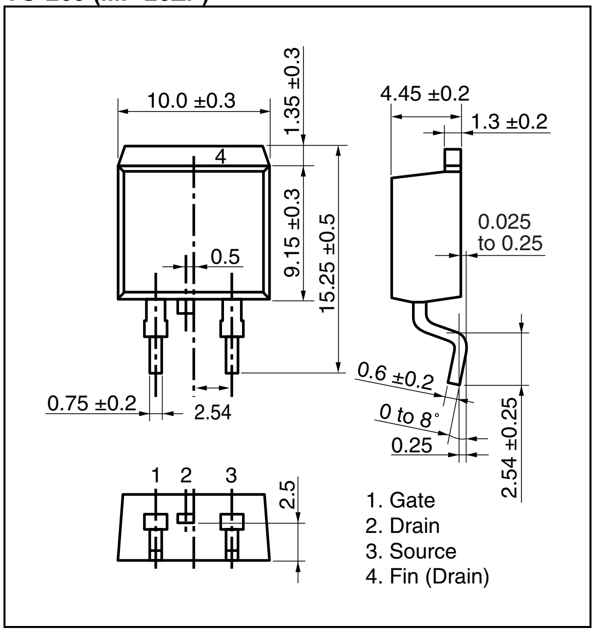


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

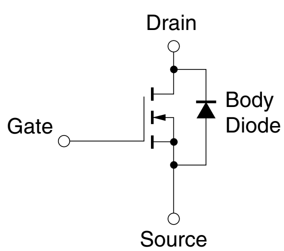


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZP)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.