Keysight U4164A
Logic Analyzer Module
with Options up to 4 Gb/s State Mode and 10 GHz Timing Mode

Data Sheet

KEYSIGHT TECHNOLOGIES

Unlocking Measurement Insights

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Product Description

The Keysight Technologies, Inc. U4164A logic analyzer system combines reliable data capture with powerful analysis and validation tools to enable you to quickly and confidently validate and debug high-speed digital designs operating at speeds up to 4 Gb/s. The U4164A logic analyzer module delivers the following unique capabilities that enable you to make measurements and achieve levels of insight unavailable with other logic analyzers:

- Quad sample state mode provides four samples with two different threshold settings from a single-touch connection to high-speed data signals under test [1]
- Dual sample, dual threshold state mode
- Clock hysteresis allows the user to define a hysteresis range about the clock threshold
- 10 GHz ¼ channel conventional and transitional timing mode [2]
- Software tool for timing de-skew
- 400 Mb (sample) memory depth option
- Four speed options corresponding to the state clock rate, data rate, and timing mode sample rates

Applications

- Functional validation of memory systems and other high-speed digital systems operating up to 4 Gb/s
- Debug of hardware and software in high-speed digital systems operating up to 4 Gb/s
- Qualitative bus level signal integrity insight using eye scan or DDR eye scan

Features

- State capture up to 4 Gb/s on 68 channels, 2.5 Gb/s on 136 channels per module
- Reliable data capture on eye openings as small as 100 ps by 100 mV
- 12.5 GHz timing zoom with 256 K sample memory
- Memory depth up to 400 M samples
- Wide variety of probing solutions including BGA, interposer, mid-bus, and flying leads
- Up to 10,880 channels in a system using Multiframe

User values

- Confidence in state measurements with signal eye openings as small as 100 ps by 100 mV
- Rapidly view signal integrity information in a matter of minutes on all the buses in your design under a wide variety of operating conditions
- Quickly and easily set up complex DDR and LPDDR measurements
- 350 MHz, 700 MHz, 1.4 GHz, and 2.5 GHz state speed options: Purchase the level of state speed capture capability you need now and upgrade as your state speed needs increase. The U4164A with the 2.5 GHz state speed option allows you to capture the highest speeds (up to 4 Gb/s) for DDR/LPDDR memory systems
- Dual-sample state mode: set separate sample positions and thresholds for DDR/LPDDR read/write captures for data rates less than 2500 Mb/s from one probe point
- Quad-sample state mode: set separate sample positions and thresholds for DDR/LPDDR read/write and rising/falling edge captures for data rates greater than 2500 Mb/s from one probe point
- Clock hysteresis: avoid false sampling on noisy clock inputs when differential clocks turn off
- 10 GHz quarter channel conventional and transitional timing mode: Identify timing problems in deep traces with high sample resolution
- 400 Mb (sample) memory depth option: Capture more system activity so you can debug complex problems when the symptom and root cause are widely separated in time

1. Available in Option -02G
2. Available in Options -01G and -02G

Product Description (Continued)

Beyond being a powerful general purpose logic analysis system, the U4164A system includes specific tools and features to enable powerful debug, validation and analysis of DDR and LPDDR memory systems.

Figure 1A shows the Read DQ and DQS eyes associated with byte lane 0 on a DDR4 system operating at 3300 Mb/s data rate. This screen shot is captured in signal trace mode with no back-to-back bursts so that the eyes for the entire burst of eight are displayed. The trace was captured using the FS2510AB DDR4 DIMM interposer providing double probe points of each DDR4 DQ with the logic analyzer module in dual-sample state mode. The U4164A logic analyzer uses its unique eye scan capability to automatically place the sampling point in both time and voltage within the eye on each individual channel for optimal sampling reliability.

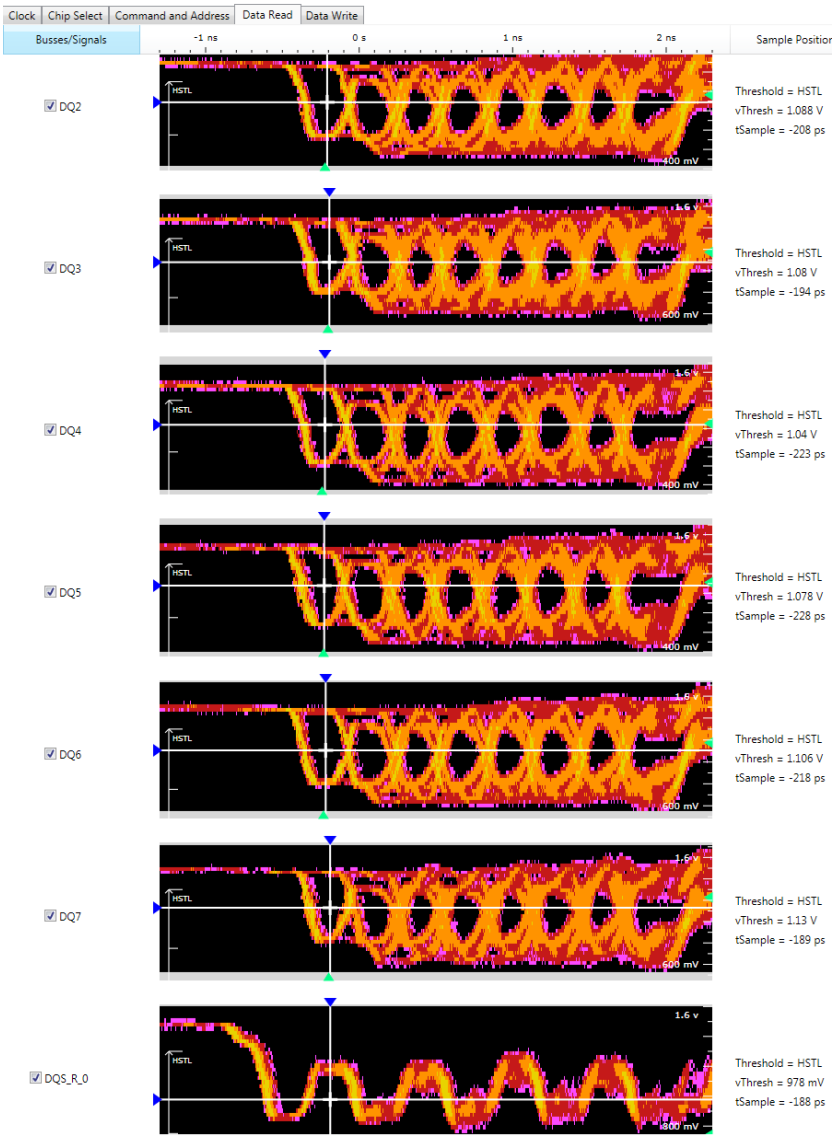


Figure 1A. DDR4 3300 Mb/s read DQ bursts for bits D2 – D7 and DQS0.

Product Description (Continued)

Figure 1B shows the trigger setup to capture a burst of eight DDR4 writes using the unique Keysight burst trigger that captures precise sequences of two to eight patterns per burst recognizer. (The U4164A has up to eight burst detectors.) The trigger sequencer operates up to 2.5 GHz, enabling accurate and precise triggering on DDR4 read or write bursts of DQ up to 4 Gb/s with each DQ sampled simultaneously for both a rising edge and falling edge sample. Notice that the exact write DQ burst in the trigger is at the trigger point in both the waveform and listing displays. The trigger marker is red and is found at the last sample in the DDR4 write burst. The green marker is for the start of the write burst and the yellow marker in the listing is at the write command where the B4661A DDR4 decoder has assembled the DQ with the write command and associated row and column addresses.

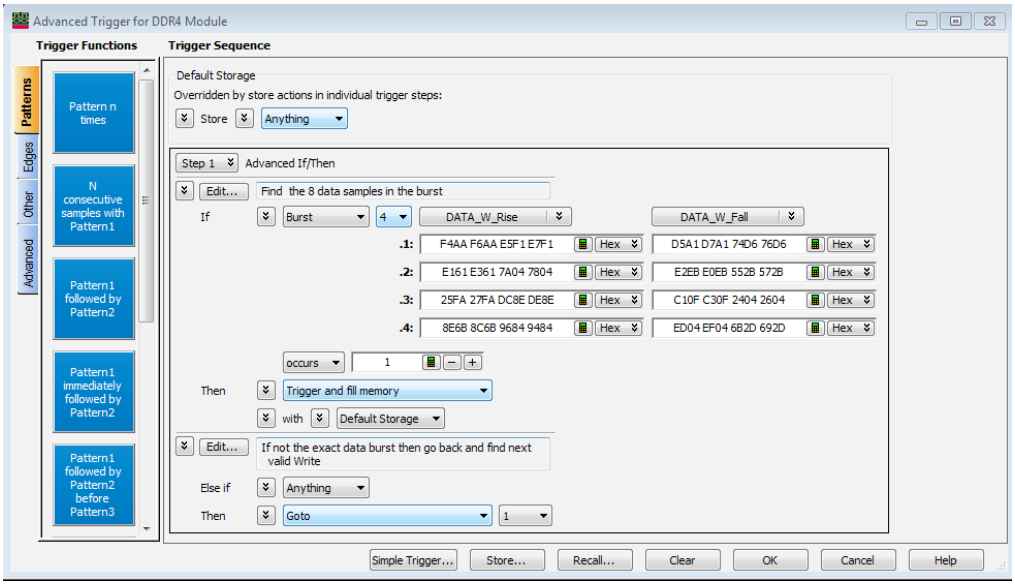


Figure 1B. DDR4 3300 Mb/s burst trigger for specific write DQ burst.

Figure 1C shows the state listing and Figure 1D shows the waveform for this capture using the B4661A DDR decoder. Figure 1E shows the transaction decode option and traffic overview of the DDR4 3300 Mb/s trace using the B4661A performance analysis software.

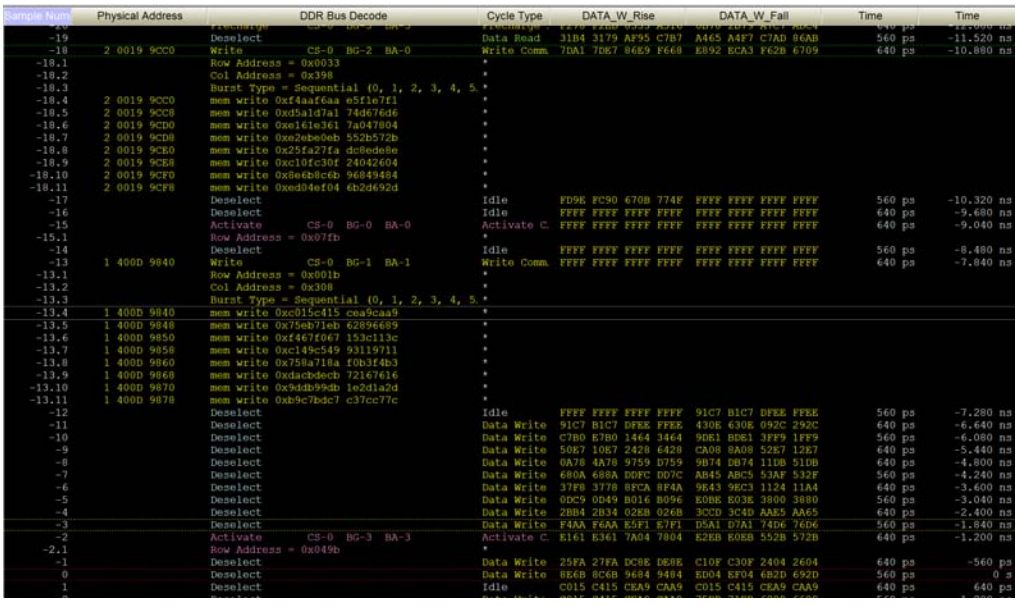


Figure 1C. DDR4 3300 Mb/s listing.

Product Description (Continued)

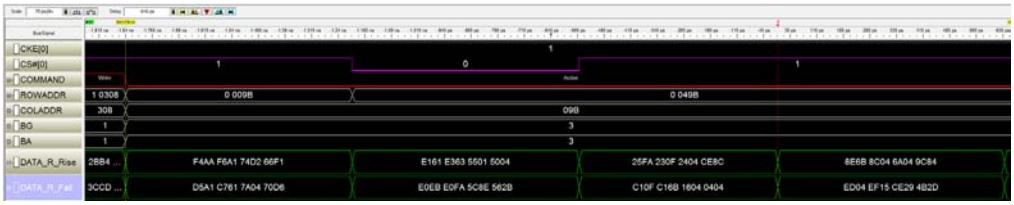


Figure 1D. DDR4 3300 Mb/s state waveform.

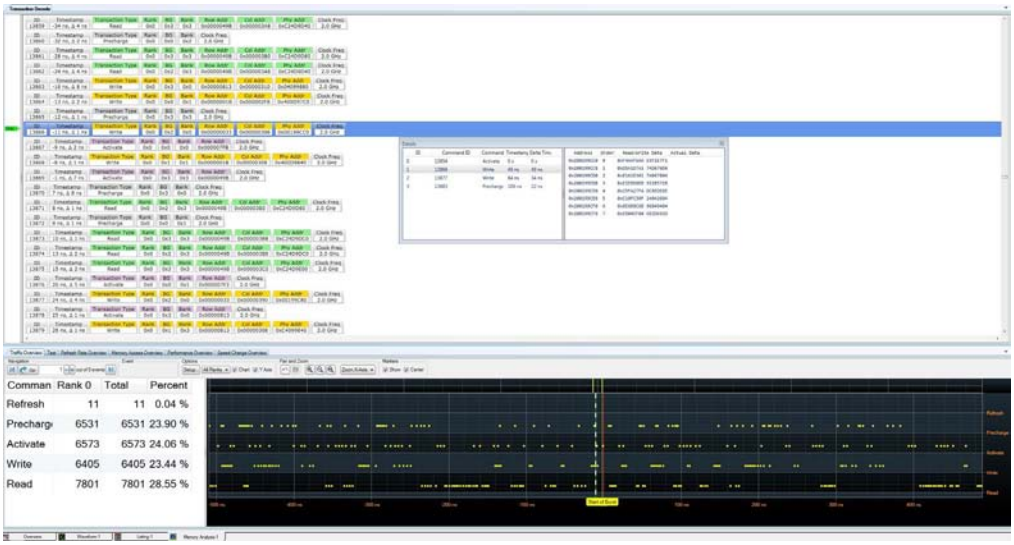


Figure 1E. DDR4 3300 Mb/s state waveform.

There are two methods to capture DDR or LPDDR memory DQ (data) transactions over 2500 Mb/s using the U4164A logic analyzer system:

1. Using quad-sample state mode, the U4164A is sampled on one clock edge, a single probe load is placed on each DQ, and quad-sample mode is used to provide separate read rising, read falling, write rising, and write falling edge captures with sample positions set independently. Read and write thresholds can be set independently. Read rising, read falling, write rising, and write falling edge captures are given different labels in the configuration so that the sample positions can be set independently.

2. Using dual-sample state mode, the U4164A is sampled on one clock edge, double probing of each DQ must be performed and provide separate read DQ and write DQ samples, and dual-sample mode is used to provide a rising and falling edge sample for each DQ, resulting in four samples taken for each DQ signal from two probe loads. Read rising, read falling, write rising, and write falling edge captures are given different labels so the sample positions can be set independently.

Dual-Sample State Mode

Dual-sample mode has multiple benefits:

1. For non-DDR or LPDDR memory trace capture, dual-sample state mode allows acquisition of state (synchronous) data at rates up to 4 Gb/s depending on the speed state option purchased. When used in this mode, the data will appear in two labels. One label for rising edge and another for falling edge captures. The logic analyzer will be clocked with one edge of the system clock. Labels can be merged using the Keysight B4602A signal extractor tool. When operated in dual-sample state mode on all pods, the channel count is 68 channels for one U4164A 136 channels for two U4164As, or 204 channels for three U4164A modules combined. Dual-sample state mode can be selected on a per-pod-pair basis, so if you have only a subset of signals that require dual-sample mode, the channel count can be higher.

2. For DDR/LPDDR memory signals up to 2.5 Gb/s, dual-sample state mode allows separation of read data samples from write data samples. The B4661A DDR2/3/4 decoder or the B4661A LPDDR/2/3/4 decoder reassembles the data to align with the associated commands. (There's no need for the B4602A tool for DDR and LPDDR solutions.)

3. For DDR4 and LPDDR4 memory solutions over 2.5 Gb/s using dual-sample state mode, double probing is required to capture read and write DQ signals and dual-sample state mode is used to capture rising and falling edge DQ samples. Using this technique, a maximum of 34 DDR4 or LPDDR4 DQ signals operating over 2.5 Gb/s can be captured per U4164A module. Address, command, and control signals for DDR or LPDDR memory do not require double probing above or below 2.5 Gb/s data rates, so modules with a mixture of address, command and DQ signals may have higher signal count depending on how the signals are routed into the U4164A.

Quad-Sample State Mode

Quad-sample state mode enables four samples with two different threshold settings from a single-touch connection to high-speed data signals under test. This results in four unique sample positions at two unique thresholds. Single-touch connection preserves probe routing space and minimized probe load on high-speed digital systems. DDR4 and LPDDR4 probing for data rates over 2.5 Gb/s are examples of where single-touch probing enables high-speed trace capture using quad-sample mode to capture read and write DQ (data) at different thresholds with rising and falling edge samples for both read and write data to sample, trigger, and display DDR4 and LPDDR4 at data rates up to 4 Gb/s.

When operated in quad-sample state mode on all pods, the channel count is 34 channels for one U4164A, 68 channels for two U4164As, or 102 channels for three U4164A modules combined. Quad-sample state mode is only available with U4164A Option -02G. Quad-sample state mode can be selected on a per-pod-pair basis, so if you have only a subset of signals that require quad-sample mode, the channel count can be higher.

State Mode Clock Inputs and Clock Qualifiers

State mode support for bursty clock inputs allows you to take measurements that include periods of in activity on the clock, such as power management transitions when the clock is inactive. In state mode, the U4164A allows one clock input into pod 1 of the clocking module.

- Double module set - bottom module of set is clocking module
- Three card set - middle module is clocking module

There are five clock qualifiers available on the clocking module. The clock inputs to pods 2, 3, 4, and 5 can be used as “AND” or “OR” clock qualifiers. The “RESET” clock qualifier input on pod 7 is available as an “AND” input only when the other clock qualifiers are setup as “OR” inputs. The most common use mode for this clock qualifier is to capture “RESET” when the other clock qualifiers are looking for clock enable (CKE) signals on DDR and LPDDR buses.

Clock hysteresis

The U4164A module has a unique clock hysteresis feature that allows the user to define a range about the clock threshold. Using clock hysteresis enables the U4164A clock input in state mode to avoid false sampling on noisy clock inputs that may float to zero volts at the differential clock input to the U4164A when the clock is turned off. Clock hysteresis improves state mode captures from systems where a differential clock input turns off and floats to zero volts.

Clock hysteresis control is inside the threshold dialog for the clock. The “hysteresis on” check box [x] is an on/off control. There is also an input for the amount of hysteresis setting in millivolts around threshold between 0 and 1 volts.

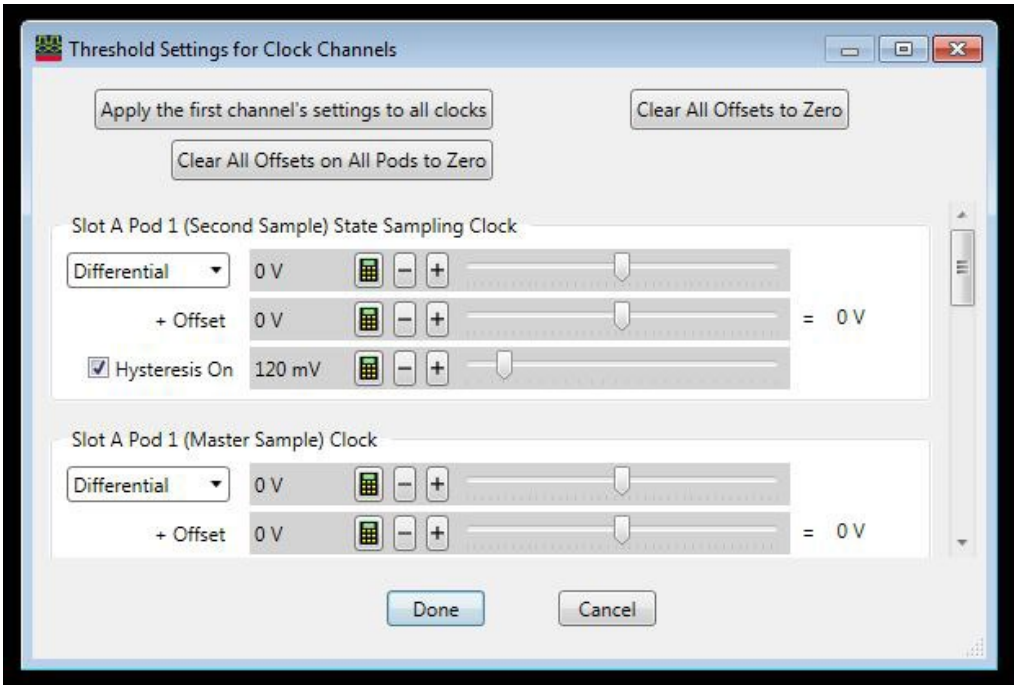


Figure 2. Clock hysteresis selection and setting in clock thresholds window. The settings shown were used to capture an LPDDR4 system initializing without the use of any clock qualifiers.

Timing Zoom

The 12.5 GHz timing zoom with 256 K sample memory gives you simultaneous state and high-resolution timing measurements covering a time span of 20 us, which corresponds to 43680 clock cycles at a 2133 MHz clock rate. Timing zoom also provides simultaneous high-resolution timing measurements with conventional and transitional timing modes of operation.

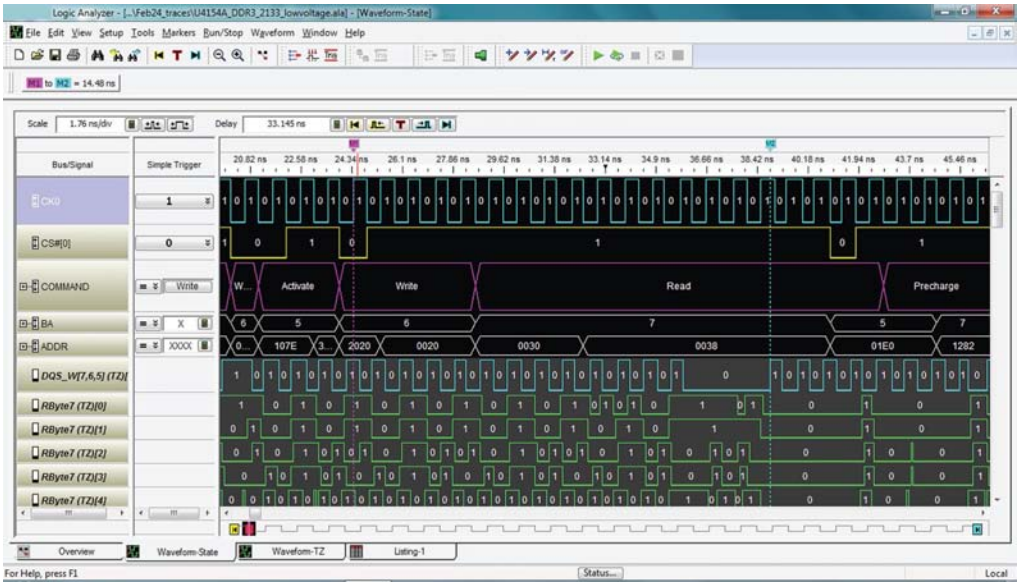


Figure 3. Timing zoom can be used to measure the time between the rising edge of the clock and the rising edge of DQS in a DDR system.

Deep Trace Captures

Using memory depth options, transitional timing and state mode store qualification triggers

Available memory depth of up to 400 M samples allows you to debug very complex problems where the cause and symptoms may be separated by several seconds. The amount of memory can be upgraded after purchase; see “Upgrades” in “Ordering Information” section of this document.

No need to sacrifice sampling resolution to view more system activity. In timing mode, if your system has bursts of activity followed by times with little activity, you can use transitional timing along with the logic analyzer’s deep memory to capture seconds to minutes of activity at 400 ps (2.5 GHz), 200 ps (5 GHz), or 100 ps (10 GHz) sampling resolutions. You also have the flexibility to increase the amount of time captured by excluding certain buses or signals from the transition detector, for example clock or strobe signals, that add little useful information to a state mode measurement.

In state mode, use store qualification to save only states of interest into memory. Figure 4 shows a store qualification trigger for state mode that stores only valid mode register settings for DDR memories, allowing deep capture of only the MRS commands. The MRS command is a “favorite” trigger that can be “recalled” from any Keysight default probing configuration for DDR memory. Other “favorite” store qualification triggers include “Filter NOP, trigger on first valid command,” which is where the valid commands and enough samples to capture the DQ bursts for DDR memory transactions are stored and “Deselected” or “NOP” states are not stored, conserving logic analyzer memory depth.

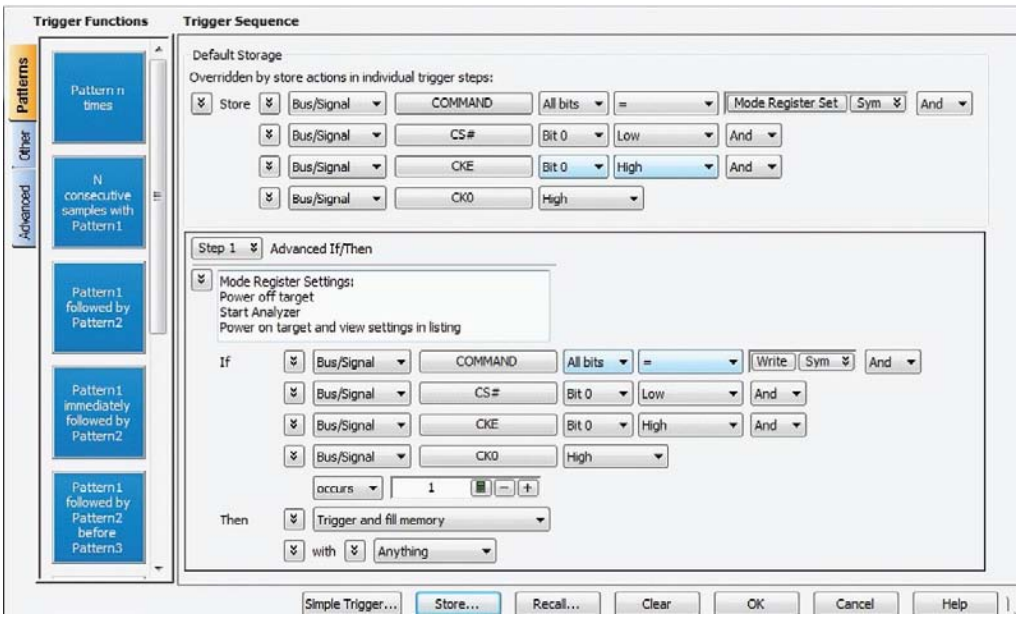


Figure 4. Mode register trigger allows you to capture key events during initialization without wasting valuable memory.

DDR Measurements Made Fast, Easy, and Powerful

The DDR setup assistant simplifies measurement setup and minimizes the time to make your first measurement. The DDR setup tool guides you through even the most complex state mode DDR/LPDDR setup in minutes. DDR eye scan makes it easy to determine the optimum acquisition sample point without requiring an oscilloscope. Keysight-qualified scans place the sample position at the center of the eye on every individual channel for maximum data capture reliability, including separate sampling positions for read and write data. The DDR setup assistant includes a variety of powerful, time-saving trigger features optimized for DDR measurements.

The DDR setup assistant tool is available at no charge as part of the Keysight B4661A memory analysis software package that can be downloaded from **www.keysight.com/find/B4661A**

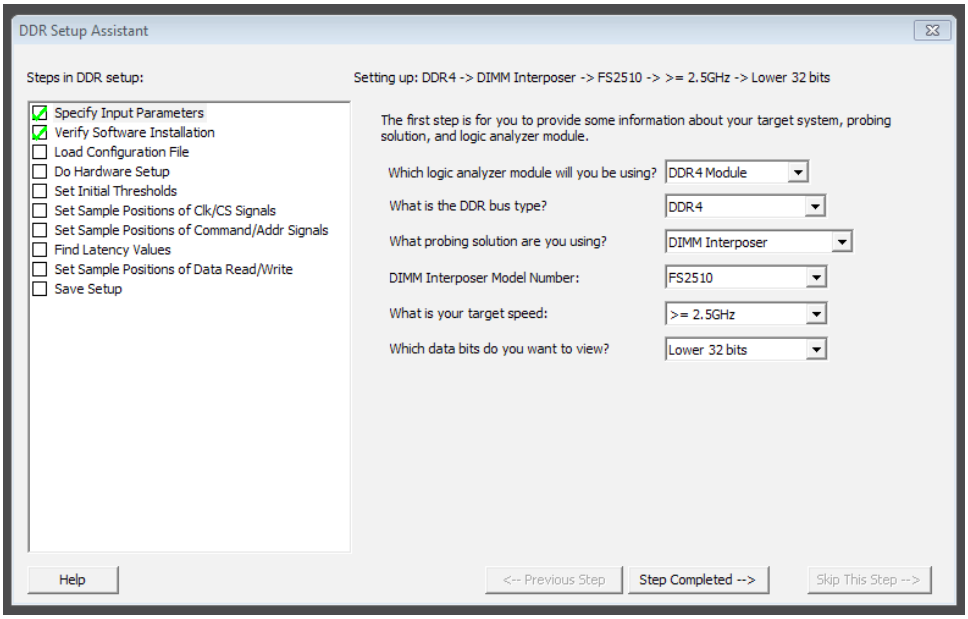


Figure 5. DDR setup assistant, with 10 simple steps, simplifies the setup of state mode measurements.

Burst Trigger and Trigger Macros

Burst trigger captures an entire data burst of eight on DDR or LPDDR memory systems from one sequence level in the trigger menu. Burst trigger is used in state mode. Up to four back-to-back bursts of eight sequential patterns can be captured. This enables capture of up to 32 sequential patterns at up to 4 Gb/s data rates from any high-speed digital system.

Intuitive trigger macros with diagrams provide visualization of triggering options and simplify the process of creating triggers.

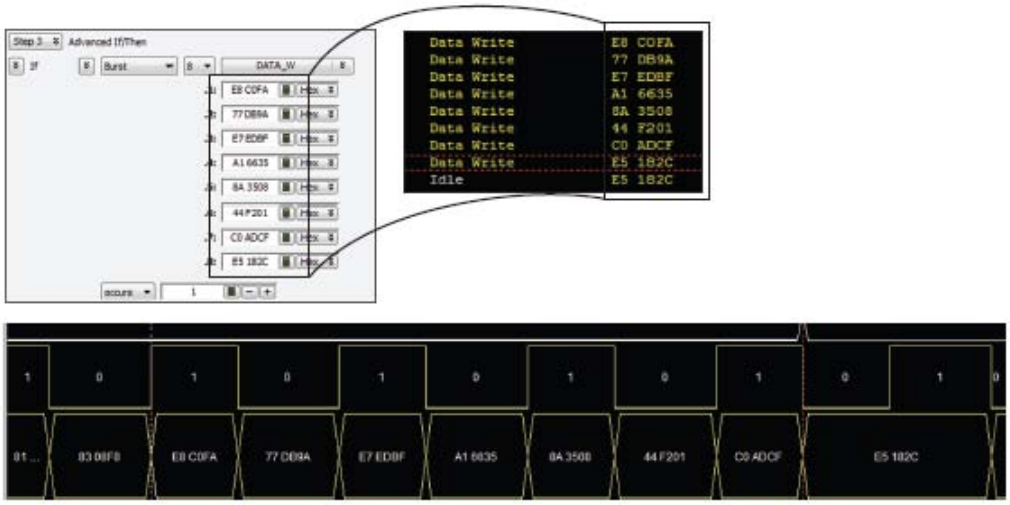


Figure 6. Burse recognizer trigger makes it easy to trigger on events in a burst read or write.

Signal Integrity Insight Made Fast and Easy

As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement in the design validation process. Eye scan lets you acquire qualitative signal integrity information in a matter of minutes on all the buses in your design under a wide variety of operating conditions.

- Identify problem signals quickly for further investigation with an oscilloscope.
- Results can be viewed for each individual signal or as a composite of multiple signals or buses.

The ability to qualify scans of any signal from any combination of other signals, full triggering capabilities for scan qualification, and customizable viewing windows allow you to sample only when the qualifying signal is active and see specific system activity of interest. Eye scan technology in the U4154B provides insights that can't be achieved as easily with any other test method. DDR eye scan automatically groups signals so you can quickly spot byte lane related signal integrity problems. Scans can be qualified based on state trigger criteria, providing unique insight. For example, read and write scans can be separated. Signal trace mode scan allows you to gather signal integrity information on two read or write cycles separated by only one cycle.

DDR eye scan is available at no charge as part of the Keysight B4661A memory analysis software package that can be downloaded from:
www.keysight.com/find/B4661A

Figure 7 shows a scan using signal trace mode where the samples in a DDR/LPDDR data burst are displayed in sequence. Figure 8 shows DDR3 DQ (data bits) scanned in overlay mode where the samples in the burst are scanned so that they overlay. Overlay mode provides the worst case eye, which allows for the most accurate sample position for the state mode sample positions.

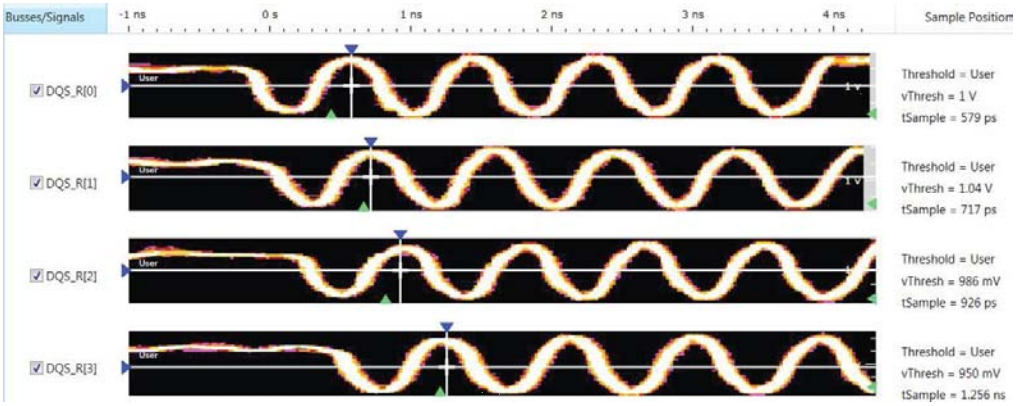


Figure 7. Burst qualified eye scan allows you to view the activity on the signals only when a burst is taking place. The screenshot above shows DDR4 2400 Mb/s read DQS 0-3 scanned in signal trace mode with no back-to-back bursts, allowing the user to view the DDR4 read strobes relative to each other, including the strobe pre-embles.

Signal Integrity Insight Made Fast and Easy (Continued)

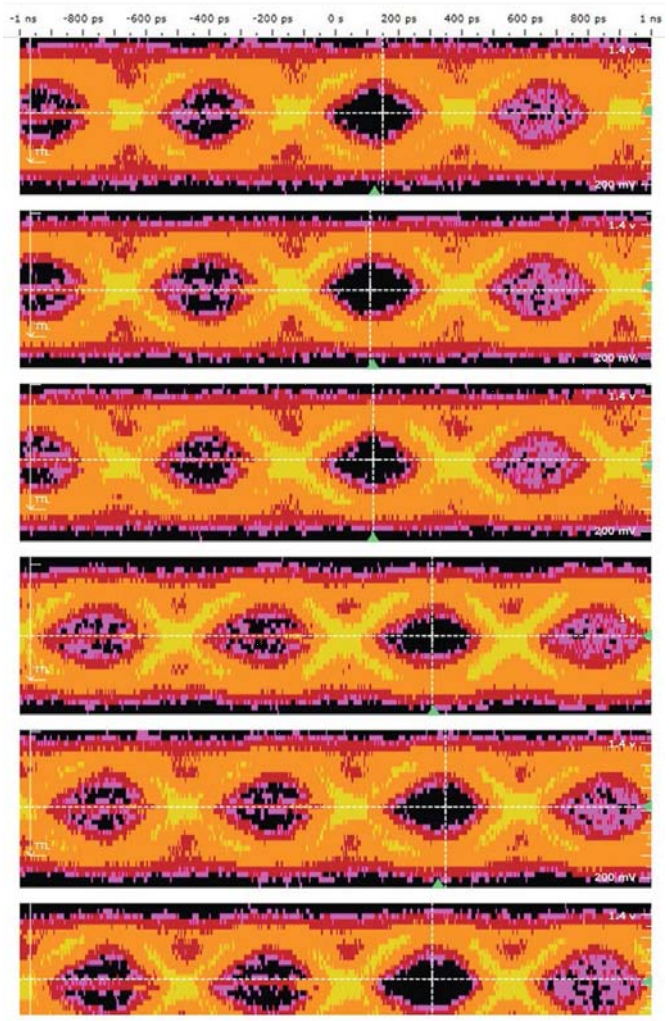


Figure 8. Eye scan clearly indicates the DDR3 byte lane shift caused by fly-by routing.

Harness your Logic Analyzer and Scope for Powerful Insight

Combine the powerful triggering and protocol analysis of a logic analyzer with the signal integrity insight of a scope to solve tough design problems. Keysight View Scope allows you to easily make time-correlated measurements between Keysight logic analyzers and oscilloscopes. The time-correlated logic analyzer and oscilloscope waveforms are integrated into a single logic analyzer waveform display for easy viewing and analysis. You can also trigger the oscilloscope from the logic analyzer (or vice versa), and automatically de-skew the two instruments. View Scope enables you to perform the following tasks more easily, quickly, and effectively:

- Validate signal integrity
- Track down problems caused by signal integrity
- Validate correct operation of A/D and D/A converters
- Validate correct logical and timing relationships between the analog and digital portions of a design

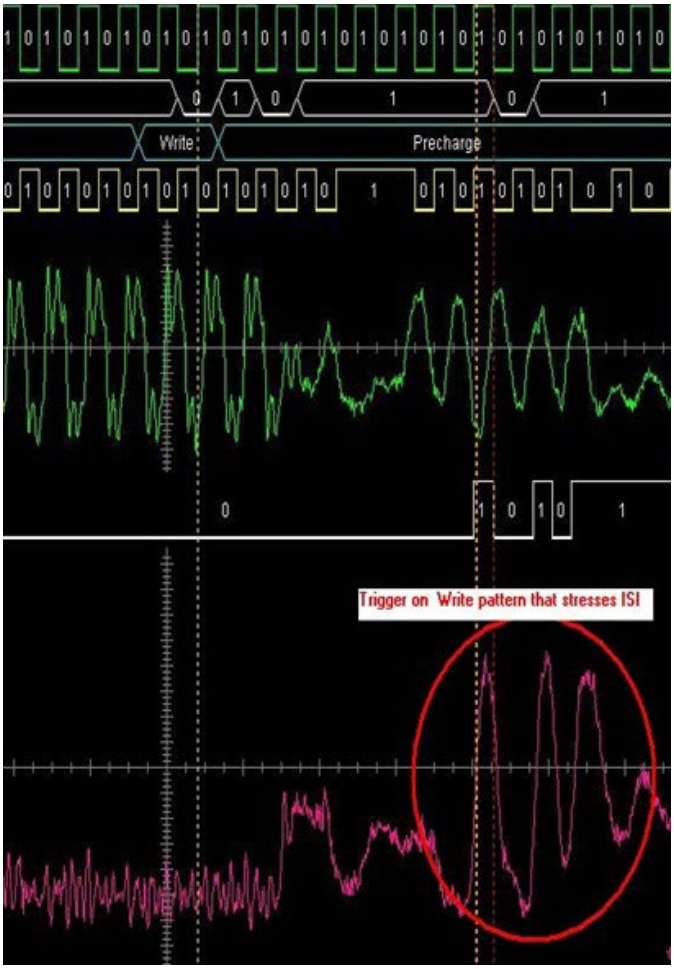


Figure 9. DQS0, DQ6 and CK0 from a DDR4 system probed by an Infiniium scope and displayed in the logic analyzer waveform using View Scope.

Programmability

You can write programs to control the logic analyzer application from remote computers on the local area network using COM. The COM automation server is part of the logic analyzer application. This software allows you to write programs to control loading, running, and storing configurations on the logic analyzer.

Operating Modes [1]

State operating modes	Conventional state sampling on both edges of the clock (synchronous)				Dual sample state sampling on one clock edge and using dual sample mode to capture rising and falling edge samples (synchronous)				Quad sample state sampling on one clock edge and using quad sample mode to capture rising and falling edge samples of both read and write DQ (data bits) on DDR4 or LPDDR4 (synchronous)
	Option -02G	Option -01G	Option -700	350 MHz (standard)	Option -02G	Option -01G	Option -700	350 MHz (standard)	Option -02G
Maximum acquisition rate	2.5 Gb/s	2.5 Gb/s	1.4 Mb/s	700 Mb/s	4 Gb/s	2.8 Gb/s	1.4 Gb/s	700 Mb/s	4 Gb/s
Number of available channels in one module	136	136	136	136	68	68	68	68	34
Number of available channels in a two module set	272	272	272	272	136	136	136	136	68
Number of available channels in a three module set	408	408	408	408	204	204	204	204	102

Timing operating modes	Conventional or transitional timing			
	Full channel	Half channel	Quarter channel Option -02G / -01G	All channels
Maximum acquisition rate	2.5 GHz	5 GHz	10 GHz	12.5 GHz
Number of available channels in one module	136	68	34	136
Number of available channels in a two module set	272	136	68	272
Number of available channels in a three module set	408	204	102	408

	State modes (synchronous)	Conventional and transitional timing modes (asynchronous)			Timing zoom
Memory depth (samples)	Conventional and dual-sample (all state speed options); Quad-sample (available with Option 02G only)	Full channel	Half channel	Quarter channel (requires Option 01G or 02G)	All options
Standard (base) memory	2 M	2 M	4 M	8 M	256 K
U4164A-004	4 M	4 M	8 M	16 M	256 K
U4164A-008	8 M	8 M	16 M	32 M	256 K
U4164A-016	16 M	16 M	32 M	64 M	256 K
U4164A-032	32 M	32 M	64 M	128 M	256 K
U4164A-064	64 M	64 M	128 M	200 M	256 K
U4164A-128	128 M	128 M	200 M	400 M	256 K
U4164A-200	200 M	200 M	400 M	800 M	256 K
U4164A-400	400 M	400 M	800 M	1.6 G	256 K

Contact Keysight Technologies for information on additional configurations.
Note: Memory can be upgraded after purchase. See “Upgrades” in “Ordering Information.”

1. Defined for general purpose use models. For DDR/LPDDR memory applications, either dual-sample or quad-sample modes are used for read/write separation. Quad-sample mode is used to capture rising and falling edge samples of both read and write DDR/LPDDR DQ signals for data rates up to 4 Gb/s from a single probe point. Dual-sample mode is used to capture read and write data instead of higher data rates. Using dual sample mode instead of quad sample mode requires, double probing of DDR/LPDDR data (DQ) to capture data rates over 2.5 Gb/s.

Optional Hardware

When you need more channels or more functions

Multiframe allows you to combine 16 AXIe chassis. [1]
One or more Y1223A Multiframe cables to connect multiple frames. Order one fewer Y1223A cables than the total number of frames/chassis to be combined.

1. One PC host is recommended for each AXIe chassis.

Optional Software

B4661A memory analysis software

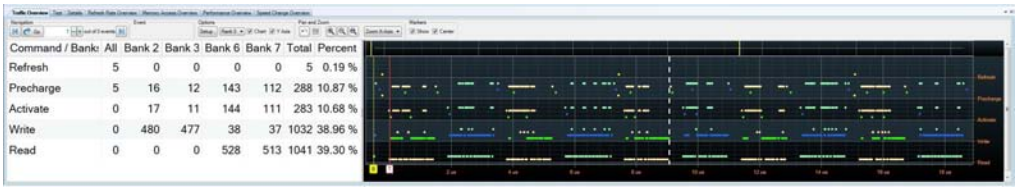
The Keysight B4661A memory analysis software offers a suite of tools that include the industry's first protocol compliance violation testing capability across speed changes, a condensed traffic overview for rapid navigation to areas of interest in the logic analyzer trace, powerful performance analysis graphics, and DDR and LPDDR decoders. With the B4661A memory analysis software and a Keysight logic analyzer, users can monitor DDR3/4 or LPDDR2/3/4 systems to debug, improve performance, and validate protocol compliance. Powerful traffic overviews, multiple viewing choices, and real-time compliance violation triggering help identify elusive DDR/LPDDR system violations.

The Keysight B4661A memory analysis software provides four standard software features and four licensed memory analysis options.

B4661A standard software features
- Default configurations for DDR and LPDDR probing solutions for Keysight logic analyzers
- DDR setup assistant
- DDR eye finder/eye scan
- DDR configuration creator

B4661A licensed software options
- DDR decoder with physical address trigger tool (B4661A-1xx)
- LPDDR decoder (B4661A-2xx)
- DDR and LPDDR compliance violation analysis (B4661A-3xx)
- Post-process compliance violation analysis real-time compliance violation analysis
- DDR3/4 and LPDDR2/3/4 performance analysis (B4661A-4xx)

Optional Software (Continued)



Command / Bank:	All	Bank 2	Bank 3	Bank 6	Bank 7	Total	Percent
Refresh	5	0	0	0	0	5	0.19 %
Precharge	5	16	12	143	112	288	10.87 %
Activate	0	17	11	144	111	283	10.68 %
Write	0	480	477	38	37	1032	38.96 %
Read	0	0	0	528	513	1041	39.30 %

Figure 10. Traffic overview example: Graphing command activity by commands and banks across the captured trace from the Keysight logic analyzer.

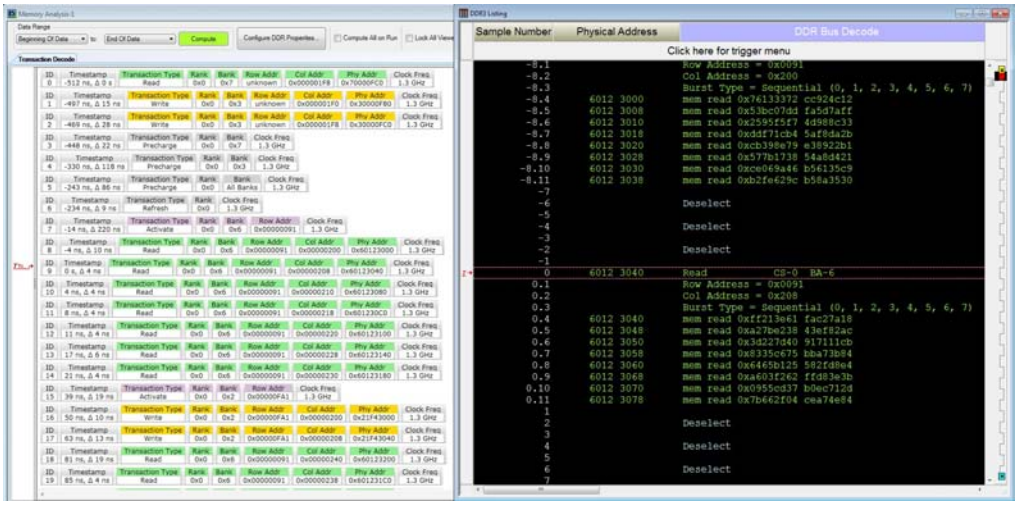


Figure 11. Transaction decode in the performance analysis option, provides a high-level view that is time-correlated to the listing window where each state is viewed using the DDR bus decoder. (The transaction decode also includes a details window to see the data associated with each read or write transaction.)

Optional Software (Continued)

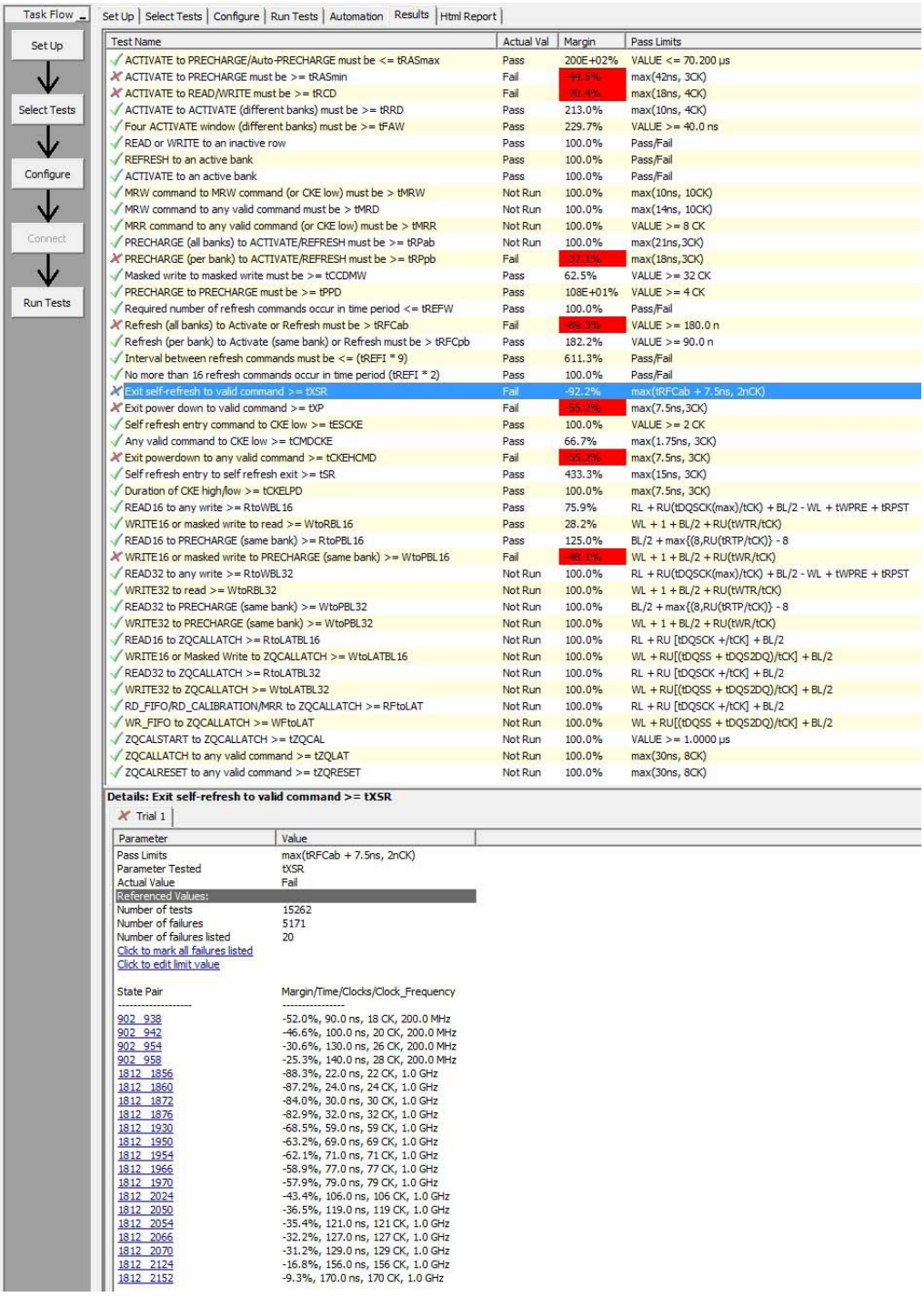


Figure 12. The post-process compliance tool includes hyperlinks to quickly jump to and/or mark violations and worst-case violations in the logic analyzer traces, transaction overview, and listing windows.

Probe/Cables As Required to Connect to the Target System

Direct connect probes – Probes that connect directly between a connector or footprint on the device under test and the front panel connector of the logic analyzer.

Probe type	Model number	Channels	Maximum data rate	Supported signal types	Comments
Connectorless, Soft Touch Pro	U4206A	34	4 Gb/s	Single-ended data, Differential or single-ended clock	Compatible with the U4164A only. Requires one U4206A per U4164A module. Use only for U4164A quad-sample state or quarter channel timing modes. Refer to U4206A user guide for example that allows for mixed modes of operation (e.g. quad-sample is selectable by pod pair)
Connectorless, Soft Touch Pro	U4204A	34	4 Gb/s	Differential or single-ended data, Differential or single-ended clock	
Flying lead	U4203A	34	1.5 Gb/s	Single-ended data, Differential or single-ended clock	
Mictor	U4205A	34	600 Mb/s	Single-ended data, Single-ended clock	

Model number	Description	Maximum data rate	Comments
U4208A	Probe/cable, 61-pin ZIF, left wing, no RC, 160-pin direct connect to U4164A	3.2 Gb/s typical	Compatible with the U4164A only. For use with W4631A or W4636A DDR4 BGA interposers that include RC network to provide proper signal termination to the logic analyzer. Uses quad-sample state mode to capture DQ signals.
U4209A	Probe/cable, 61-pin ZIF, right wing, no RC, 160-pin direct connect to U4164A	3.2 Gb/s typical	Compatible with the U4164A only. For use with W4631A or W4636A DDR4 BGA interposers. Includes RC network to provide proper signal termination to the logic analyzer. Uses quad-sample state mode to capture DQ signals.

Probe/Cables As Required to Connect to the Target System (Continued)

General purpose probes as required to connect to the target system. (Probes in this chart require U4201A cables.)

Probe type	Model number	Channels	Maximum data rate	Supported signal types	Number of U4201A required per probe
Soft Touch Connectorless Pro Series	E5406A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock	1 for each E5406A
Soft Touch Connectorless Low Profile	E5402A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock	1 for each E5402A
Soft Touch Connectorless Classic	E5390A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock	1 for each E5390A
Soft Touch Connectorless Half-size	E5398A	17 (16 data, 1 clock)	4 Gb/s	Single-ended data, differential or single-ended clock	1 for every E5398A
Soft Touch Connectorless Pro Series	E5405B	17 (16 data, 1 clock)	4 Gb/s	Differential or single-ended data, differential or single-ended clock	1 for every 2 E5405B
Samtec connector	E5378A	34 (32 data, 2 clock)	1.5 Gb/s	Single-ended data, differential or single-ended clock	1 for each E5378A
Samtec connector	E5379A	17 (16 data, 1 clock)	1.5 Gb/s	Differential or single-ended data, differential or single-ended clock	1 for every 2 E5379A
Mictor connector	E5380B	34 (32 data, 2 clock)	600 Mb/s	Single-ended data, differential or single-ended clock	1 for each E5380B
General purpose flying leads	E5382B	17 (16 data, 1 clock)	1.5 Gb/s	Single-ended data, differential or single-ended clock	1 for every 2 E5382B
General purpose flying leads	E5381B	17 (16 data, 1 clock)	1.5 Gb/s	Differential or single-ended data, differential or single-ended clock	1 for every 2 E5381B

Recommended probes for DDR and LPDDR memory include BGA probes, interposers, and Soft Touch mid-bus probes. Interposers are available from FuturePlus Systems or through Keysight. Refer to “Ordering Information.” Information on FuturePlus interposers http://www.futureplus.com/DDR3-Memory/keysight-la-support-overview.html.

For additional DDR/2/3/4 and LPDDR/2/3/4 probing options, contact your local Keysight representative www.keysight.com/find/contactus.

U4164A State Speed Option Requirements for DDR/LPDDR Data Rates

U4164A Requires

- Chassis and host PC
- Cables and/or probing to connect to the DUT
- Version 6.20 or higher of the logic and protocol analyzer software
- Host PC running compatible 64-bit OS (refer to logic and protocol analyzer software download site for latest supported operating systems)

U4164A Includes

- Qty (1) U4164A logic analyzer module
- Qty (2) U4154-61602 flex cables for connecting multiple U4164A modules into module sets

For capture of DDR/LPDDR memory ADD/CMD/DATA

DDR/LPDDR data rates		Base state clock rate: 350 MHz clock [1]	Option 700: 700 MHz clock [1]	Option 01G: 1.4 GHz clock [1]	Option 02G: 2.5 GHz clock [2]
DDR or LPDDR	≤ 700 Mb/s	√	√	√	√
DDR2	≤ 700 Mb/s	√	√	√	√
DDR3	≤ 1400 Mb/s		√	√	√
	≤ 2500 Mb/s			√	√
	> 2500 Mb/s				√
DDR4	≤ 2500 Mb/s			√	√
	> 2500 Mb/s				√
LPDDR2	≤ 1400 Mb/s		√	√	√
LPDDR3	≤ 1400 Mb/s		√	√	√
	≤ 2500 Mb/s			√	√
LPDDR4	≤ 2500 Mb/s			√	√
	> 2500 Mb/s				√

1. Requires dual sample state mode for simultaneous read/write data capture.
2. Requires dual sample state or quad sample mode for simultaneous read/write data capture. Dual sample state mode requires double probing of DQ over 2.5 Gb/s. Quad-sample state mode operates from a single probe load.

Minimum Hardware

Module quantity considerations

The following table provides examples of general guidelines for the number of U4164A modules required for a few example applications. Refer to the requirements of your specific devices, interposers and probes to determine the requirements for your application.

DUT configuration	U4164A module requirements
General purpose measurement requiring a given number of channels on a single time base	Each U4164A has 136 channels. A maximum of three U4164As can be combined for 408 channels
DDR4 DIMM Interposer, > 2.5 Gb/s data rates, capture all ADD/CMD/data	Three U4164A modules, each with Option 02G
DDR2/3/4, 64-bit data, ≤ 2.5 Gb/s data rates, capture all ADD/CMD/data (read and write)	Two U4164A modules, each with Option 01G
LPDDR1/2/3/4, ≤ 2.5 Gb/s data rates	One U4164A module
LPDDR4, > 2.5 Gb/s data rates	May require up to three U4164A modules (depends on the number of data signals probed and the probing layout) [1]

1. To determine the number of channels, and therefore the number of modules, required for a DDR/LPDDR memory system operating at > 2.5 Gb/s, allocate four U4164A channels for each DDR/LPDDR memory DQ captured.

Chassis and controller considerations

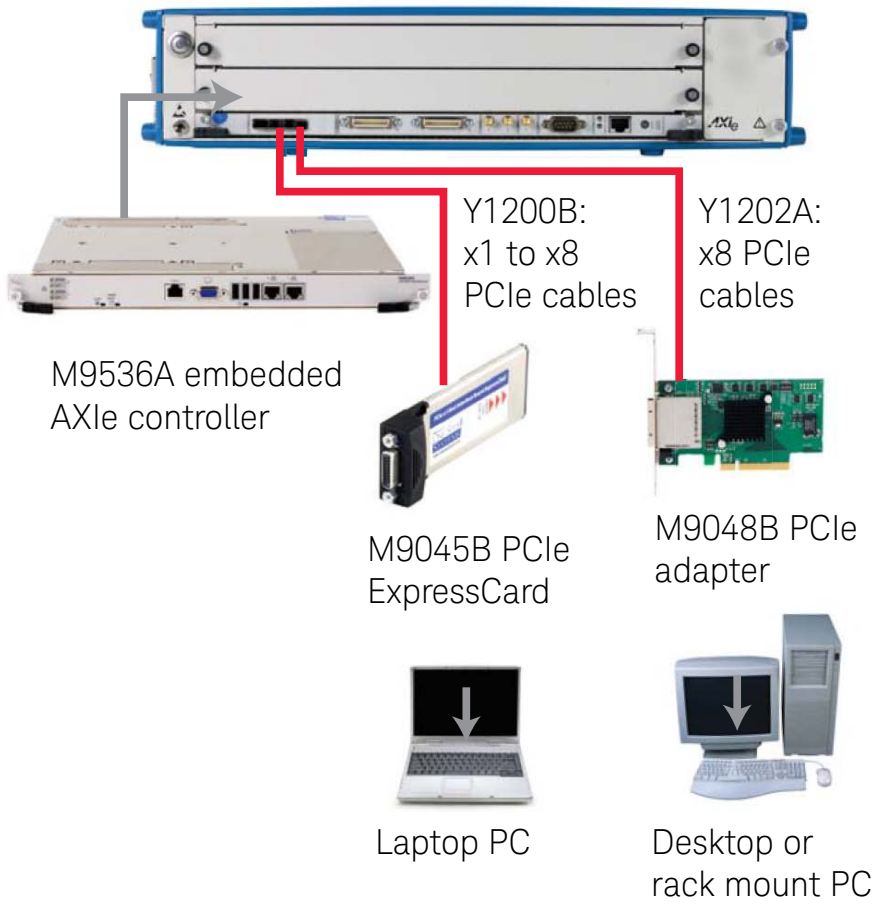


Figure 13.

Minimum Hardware (Continued)

Chassis and controller considerations (Continued)

- There are three host PC possibilities for an AXIe chassis - M9536A embedded controller, external laptop PC, or external desktop PC. Select one of the host PC configurations above for your U4164A system
- If you're using a laptop or desktop PC, see 5990-7632EN for a list of tested computers
- An M9505A 5-slot chassis is required when using a U4164A three-module set or a U4164A two-module set when used with an M9536A embedded controller as the M9536A is installed in the bottom slot (slot 1) of the chassis
- Version 6.20 or higher of the logic and protocol analyzer software needs to be installed on the host PC. Refer to the software download site for the latest supported operating systems

Cables

Up to four U4201A logic analyzer cables may be required per U4164A module depending on probing method. See probing chart for details. Interposers with direct connect cabling, such as the FuturePlus FS2510AB DDR4 DIMM interposer, do not require additional U4201A cables.

Typical Configurations

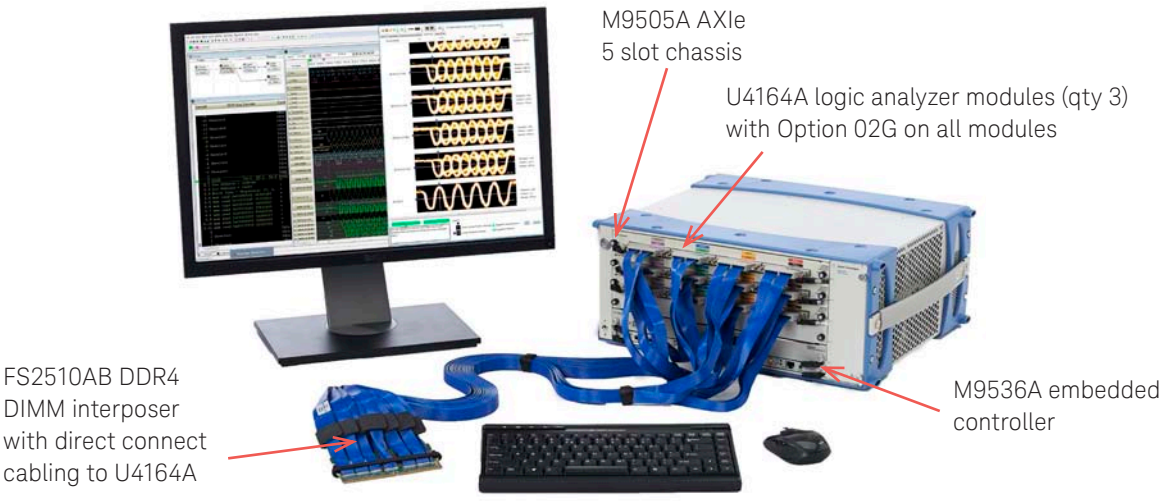


Figure 14. Typical configuration for DDR4 DIMM debug and validation for data rates greater 2500 Mb/s.

Recommended configuration for DDR4 DIMM solution over 2.5 Gb/s data rates		
Model	**Quantity**	**Description**
U4164A	3	Logic analyzer module, 136 channel, 12.5 GHz TZ, 5 GHz timing, 350 MHz base state speed, 2 Mb
U4164A-02G	3	Increase maximum speeds: state to 4 Gb/s (2.5 GHz) and timing to 10 GHz
M9505A	1	AXIe 5 slot chassis
M9536A	1	AXIe Embedded controller or M9045B or M9048A PCI Express® adaptors
FS2510AB with FS1070		DDR4 DIMM interposer from FuturePlus Systems. Available through Keysight

Note: M9536A controller, if used, must be installed in slot 1.

Typical Configurations (Continued)

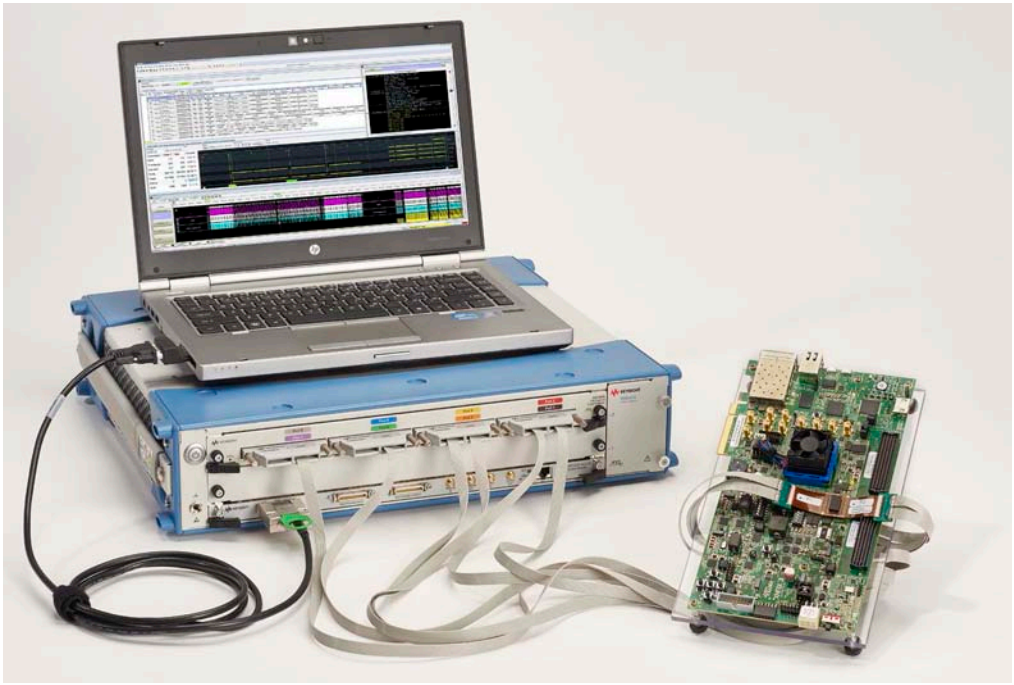


Figure 15. Typical DDR4 BGA interposer configuration for data rates up to 3.2 Gb/s.

DDR4 BGA Interposer Configurations for use with U4164A Quad Sample State Mode

DDR4 DRAM type	Data width	DDR4 signal access	BGA interposer	Probe cables (qty)	Logic analyzer compatibility	Order summary model/option (qty)
x4	x4	Command, Address, Control and Data	W4643A	U4208A (1) U4209A (1)	U4164A only (with Option -02G)	U4164A (1) [1] U4164A-02G (1) W4643A U4208A (1) U4209A (1)
x8	x8					
x16	x16	Command, Address, Control and Data	W4641A	U4208A (1) U4209A (1)	U4164A only (with Option -02G	U4164A (1) [1] U4164A-02G (1) W4641A U4208A (1) U4209A (1)

1. Using dual sample mode for simultaneous read/write data capture.

Related Products

Model	Description
U4301B	PCIe® Gen3 analyzer, base config 5 Gb/s, x1 linkwidth, 8 GB capture buffer
FS2510 AB	FuturePlus DDR4 DIMM Interposer
FS2512	FuturePlus DDR4 SODIMM Interposer

Technical Specifications and Characteristics

All specifications refer to the combination of a U4164A logic analyzer module, U4201A logic analyzer probe cable, and any Keysight Soft Touch probe. Probe variations will influence results.

State (Synchronous) sampling mode	
Maximum state data rate Option 02G, 2.5 GHz state mode (spec)	2.5 Gb/s on 136 channels per U4164A, using either or both edges of clock (spec)
	4 Gb/s on 68 channels per U4164A, clocking on either edge of the clock (typ)
Maximum state data rate -01G 1.4 GHz state mode (spec)	2.5 Gb/s on 136 channels per U4164A, using both edges of clock (spec)
	2.8 Gb/s on 68 channels per U4164A, clocking on either edge of the clock (typ)
Maximum state data rate Option -700	1.4 Gb/s on 136 channels using both edges of clock (spec)
Maximum state data rate 350 MHz standard (base)	700 Mb/s on 136 channels using both edges of clock (spec)
Maximum state clock frequency (typ)	2.5 GHz Option -02G
	1.4 GHz Option -01G
	700 MHz Option -700
	350 MHz standard (base)
Minimum state clock frequency[1] (typ)	12.5 MHz (single edge)
	6.25 MHz (both edges)
Sample position adjustment resolution (typ)	5 ps or 20 ps
Sample position adjustment accuracy (typ)	± 150 ps
Minimum data valid window (typ)	100 ps
Minimum setup time (typ)	50 ps
Minimum hold time (typ)	50 ps
Minimum eye height (typ)	100 mV
Sample position adjustment range (typ)	7 ns
Minimum state clock pulse width (typ)	200 ps
Number of clocks (nom)	1
Minimum time between active clock edges (typ)	400 ps
Maximum time between active clock edges 1 (typ)	80 ns
Number of clock qualifiers	4 (pods 2, 3, 4, and 5 on clocking module)
Clock qualifier setup time	150 ps
Clock qualifier hold time	150 ps
Number of “RESET” clock qualifiers	1 (pod 7 of clocking module)
“RESET” clock qualifier setup time	2 ns
“RESET” clock qualifier hold time	0 ps
Time tag resolution (typ)	80 ps
Maximum time count between stored states (typ)	66 days

1. Clock can pause for up to 66 days once every 8 or more edges.

Technical Specifications and Characteristics (Continued)

Timing (Asynchronous) sampling mode			
	Full-channel mode	**Half-channel mode**	**Quarter-channel mode**
Maximum time between transitions (nom)	66 days		
Minimum data pulse width (typ)	1 sample period + 200 ps		
Time interval accuracy (typ)	± (1 sample period + 400 ps + 0.01% of time interval reading)		
Maximum sample rate (nom)	2.5 GHz	5 GHz	10 GHz
Minimum sample period (nom)	400 ps	200 ps	100 ps
Pod usage (nom) 1 pod from each	All pods	Odd from each odd/even pod pair	Even signal inputs (0, 2, 4, 6, 8) from odd pod of each odd/even pair plus clock input
Timing Zoom (Asynchronous) sampling mode			
Timing Zoom sampling rate (nom)		12.5 GHz	
Timing Zoom memory depth (nom)		256 K samples	
Trigger characteristics			
Maximum trigger sequence speed (typ)		2500 MHz (400 ps) Option -02G	
		1400 MHz (714 ps) Option -01G	
		700 MHz (1.428 ns) Option -700	
		350 MHz (2.856 ns) standard (base) module	
Trigger resources (nom)		16 patterns evaluated as =, ! =, >, > =, <, < =	
		8 double-bounded ranges evaluated as in range, not in range	
		4 to 8 burst detectors	
		4 edge detectors in timing, 3 in transitional timing	
		1 occurrence counter persequence level	
		1 timer	
		3 flags	
		1 arm in	
Trigger resource Boolean conditions (nom)		Arbitrary Boolean combinations	
Trigger actions (nom)		Goto	
		Trigger and fill memory	
		Trigger and Goto	
		Trigger, send e-mail, and fill memory	
Store qualification actions (nom)		Default (global) and per sequence level	
		Store/don't store sample	
		Turn on/off default storing	
Timer actions		Start from reset	
		Stop and reset	
		Pause	
		Resume	
Flag actions		Set	
		Clear	
		Pulse set	
		Pulse clear	

Technical Specifications and Characteristics (Continued)

Trigger characteristics (Continued)	
Maximum trigger sequence levels (nom)	8
Trigger sequence level branching (nom)	Arbitrary 4-way if/then/else
Trigger position (nom)	Start, center, end, or user-defined
Maximum occurrence counter (nom)	999,999,999
Maximum pattern width (nom)	128 bits – single label
	408 bits – AND of multiple labels across three-card set
Maximum range width (nom)	64 bits
Timer range (nom)	100 ns to 27 hours (in timing modes)
	200 * state clock period to 27 hours (in state mode)
Timer resolution (nom)	5 ns
Timer accuracy (typ)	± (5 ns + 0.01%) (in timing modes)
	± (8 * state clock period + 2 ns + 0.01%) (in state mode)
Timer reset latency (nom)	40 ns (in timing modes)
	80 * state clock period (in state mode)
General	
Number of channels (nom)	136 in one U4164A
	272 in two U4164As combined
	408 with three U4164A combined
Maximum channels on a single time base and trigger (nom)	408
Number of analyzers (nom)	1
Input signal amplitude V_{amptd} (typ)	≥ 350 mV
Supported signal types	Single-ended and differential
Voltage threshold (typ)	–5 to +5 V
	–4 to +4 V when in dual sample or quad sample state modes
Minimum threshold resolution (typ)	2 mV
Threshold accuracy (typ)	± (30 mV + 1% of setting)
Threshold setting granularity	By channel

Environmental and Physical

Operating environment	
Temperature (nom)	0 to +40 °C
Humidity (nom)	0 to 80% relative humidity at 40 °C
Altitude	0 to 3000 m
Vibration	Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 0.2 g rms
Non-operating environment	
Temperature (nom)	–40 to +75 °C
Humidity (nom)	0 to 90% relative humidity at 65 °C
Altitude	0 to 15,300 m
Vibration (in shipping carton)	Random vibration 5 to 500 Hz
	10 minutes per axis
	Approximately 2.41
	Swept sine resonant search
	5 to 500 Hz
	0.50 g (0-peak)
	5 minute resonant dwell at 4 resonances per axis
Weight	2.34 kg

Definitions for specifications

Specification (spec): Represents warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 to 40 °C, unless otherwise stated, and after a 45 minute warm-up period. The specifications include measurement uncertainty. Data represented in this document are specifications unless otherwise noted.

Typical (typ): Represents characteristic performance, which 80% of the instruments manufactured will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 25 °C).

Nominal (nom): The expected mean or average performance, or an attribute whose performance is by design, such as the 50 Ω connector. This data is not warranted and is measured at room temperature (approximately 25 °C).

Measured (meas): An attribute measured during the design phase for purposes of communicating expected performance, such as amplitude drift vs. time. This data is not warranted and is measured at room temperature (approximately 25 °C).

Ordering

Model	Description
U4164A	Logic analyzer module, 136 ch, 12.5 GHz TZ, 5 GHz timing, 350 MHz base state speed, 2 Mb (memory depth in samples)
U4164A-A6J	ANSI Z540-1-1994 calibration
State and timing speed options	
U4164A-700	Increase maximum state speed to 700 MHz
U4164A-01G	Increase maximum speeds: state to 2.8 Gb/s (1.4 GHz) and timing to 10 GHz
U4164A-02G	Increase maximum speeds: state to 4 Gb/s (2.5 GHz) and timing to 10 GHz
Memory depth options	
U4164A-004	Increase acquisition memory depth to 4 Mb
U4164A-008	Increase acquisition memory depth to 8 Mb
U4164A-016	Increase acquisition memory depth to 16 Mb
U4164A-032	Increase acquisition memory depth to 32 Mb
U4164A-064	Increase acquisition memory depth to 64 Mb
U4164A-128	Increase acquisition memory depth to 128 Mb
U4164A-200	Increase acquisition memory depth to 200 Mb
U4164A-400	Increase acquisition memory depth to 400 Mb
Cables, chassis, and embedded controller	
U4201A	Logic analyzer cable for connecting U4161A to 90-pin E53xx and E54xx Series probes
N2815A	MSO/logic analyzer cable for connecting U4164A to 90-pin logic analyzer probes. (Connects even and/or odd headers of E53xx and E54xx Series 90-pin probes into odd pod of U4164A pod pair only. Useful for dual-sample state mode, not for full-channel mode)
M9502A	AXIe 2-slot chassis
M9505A	AXIe 5-slot chassis
Y1223A	Multiframe cable
M9536A	AXIe embedded PC controller
M9536A-M16	Memory upgrade from 8 GB to 16 GB RAM
Upgrades for U4164A logic analyzer modules (after purchase)	
U4164A state and timing speed upgrades	
U4164AU-700	Increase maximum state speed to 700 MHz
U4164AU-01G	Increase maximum speeds: state to 2.8 Gb/s (1.4 GHz) and timing to 10 GHz
U4164AU-02G	Increase maximum speeds: state to 4 Gb/s (2.5 GHz) and timing to 10 GHz
U4164A memory depth upgrades	
U4164AU-004	Increase acquisition memory depth to 4 Mb
U4164AU-008	Increase acquisition memory depth to 8 Mb
U4164AU-016	Increase acquisition memory depth to 16 Mb
U4164AU-032	Increase acquisition memory depth to 32 Mb
U4164AU-064	Increase acquisition memory depth to 64 Mb
U4164AU-128	Increase acquisition memory depth to 128 Mb
U4164AU-200	Increase acquisition memory depth to 200 Mb
U4164AU-400	Increase acquisition memory depth to 400 Mb

Ordering (Continued)

Optional software

B4661A	Memory analysis software for logic analyzers. Standard features for DDR/LPDDR include default configurations, Setup Assistant, Configuration Creator, and Eye Finder and Eye Scan.
Fixed perpetual licenses	
B4661A-1FP	DDR decoder with physical address trigger tool, fixed perpetual license
B4661A-2FP	LPDDR decoder, fixed perpetual license
B4661A-3FP	DDR and LPDDR compliance violation analysis, fixed perpetual license
B4661A-4FP	DDR3/4 and LPDDR2/3/4 performance analysis, fixed perpetual license
Transportable perpetual licenses	
B4661A-1TP	DDR decoder with physical address trigger tool, transportable perpetual license
B4661A-2TP	LPDDR decoder, transportable perpetual license
B4661A-3TP	DDR and LPDDR compliance violation analysis, transportable perpetual license
B4661A-4TP	DDR3/4 and LPDDR2/3/4 performance analysis, transportable perpetual license
Floating/server perpetual licenses	
B4661A-1NP	DDR decoder with physical address trigger tool, network/floating perpetual license
B4661A-2NP	LPDDR decoder, network/floating perpetual license
B4661A-3NP	DDR and LPDDR compliance violation analysis, network/floating perpetual license
B4661A-4NP	DDR3/4 LPDDR2/3/4 performance analysis, network/floating perpetual license
Other software	
B4601A	Data import tool
B4601C	Signal-to-parallel analysis pacakage
B4602A	Signal extractor tool
B4655A	FPGA dynamic probe for Xilinx
B4656A	FPGA dynamic probe for Altera

Probes and interposers

Direct connect probes	
U4203A	Single-ended 34-channel flying lead
U4204A	Soft Touch Pro Series single-ended 34-channel data, differential clock connectorless probe
U4205A	Single-ended 34-channel Mictor connector probe
U4206A	34-channel, Soft Touch Pro, single-ended, quad x 160-pin direct connect

Ordering (Continued)

General purpose probes (require U4201A cables)	
E5405B	Pro Series soft touch connectorless probe - differential, for 90-pin cable (17 channels)
E5406A	Pro Series soft touch connectorless probe - single-ended, for 90-pin cable (34 channels)
E5402A	Low profile, Pro Series soft touch connectorless probe - single-ended, for 90-pin cable
E5390A	Soft touch connectorless probe-single-ended, with 90-pin cable connectors
E5398A	Half-size soft touch connectorless probe with 90-pin cable connectors
E5381B	Differential flying leads, 17 channels
E5382B	Single-ended flying leads, 17 channels
E5378A	Samtec probe-single-ended, with 90-pin cable connectors
E5379A	Samtec probe-differential, with 90-pin cable connectors
E5380B	Mictor probe-single-ended, with 90-pin cable connectors
DDR4 probes/interposers	
W4641A	Interposer, DDR4 x16 BGA 2-wing single-touch DQ, used with quad-sample mode, requires one U4208A left ZIF probe cable and one U4209A right ZIF probe/cable
W4643A	Interposer, DDR4 x4/x8 BGA 2-wing single-touch DQ, used with quad-sample mode, requires one U4208A left ZIF probe cable and one U4209A right ZIF probe/cable
W4631A	Interposers, DDR4 x16 BGA 4-wing double probed DQ, used with dual sample mode and two E5849A ZIF cables or one DDR4 x16 ZIF cable for W4631A
W4633A	Interposer, DDR4 x4/x8 BGA 3-wing double probed DQ, used with dual sample mode and two E5849A ZIF cables
W4636A	Interposer, 96 ball BGA, DDR4 x16 2-wing command and reduced data for LA
E5849A	Cable, high data rate ZIF for use with W4631A and W4633A DDR4 double probed DQ BGA interposers
FuturePlus FS2510AB	DDR4 3300 DIMM interposer (optional FS1070 conversion kit for FS2510 for data rates over 2.5 Gb/s)
FuturePlus FS2512	DDR4 1867 SODIMM interposer
DDR3 probes/interposers	
W3631A	DDR3 x16 BGA stacked DRAM under 2 G deep command and data probe for logic analyzer and scope
W3633A	DDR3 x4/x8 BGA command and data probe for logic analyzer and scope
W3636A	DDR3 x16 BGA single die command and data probe for logic analyzer and scope (covers > 2 G), for non-stacked DRAM
E5847A	46-ch single-ended ZIF probe for DDR3 x4/x8 DRAM BGA probe connection to 90-pin logic analyzer cable
E5845A	46-ch single-ended ZIF probe for DDR3 x16 DRAM BGA probe connection to 90-pin logic analyzer cable
FuturePlus FS2352B	DDR3 2133 DIMM interposer
FuturePlus FS2354	DDR3 1600 SODIMM interposer
DDR2 probes/interposers	
W2631B	DDR2 x16 BGA ADD/CMD/DATA probe for logic analyzers and scopes
W2633B	DDR2 x4/x8 BGA ADD/CMD/DATA probe for logic analyzers and scopes

Warranty and Calibration

Advantage services: calibration and warranty	
Keysight Advantage Services is committed to your success throughout your equipment's lifetime.	
Calibration	**Description**
Select Keysight calibration plan	
R1282A R-50C-011-3	3-year calibration assurance plan (return to Keysight): Priority calibration service covering all calibration costs for 3 years; 15% cheaper than buying stand-alone calibrations.
R1282A R-50C-011-5	5-year calibration assurance plan (return to Keysight): Priority calibration service covering all calibration costs for 5 years; 20% cheaper than buying stand-alone calibrations.
R1282A R-50C-021-3	ANSI Z540-1-1994 calibration – 3 years
R1282A R-50C-021-5	ANSI Z540-1-1994 calibration – 5 years
Warranty	**Description**
Select coverage	
R1280A included	3-year warranty (return to Keysight), standard
R1280A R-51B-001-5Z	5-year warranty assurance plan (return to Keysight): Priority warranty service includes one-time coverage for an EOS/ESD failure.

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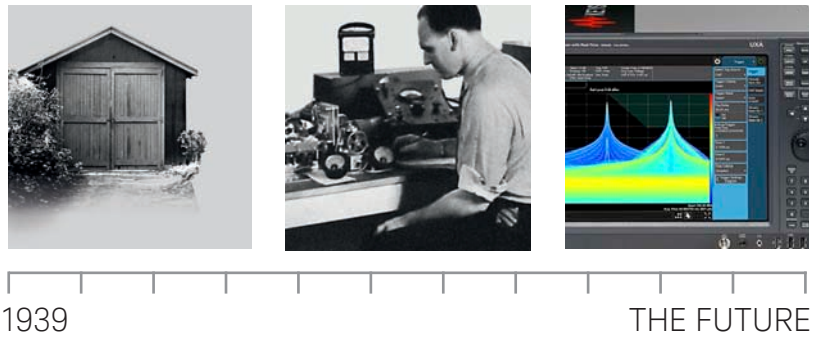
For more than 75 years, we've been helping you unlock measurement insights. Our unique combination of hardware, software and people can help you reach your next breakthrough. Unlocking measurement insights since 1939.



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