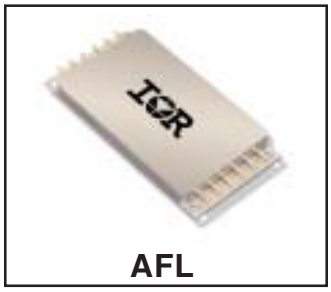
International
IOR Rectifier

PD-94458C

# AFL28XXD SERIES

## 28V Input, Dual Output

## HYBRID-HIGH RELIABILITY DC/DC CONVERTER




AFL

## Description

The AFL Series of DC/DC converters feature high power density with no derating over the full military temperature range. This series is offered as part of a complete family of converters providing single and dual output voltages and operating from nominal +28V or +270V inputs with output power ranging from 80W to 120W. For applications requiring higher output power, individual converters can be operated in parallel. The internal current sharing circuits assure equal current distribution among the paralleled converters. This series incorporates International Rectifier's proprietary magnetic pulse feedback technology providing optimum dynamic line and load regulation response. This feedback system samples the output voltage at the pulse width modulator fixed clock frequency, nominally 550KHz. Multiple converters can be synchronized to a system clock in the 500KHz to 700KHz range or to the synchronization output of one converter. Undervoltage lockout, primary and secondary referenced inhibit, soft-start and load fault protection are provided on all models.

These converters are hermetically packaged in two enclosure variations, utilizing copper core pins to minimize resistive DC losses. Three lead styles are available, each fabricated with International Rectifier's rugged ceramic lead-to-package seal assuring long term hermeticity in the most harsh environments.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are fabricated utilizing DSCC qualified processes. For available screening options, refer to device screening table in the data sheet. Variations in electrical, mechanical and screening can be accommodated. Contact IR Santa Clara for special requirements.

## Features

- 16V To 40V Input Range
- ±5V, ±12V, and ±15V Outputs Available
- High Power Density - up to 70W/in$^3$
- Up To 100W Output Power
- Parallel Operation with Power Sharing
- Low Profile (0.380") Seam Welded Package
- Ceramic Feedthru Copper Core Pins
- High Efficiency - to 87%
- Full Military Temperature Range
- Continuous Short Circuit and Overload Protection
- Output Voltage Trim
- Primary and Secondary Referenced Inhibit Functions
- Line Rejection > 40dB - DC to 50KHz
- External Synchronization Port
- Fault Tolerant Design
- Single Output Versions Available
- Standard Microcircuit Drawings Available

## Specifications

| Absolute Maximum Ratings | |
|---|---|
| Input voltage | -0.5V to +50VDC |
| Soldering temperature | 300°C for 10 seconds |
| Operating case temperature | -55°C to +125°C |
| Storage case temperature | -65°C to +135°C |

**Static Characteristics** -55°C ≤ $T_{CASE}$ ≤ +125°C, 16V≤ $V_{IN}$ ≤ 40V unless otherwise specified.

| Parameter | Group A Subgroups | Test Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT VOLTAGE** | | Note 6 | 16 | 28 | 40 | V |
| **OUTPUT VOLTAGE** | | $V_{IN}$ = 28 Volts, 100% Load | | | | |
| AFL2805D | 1 | Positive Output | 4.95 | 5.00 | 5.05 | |
| | 1 | Negative Output | -5.05 | -5.00 | -4.95 | |
| AFL2812D | 1 | Positive Output | 11.88 | 12.00 | 12.12 | |
| | 1 | Negative Output | -12.12 | -12.00 | -11.88 | |
| AFL2815D | 1 | Positive Output | 14.85 | 15.00 | 15.15 | |
| | 1 | Negative Output | -15.15 | -15.00 | -14.85 | |
| AFL2805D | 2, 3 | Positive Output | 4.90 | | 5.10 | V |
| | 2, 3 | Negative Output | -5.10 | | -4.90 | |
| AFL2812D | 2, 3 | Positive Output | 11.76 | | 12.24 | |
| | 2, 3 | Negative Output | -12.24 | | -11.76 | |
| AFL2815D | 2, 3 | Positive Output | 14.70 | | 15.30 | |
| | 2, 3 | Negative Output | -15.30 | | -14.70 | |
| **OUTPUT CURRENT** | | $V_{IN}$ = 16, 28, 40 Volts - Notes 6, 11 | | | | |
| AFL2805D | | Either Output | | | 12.8 | |
| AFL2812D | | Either Output | | | 6.4 | A |
| AFL2815D | | Either Output | | | 5.3 | |
| **OUTPUT POWER** | | Total of Both Outputs. Notes 6,11 | | | | |
| AFL2805D | | | 80 | | | |
| AFL2812D | | | 96 | | | W |
| AFL2815D | | | 100 | | | |
| **MAXIMUM CAPACITIVE LOAD** | | Each Output Note 1 | 10,000 | | | µF |
| **OUTPUT VOLTAGE TEMPERATURE COEFFICIENT** | | $V_{IN}$ = 28 Volts, 100% Load - Notes 1, 6 | -0.015 | | +0.015 | %/°C |
| **OUTPUT VOLTAGE REGULATION** | | Note 10 | | | | |
| Line | 1, 2, 3 | No Load, 50% Load, 100% Load | -0.5 | | +0.5 | |
| Load | 1, 2, 3 | $V_{IN}$ = 16, 28, 40 Volts. | -1.0 | | +1.0 | |
| Cross | | $V_{IN}$ = 16, 28, 40 Volts. Note 12 | | | | |
| AFL2805D | 1, 2, 3 | Positive Output | -1.0 | | +1.0 | % |
| | | Negative Output | -8.0 | | +8.0 | |
| AFL2812D | 1, 2, 3 | Positive Output | -1.0 | | +1.0 | |
| | | Negative Output | -5.0 | | +5.0 | |
| AFL2815D | 1, 2, 3 | Positive Output | -1.0 | | +1.0 | |
| | | Negative Output | -5.0 | | +5.0 | |

For Notes to Specifications, refer to page 4

**Static Characteristics** (Continued)

| Parameter | Group A Subgroups | Test Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| **OUTPUT RIPPLE VOLTAGE** | | $V_{IN}$ = 16, 28, 40 Volts, 100% Load, BW = 10MHz | | | | |
| AFL2805D | 1, 2, 3 | | | | 60 | |
| AFL2812D | 1, 2, 3 | | | | 80 | $mV_{pp}$ |
| AFL2815D | 1, 2, 3 | | | | 80 | |
| **INPUT CURRENT** | | $V_{IN}$ = 28 Volts | | | | |
| No Load | 1 | $I_{OUT}$ = 0 | | | 80 | |
| | 2, 3 | | | | 100 | |
| Inhibit 1 | 1, 2, 3 | Pin 4 Shorted to Pin 2 | | | 5.0 | mA |
| Inhibit 2 | | Pin 12 Shorted to Pin 8 | | | | |
| AFL2805D | 1, 2, 3 | | | | 50 | |
| AFL2812D, 15D | 1, 2, 3 | | | | 30 | |
| **INPUT RIPPLE CURRENT** | | $V_{IN}$ = 28 Volts, 100% Load | | | | |
| AFL2805D | 1, 2, 3 | | | | 60 | |
| AFL2812D | 1, 2, 3 | | | | 60 | $mA_{pp}$ |
| AFL2815D | 1, 2, 3 | | | | 60 | |
| **CURRENT LIMIT POINT** | | $V_{OUT}$ = 90% $V_{NOM}$ , Equal current on | | | | |
| **Expressed as a percentage of Full Rated Load** | 1 | positive and negative outputs. Note 5 | 115 | | 125 | |
| | 2 | | 105 | | 115 | % |
| | 3 | | 125 | | 140 | |
| **LOAD FAULT POWER DISSIPATION** | | $V_{IN}$ = 28 Volts | | | | |
| Overload or Short Circuit | 1, 2, 3 | | | | 33 | W |
| **EFFICIENCY** | | $V_{IN}$ = 28 Volts, 100% Load | | | | |
| AFL2805D | 1, 2, 3 | | 78 | 81 | | |
| AFL2812D | 1, 2, 3 | | 82 | 84 | | % |
| AFL2815D | 1, 2, 3 | | 81 | 85 | | |
| **ENABLE INPUTS** (Inhibit Function) | | | | | | |
| Converter Off | 1, 2, 3 | Logical Low on Pin 4 or Pin 12 | -0.5 | | 0.8 | V |
| Sink Current | | Note 1 | | | 100 | µA |
| Converter On | 1, 2, 3 | Logical High on Pin 4 and Pin 12 - Note 9 | 2.0 | | 50 | V |
| Sink Current | | Note 1 | | | 100 | µA |
| **SWITCHING FREQUENCY** | 1, 2, 3 | | 500 | 550 | 600 | KHz |
| **SYNCHRONIZATION INPUT** | | | | | | |
| Frequency Range | 1, 2, 3 | | 500 | | 700 | KHz |
| Pulse Amplitude, Hi | 1, 2, 3 | | 2.0 | | 10 | V |
| Pulse Amplitude, Lo | 1, 2, 3 | | -0.5 | | 0.8 | V |
| Pulse Rise Time | | Note 1 | | | 100 | ns |
| Pulse Duty Cycle | | Note 1 | 20 | | 80 | % |
| **ISOLATION** | 1 | Input to Output or Any Pin to Case (except Pin 3). Test @ 500VDC | 100 | | | MΩ |
| **DEVICE WEIGHT** | | Slight Variations with Case Style | | 85 | | g |
| **MTBF** | | MIL-HDBK-217F, AIF @ $T_C$ = 70°C | 300 | | | KHrs |

For Notes to Specifications, refer to page 4

**Dynamic Characteristics** -55°C ≤ $T_{CASE}$ ≤ +125°C, $V_{IN}$=28V unless otherwise specified.

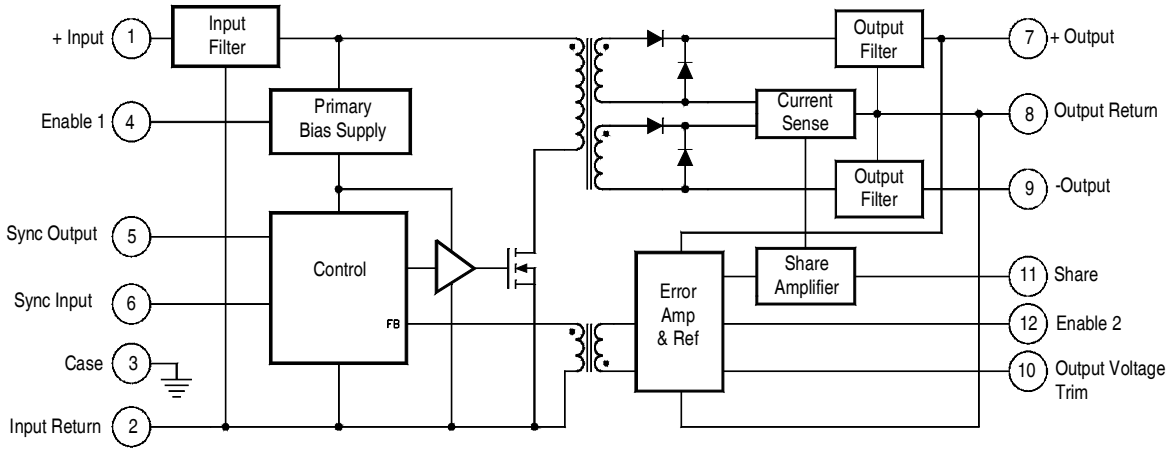
| Parameter | | Group A Subgroups | Test Conditions | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|---|
| **LOAD TRANSIENT RESPONSE** | | | Note 2, 8 | | | | |
| AFL2805D Either Output | Amplitude | 4, 5, 6 | Load Step 50% ⇔ 100% | -450 | | 450 | mV |
| | Recovery | 4, 5, 6 | | | | 200 | µs |
| | Amplitude | 4, 5, 6 | Load Step 10% ⇔ 50% | -450 | | 450 | mV |
| | Recovery | 4, 5, 6 | 10% ⇒ 50% | | | 200 | µs |
| | | | 50% ⇒ 10% | | | 400 | µs |
| AFL2812D Either Output | Amplitude | 4, 5, 6 | Load Step 50% ⇔ 100% | -750 | | 750 | mV |
| | Recovery | 4, 5, 6 | | | | 200 | µs |
| | Amplitude | 4, 5, 6 | Load Step 10% ⇔ 50% | -750 | | 750 | mV |
| | Recovery | 4, 5, 6 | 10% ⇒ 50% | | | 200 | µs |
| | | | 50% ⇒ 10% | | | 400 | µs |
| AFL2815D Either Output | Amplitude | 4, 5, 6 | Load Step 50% ⇔ 100% | -750 | | 750 | mV |
| | Recovery | 4, 5, 6 | | | | 200 | µs |
| | Amplitude | 4, 5, 6 | Load Step 10% ⇔ 50% | -750 | | 750 | mV |
| | Recovery | 4, 5, 6 | 10% ⇒ 50% | | | 200 | µs |
| | | | 50% ⇒ 10% | | | 400 | µs |
| **LINE TRANSIENT RESPONSE** | | | Note 1, 2, 3 | | | | |
| | Amplitude | | $V_{IN}$ Step = 16 ⇔ 40 Volts | -500 | | 500 | mV |
| | Recovery | | | | | 500 | µs |
| **TURN-ON CHARACTERISTICS** | | | $V_{IN}$ = 16, 28, 40 Volts. Note 4 | | | | |
| | Overshoot | 4, 5, 6 | Enable 1, 2 on. (Pins 4, 12 high or | | | 250 | mV |
| | Delay | 4, 5, 6 | open) | 0 | 4.0 | 10 | ms |
| **LOAD FAULT RECOVERY** | | | Same as Turn On Characteristics. | | | | |
| **LINE REJECTION** | | | MIL-STD-461D, CS101, 30Hz to 50KHz Note 1 | 40 | 50 | | dB |

Notes to Specifications:

1. Parameters not 100% tested but are guaranteed to the limits specified in the table.
2. Recovery time is measured from the initiation of the transient to where $V_{out}$ has returned to within ±1.0% of $V_{out}$ at 50% load.
3. Line transient transition time ≥ 100µs.
4. Turn-on delay is measured with an input voltage rise time of between 100V and 500V per millisecond.
5. Current limit point is that condition of excess load causing output voltage to drop to 90% of nominal.
6. Parameter verified as part of another test.
7. All electrical tests are performed with the remote sense leads connected to the output leads at the load.
8. Load transient transition time ≥ 10µs.
9. Enable inputs internally pulled high. Nominal open circuit voltage ≈ 4.0VDC.
10. Load current split equally between +$V_{out}$ and -$V_{out}$.
11. Output load must be distributed so that a minimum of 20% of the total output power is being provided by one of the outputs.
12. Cross regulation measured with load on tested output at 20% of maximum load while changing the load on other output from 20% to 80%.

## Block Diagram

Figure I. Dual Output




## Circuit Operation and Application Information

The AFL series of converters employ a forward switched mode converter topology. (refer to the block diagram in Figure I.) Operation of the device is initiated when a DC voltage whose magnitude is within the specified input voltage limits is applied between pins 1 and 2. If pin 4 is enabled (at a logical 1 or open) the primary bias supply will begin generating a regulated housekeeping voltage bringing the circuitry on the primary side of the converter to life. A power MOSFET is used to chop the DC input voltage into a high frequency square wave, applying this chopped voltage to the power transformer at the nominal converter switching frequency. By maintaining a DC voltage within specified operating range at the input, continuous generation of the bias voltage is assured.

The switched voltage impressed on the secondary output transformer windings is rectified and filtered to provide the positive and negative converter output voltages. An error amplifier on the secondary side compares the positive output voltage to a precision reference and generates an error signal proportional to the difference. This error signal is magnetically coupled through the feedback transformer into the control section of the converter varying the pulse width of the square wave signal driving the MOSFETs, narrowing the pulse width if the output voltage is too high and widening it if it is too low. These pulse width variations provide the necessary corrections to regulate the magnitude of output voltage within its' specified limits.

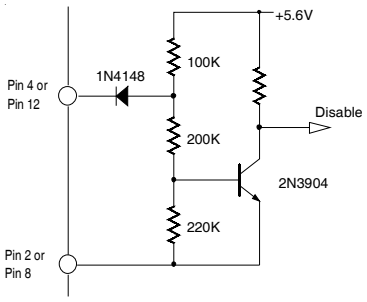
Because the primary portion of the circuit is coupled to the secondary side with magnetic elements, full isolation from input to output is maintained.

Although incorporating several sophisticated and useful ancilliary features, basic operation of the AFL28XXD series series can be initiated by simply applying an input voltage to pins 1 and 2 and connecting the appropriate loads between pins 7, 8, and 9. As is the case with any high power density converter, operation should not be initiated before secure attachment to an appropriate heat dissipator. (See **Thermal Considerations,** page 7) Additional application information is provided in the paragraphs following.

### Inhibiting Converter Output (Enable)

As an alternative to application and removal of the DC voltage to the input, the user can control the converter output by providing TTL compatible, positive logic signals to either of two enable pins (pin 4 or 12). The distinction between these two signal ports is that enable 1 (pin 4) is referenced to the input return (pin 2) while enable 2 (pin 12) is referenced to the output return (pin 8). Thus, the user has access to an inhibit function on either side of the isolation barrier. Each port is internally pulled "high" so that when not used, an open connection on both enable pins permits normal converter operation. When their use is desired, a logical "low" on either port will shut the converter down.

Figure II. Enable Input Equivalent Circuit



Internally, these ports differ slightly in their function. In use, a low on Enable 1 completely shuts down all circuits in the converter, while a low on Enable 2 shuts down the secondary side while altering the controller duty cycle to near zero. Externally, the use of either port is transparent to the user save for minor differences in idle current. (See specification table).

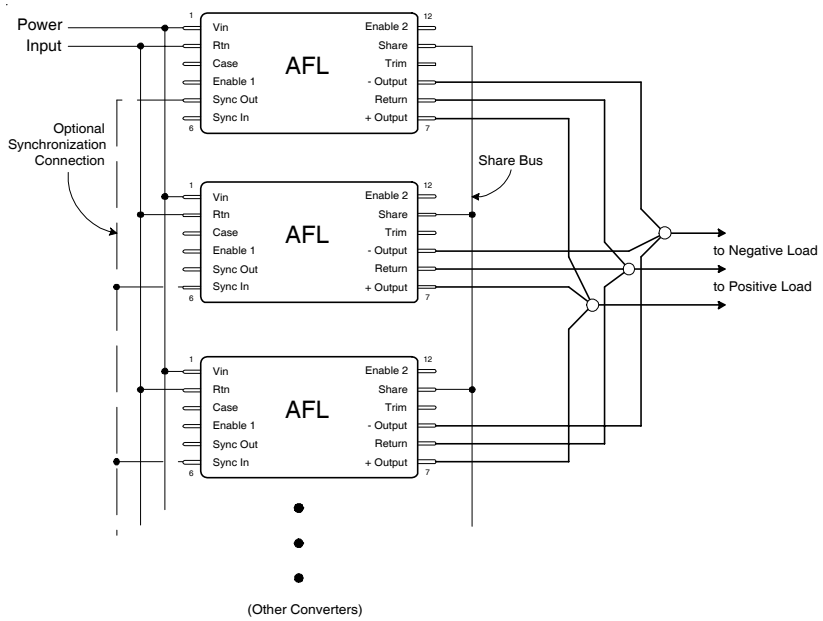
## Synchronization of Multiple Converters

When operating multiple converters, system requirements often dictate operation of the converters at a common frequency. To accommodate this requirement, the AFL series converters provide both a synchronization input and output.

The sync input port permits synchronization of an AFL connverter to any compatible external frequency source operating between 500KHz and 700KHz. This input signal should be referenced to the input return and have a 10% to 90% duty cycle. Compatibility requires transition times less than 100ns, maximum low level of +0.8V and a minimumigh level of +2.0V. The sync output of another converter which has been designated as the master oscillator provides a convenient frequency source for this mode of operation. When external synchronization is not indicted, the sync in pin should be left open (unconnected) thereby permitting the converter to operate at its' own internally set frequency.

The sync output signal is a continuous pulse train set at 550 ± 50KHz, with a duty cycle of 15 ± 5%. This signal is referenced to the input return and has been tailored to be compatible with the AFL sync input port. Transition times are less than 100ns and the low level output impedance is less than 50Ω. This signal is active when the DC input voltage is within the specified operating range and the converter is not inhibited. This synch output has adequate drive reserve to synchronize at least five additional converters. A typical synchronization connection option is illustrated in Figure III.

Figure III. Preferred Connection for Parallel Operation




## Parallel Operation-Current and Stress Sharing

Figure III. illustrates the preferred connection scheme for operation of a set of AFL converters with outputs operating in parallel. Use of this connection permits equal current sharing among the members of a set whose load current exceeds the capacity of an individual AFL. An important feature of the AFL series operating in the parallel mode is that in addition to sharing the current, the stress induced by temperature will also be shared. Thus if one member of a paralleled set is operating at a higher case temperature, the current it provides to the load will be reduced as compensation for the temperature induced stress on that device.

When operating in the shared mode, it is important that symmetry of connection be maintained as an assurance of optimum load sharing performance. Thus, converter outputs should be connected to the load with equal lengths of wire of the same gauge and should be connected to a common physical point, preferably at the load along with the converter output and return leads. All converters in a paralleled set must have their share pins connected together. This arrangement is diagrammatically illustrated in Figure III. showing the output and return pins connected at a star point which is located close as possible to the load.

As a consequence of the topology utilized in the current sharing circuit, the share pin may be used for other functions. In applications requiring only a single converter, the voltage appearing on the share pin may be used as a "total current monitor". The share pin open circuit voltage is nominally +1.00V at no load and increases linearly with increasing total output current to +2.20V at full load. Note that the current we refer to here is the total output current, that is, the sum of the positive and negative outout currents.

## Thermal Considerations

Because of the incorporation of many innovative technological concepts, the AFL series of converters is capable of providing very high output power from a package of very small volume. These magnitudes of power density can only be obtained by combining high circuit efficiency with effective methods of heat removal from the die junctions. This requirement has been effectively addressed inside the device; but when operating at maximum loads, a significant amount of heat will be generated and this heat must be conducted away from the case. To maintain the case temperature at or below the specified maximum of 125°C, this heat must be transferred by conduction to an appropriate heat dissipater held in intimate contact with the converter base-plate.

Since the effectiveness of this heat transfer is dependent on the intimacy of the baseplate/heatsink interface, it is strongly recommended that a high thermal conductivity heat transferring medium is inserted between the baseplate and heatsink. The material most frequently utilized at the factory during all testing and burn-in processes is sold under the trade name of Sil-Pad® 400[1]. This particular product is an insulator but electrically conductive versions are also available. Use of these materials assures maximum surface contact with the heat dissipater thereby compensating for any minor surface variations. While other available types of heat conductive materials and thermal compounds provide similar effectiveness, these alternatives are often less convenient and can be somewhat messy to use.

[1]Sil-Pad is a registered Trade Mark of Bergquist, Minneapolis, MN

A conservative aid to estimating the total heat sink surface area ($A_{HEAT\ SINK}$) required to set the maximum case temperature rise ($\Delta T$) above ambient temperature is given by the following expression:

$$A_{\text{HEAT SINK}} \approx \left\{\frac{\Delta T}{80P^{0.85}}\right\}^{-1.43} - 3.0$$

where

$\Delta T$ = Case temperature rise above ambient

$P$ = Device dissipation in Watts = $P_{OUT}\left\{\frac{1}{Eff} - 1\right\}$

As an example, assume that it is desired to operate an AFL2815D in a still air environment where the ambient temperature is held to a constant +25°C while holding the case temperature at $T_C \leq +85°C$; then case temperature rise is

$$\Delta T = 85 - 25 = 60°C$$

From the Specification Table, the worst case full load efficiency for AFL2815D is 83% at 100W: thus, power dissipation at full load is given by

$$P = 100 \bullet \left\{\frac{1}{.83} - 1\right\} = 100 \bullet (0.205) = 20.5\text{W}$$

and the required heat sink area is

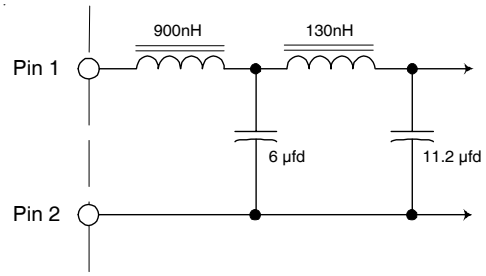
$$A_{\text{HEAT SINK}} = \left\{\frac{60}{80 \bullet 20.5^{0.85}}\right\}^{-1.43} - 3.0 = 56.3\ \text{in}^2$$

Thus, a total heat sink surface area (including fins, if any) of 56 $in^2$ in this example, would limit case rise to 60°C above ambient. A flat aluminum plate, 0.25" thick and of approximate dimension 4" by 7" (28 $in^2$ per side) would suffice for this application in a still air environment. Note that to meet the criteria in this example, both sides of the plate require unrestricted exposure to the +25°C ambient air.

## Input Filter

The AFL28XXD series converters incorporate a two stage LC input filter whose elements dominate the input load impedance characteristic during the turn-on sequence. The input circuit is as shown in Figure IV.

Figure IV. Input Filter Circuit



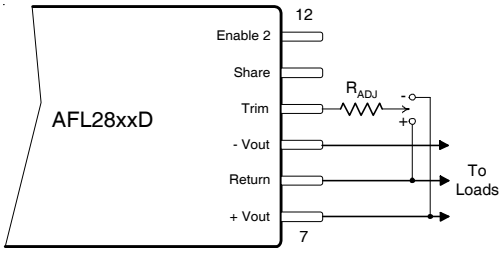

## Undervoltage Lockout

A minimum voltage is required at the input of the converter to initiate operation. This voltage is set to 14V ± 0.5V. To preclude the possibility of noise or other variations at the input falsely initiating and halting converter operation, a hysteresis of approximately 1.0V is incorporated in this circuit. Thus if the input voltage droops to 13V ± 0.5V, the converter will shut down and remain inoperative until the input voltage returns to ≈14V.

## Output Voltage Adjust

By use of the trim pin (10), the magnitude of output voltages can be adjusted over a limited range in either a positive or negative direction. Connecting a resistor between the trim pin and either the output return or the positive output will raise or lower the magnitude of output voltages. The span of output voltage adjustment is restricted to the limits shown in Table I.

Figure V. Connection for $V_{OUT}$ Adjustment




Connect $R_{adj}$ to + to increase, - to decrease

Table 1. Output Voltage Trim Values and Limits

| AFL2805D | | AFL2812D | | AFL2815D | |
|---|---|---|---|---|---|
| $V_{out}$ | $R_{adj}$ | $V_{out}$ | $R_{adj}$ | $V_{out}$ | $R_{adj}$ |
| 5.5 | 0 | 12.5 | 0 | 15.5 | 0 |
| 5.4 | 12.5K | 12.4 | 47.5K | 15.4 | 62.5K |
| 5.3 | 33.3K | 12.3 | 127K | 15.3 | 167K |
| 5.2 | 75K | 12.2 | 285K | 15.2 | 375K |
| 5.1 | 200K | 12.1 | 760K | 15.1 | 1.0M |
| 5.0 | ∞ | 12.0 | ∞ | 15.0 | ∞ |
| 4.9 | 190K | 11.7 | 975K | 14.6 | 1.2M |
| 4.8 | 65K | 11.3 | 288K | 14.0 | 325K |
| 4.7 | 23K | 10.8 | 72.9K | 13.5 | 117K |
| 4.6 | 2.5K | 10.6 | 29.9K | 13.0 | 12.5K |
| 4.583 | 0 | 10.417 | 0 | 12.917 | 0 |

Note that the nominal magnitude of output voltage resides in the middle of the table and the corresponding resistor value is set to ∞. To set the magnitude greater than nominal, the adjust resistor is connected to output return. To set the magnitude less than nominal, the adjust resistor is connected to the positive output. (Refer to Figure V.)

For output voltage settings that are within the limits, but between those listed in Table I, it is suggested that the resistor values be determined empirically by selection or by use of a variable resistor. The value thus determined can then be replaced with a good quality fixed resistor for permanent installation.

When use of this adjust feature is elected, the user should be aware that the temperature performance of the converter output voltage will be affected by the temperature performance of the resistor selected as the adjustment element and therefore, is advised to employ resistors with a tight temperature coefficient of resistance.

## General Application Information

The AFL28XXD series of converters are capable of providing large transient currents to user loads on demand. Because the nominal input voltage range in this series is relatively low, the resulting input current demands will be correspondingly large. It is important therefore, that the line impedance be kept very low to prevent steady state and transient input currents from degrading the supply voltage between the voltage source and the converter input. In applications requiring high static currents and large transients, it is recommended that the input leads be made of adequate size to minimize resistive losses, and that a good quality capacitor of approximately 100µfd be connected directly across the input terminals to assure an adequately low impedance at the input terminals. Table I relates nominal resistance values and selected wire sizes.

Table 2. Nominal Resistance of Cu Wire

| Wire Size, AWG | Resistance per ft |
|---|---|
| 24 Ga | 25.7 mΩ |
| 22 Ga | 16.2 mΩ |
| 20 Ga | 10.1 mΩ |
| 18 Ga | 6.4 mΩ |
| 16 Ga | 4.0 mΩ |
| 14 Ga | 2.5 mΩ |
| 12 Ga | 1.6 mΩ |

As an example of the effects of parasitic resistance, consider an AFL2815D operating at full power of 100W. From the specification sheet, this device has a minimum efficiency of 83% which represents an input power of more than 120W. If we consider the case where line voltage is at its' minimum of 16V, the steady state input current necessary for this example will be slightly greater than 7.5A. If this device were connected to a voltage source with 10 feet of 20 gauge wire, the round trip (input and return) would result in 0.2Ω of resistance and 1.5V of drop from the source to the converter. To assure 16V at the input, a source closer to 18V would be required. In applications using the paralleling option, this drop will be multiplied by the number of paralleled devices. By choosing 14 or 16 gauge wire in this example, the parasitic resistance and resulting voltage drop will be reduced to 25% or 31% of that with 20 gauge wire.

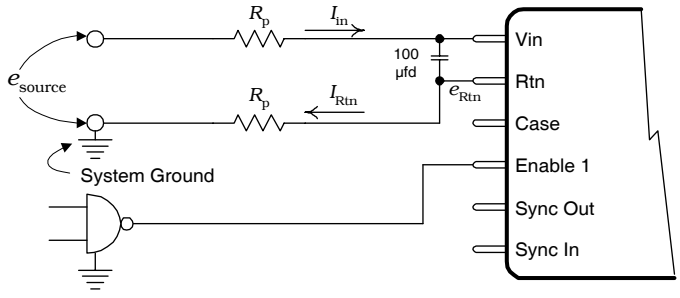
Another potential problem resulting from parasitically induced voltage drop on the input lines is with regard to the operation of the enable 1 port. The minimum and maximum operating levels required to operate this port are specified with respect to the input common return line at the converter. If a logic signal is generated with respect to a 'common' that is distant from the converter, the effects of the voltage drop over the return line must be considered when establishing the worst case TTL switching levels. These drops will effectively impart a shift to the logic levels. In Figure VI, it can be seen that referred to system ground, the voltage on the input return pin is given by

$$e_{Rtn} = I_{Rtn} \bullet R_P$$

Therefore, the logic signal level generated in the system must be capable of a TTL logic high plus sufficient additional amplitude to overcome $e_{Rtn}$. When the converter is inhibited, $I_{Rtn}$ diminishes to near zero and $e_{Rtn}$ will then be at system ground.

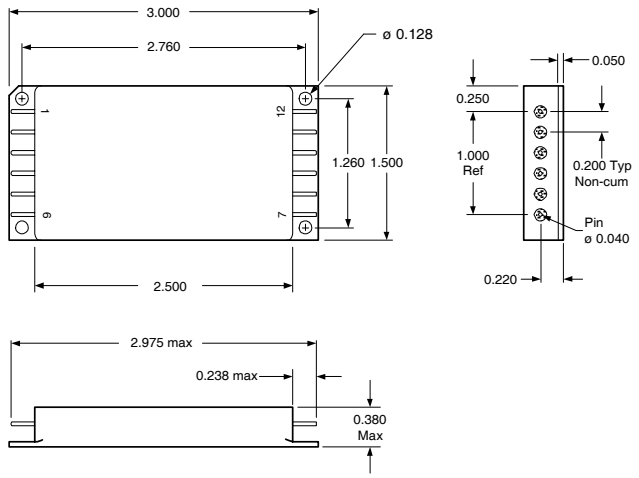
Incorporation of a 100µfd capacitor at the input terminals is recommended as compensation for the dynamic effects of the parasitic resistance of the input cable reacting with the complex impedance of the converter input, and to provide an energy reservoir for transient input current requirements.

Figure VI. Problems of Parasitic Resistance in input Leads



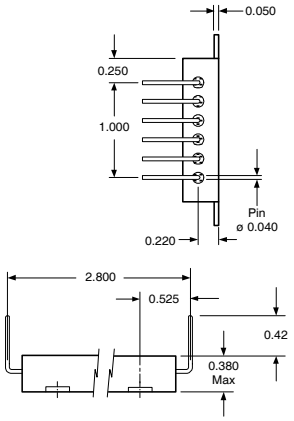
## Mechanical Outlines

### Case X

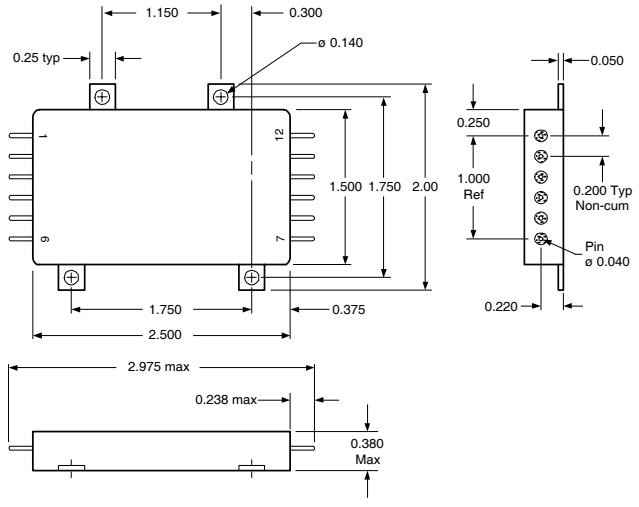



### Case W

Pin Variation of Case Y

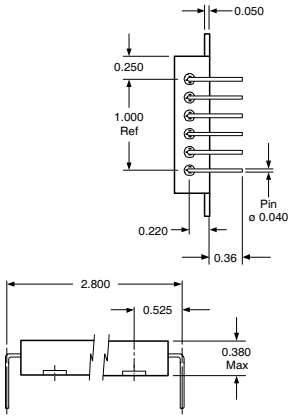



### Case Y




### Case Z

Pin Variation of Case Y




Tolerances, unless otherwise specified: .XX = ±0.010
.XXX = ±0.005

**BERYLLIA WARNING**: These converters are hermetically sealed; however they contain BeO substrates and should not be ground or subjected to any other operations including exposure to acids, which may produce Beryllium dust or fumes containing Beryllium

**Pin Designation**

| Pin # | Designation |
|---|---|
| 1 | + Input |
| 2 | Input Return |
| 3 | Case Ground |
| 4 | Enable 1 |
| 5 | Sync Output |
| 6 | Sync Input |
| 7 | + Output |
| 8 | Output Return |
| 9 | - Output |
| 10 | Output Voltage Trim |
| 11 | Share |
| 12 | Enable 2 |

**Standard Microcircuit Drawing Equivalence Table**

| Standard Microcircuit Drawing Number | IR Standard Part Number |
|---|---|
| 5962-95795 | AFL2805D |
| 5962-95796 | AFL2812D |
| 5962-94724 | AFL2815D |

## Device Screening

| Requirement | MIL-STD-883 Method | No Suffix | ES ② | HB | CH |
|---|---|---|---|---|---|
| Temperature Range | — | -20°C to +85°C | -55°C to +125°C ③ | -55°C to +125°C | -55°C to +125°C |
| Element Evaluation | MIL-PRF-38534 | N/A | N/A | N/A | Class H |
| Non-Destructive Bond Pull | 2023 | N/A | N/A | N/A | N/A |
| Internal Visual | 2017 | ① | Yes | Yes | Yes |
| Temperature Cycle | 1010 | N/A | Cond B | Cond C | Cond C |
| Constant Acceleration | 2001, Y1 Axis | N/A | 500 Gs | 3000 Gs | 3000 Gs |
| PIND | 2020 | N/A | N/A | N/A | N/A |
| Burn-In | 1015 | N/A | 48 hrs@hi temp | 160 hrs@125°C | 160 hrs@125°C |
| Final Electrical ( Group A ) | MIL-PRF-38534 & Specification | 25°C | 25°C ② | -55°C, +25°C, +125°C | -55°C, +25°C, +125°C |
| PDA | MIL-PRF-38534 | N/A | N/A | N/A | 10% |
| Seal, Fine and Gross | 1014 | Cond A | Cond A, C | Cond A, C | Cond A, C |
| Radiographic | 2012 | N/A | N/A | N/A | N/A |
| External Visual | 2009 | ① | Yes | Yes | Yes |

Notes:
① Best commercial practice
② Sample tests at low and high temperatures
③ -55°C to +105°C for AHE, ATO, ATW

## Part Numbering

AFL 28 05 D X /CH

**Model**

**Input Voltage**
28 = 28V
50 = 50V
120 = 120V
270 = 270V

**Output Voltage**
05 = ±5V
12 = ±12V
15 = ±15V

**Output**
D = Dual

**Case Style**
W, X, Y, Z

**Screening Level**
(Please refer to Screening Table)
No suffix, ES, HB, CH

International
IOR Rectifier

**WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
**IR SANTA CLARA:** 2270 Martin Av., Santa Clara, California 95050, Tel: (408) 727-0500
Visit us at www.irf.com for sales contact information.