

N-channel 950 V, 2 Ω typ., 3.5 A Zener-protected SuperMESH™ 5 Power MOSFETs in DPAK, TO-220FP and TO-220 packages

Datasheet – production data

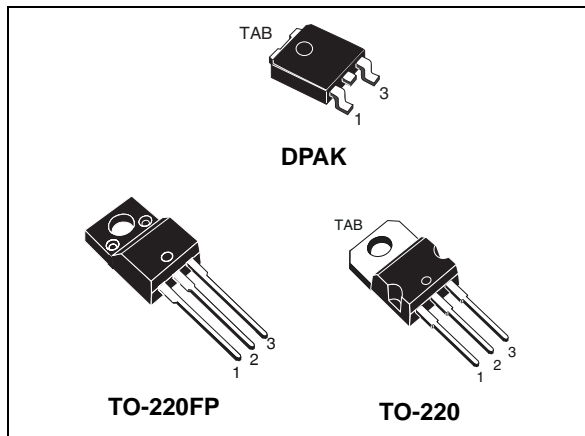
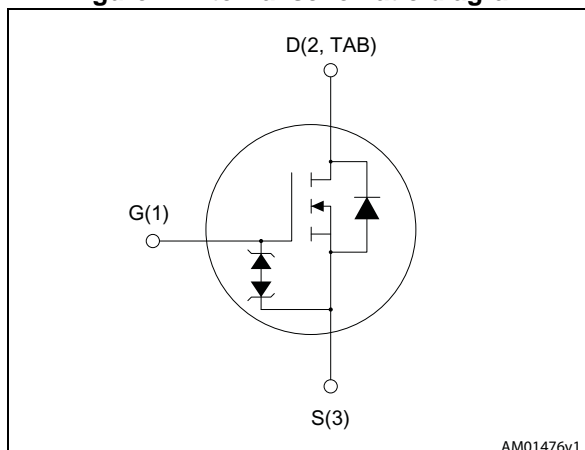


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STD5N95K5	950 V	2.5 Ω	3.5 A	70 W
STF5N95K5				25 W
STP5N95K5				70 W

- TO-220 worldwide best R_{DS(on)}
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These N-channel Zener-protected Power MOSFETs are designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD5N95K5	5N95K5	DPAK	Tape and reel
STF5N95K5		TO-220FP	Tube
STP5N95K5		TO-220	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220	TO-220FP	
V_{GS}	Gate- source voltage	30		V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	3.5	3.5 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	2.2	2.2 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	14		A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	70	25	W
I_{AR}	Max current during repetitive or single pulse avalanche	1		A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	70		mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ °C}$)		2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	- 55 to 150		°C

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 3.5\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DSPeak} \leq V_{(BR)DSS}$
4. $V_{SD} \leq 640\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		DPAK, TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.47	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5		°C/W

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	950			V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 950 V, V _{GS} = 0 V _{DS} = 950 V, V _{GS} = 0, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body leakage current	V _{GS} = ± 20 V; V _{DS} = 0			10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 1.5 A		2	2.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0	-	220	-	pF
C _{oss}	Output capacitance		-	17	-	pF
C _{rss}	Reverse transfer capacitance		-	1	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{GS} = 0, V _{DS} = 0 to 760 V	-	30	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	11	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	17	-	Ω
Q _g	Total gate charge	V _{DD} = 760 V, I _D = 3.5 A	-	12.5	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V	-	2	-	nC
Q _{gd}	Gate-drain charge	(see Figure 19)	-	10	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$, $I_D = 1.75\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ <i>(see Figure 18)</i>	-	12	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off-delay time		-	32	-	ns
t_f	Fall time		-	25	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		3.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		14	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3.5\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 3.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ <i>(see Figure 20)</i>	-	330		ns
Q_{rr}	Reverse recovery charge		-	2.2		μC
I_{RRM}	Reverse recovery current		-	13		A
t_{rr}	Reverse recovery time	$I_{SD} = 3.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ <i>(see Figure 20)</i>	-	525		ns
Q_{rr}	Reverse recovery charge		-	3.2		μC
I_{RRM}	Reverse recovery current		-	12		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device’s ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK

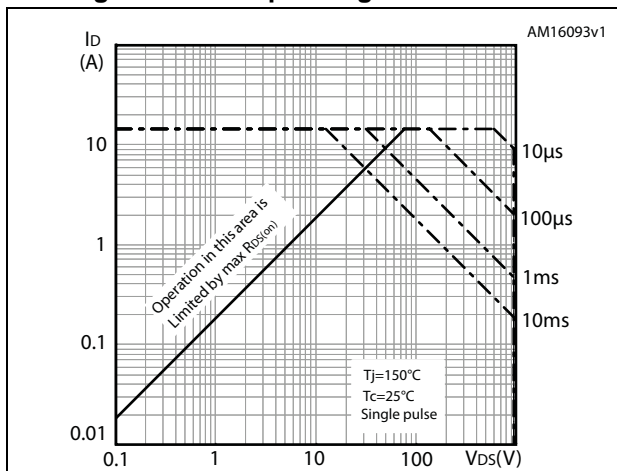


Figure 3. Thermal impedance for DPAK

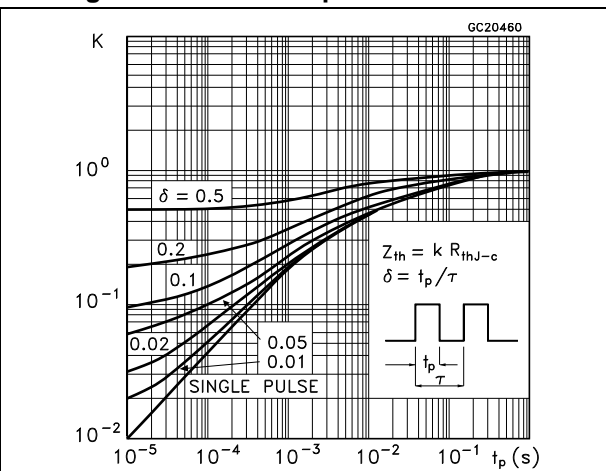


Figure 4. Safe operating area for TO-220FP

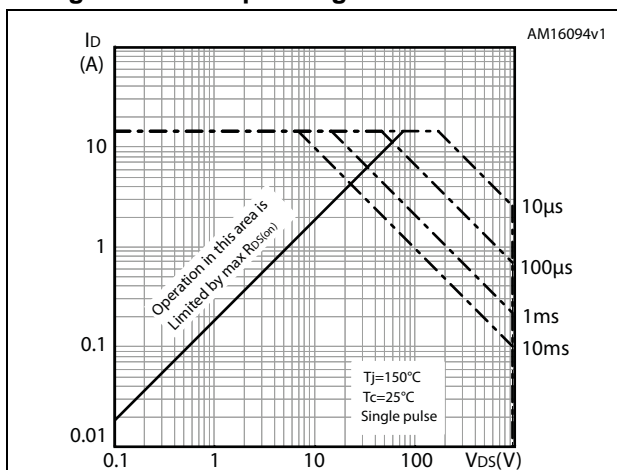


Figure 5. Thermal impedance for TO-220FP

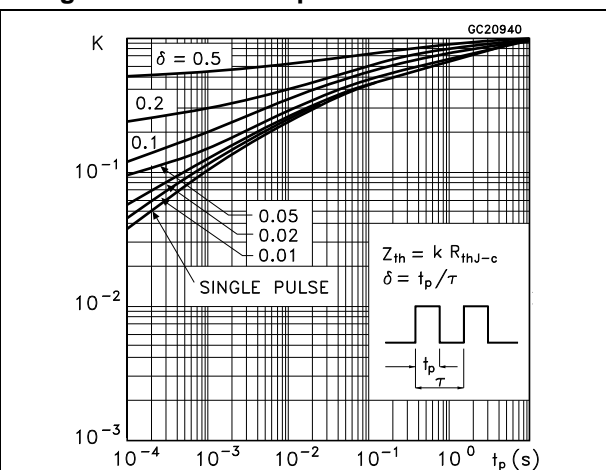


Figure 6. Safe operating area for TO-220

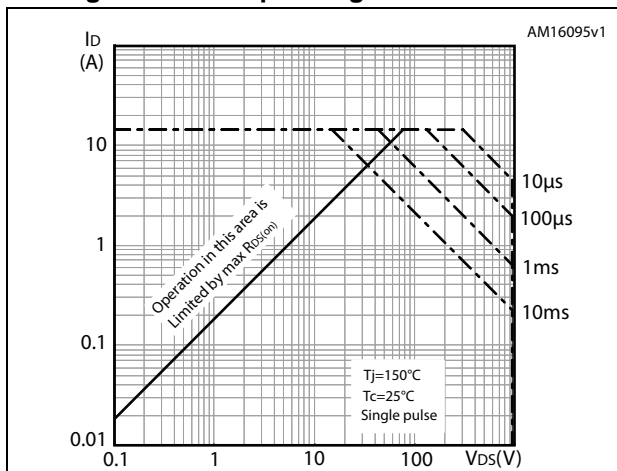


Figure 7. Thermal impedance for TO-220

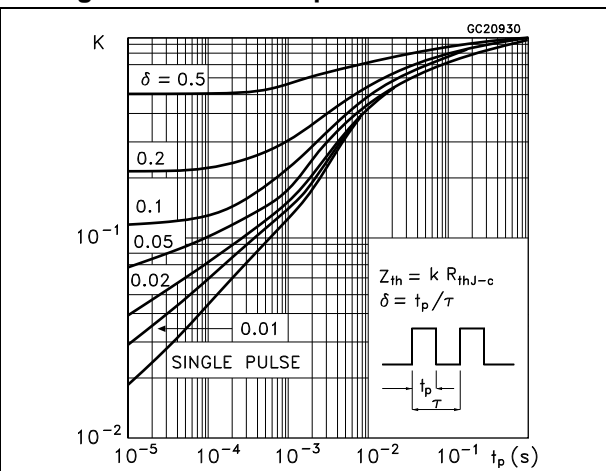


Figure 8. Output characteristics

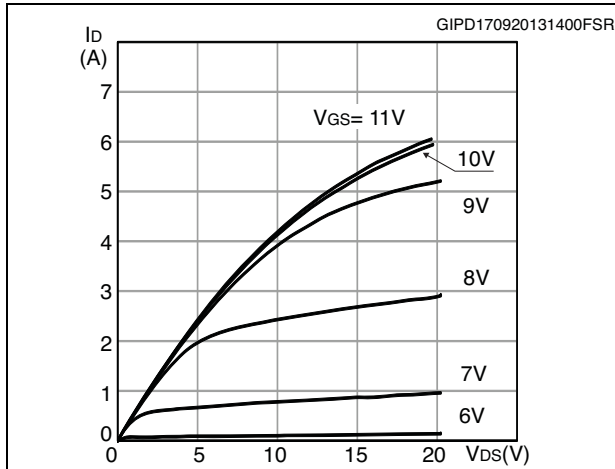


Figure 9. Transfer characteristics

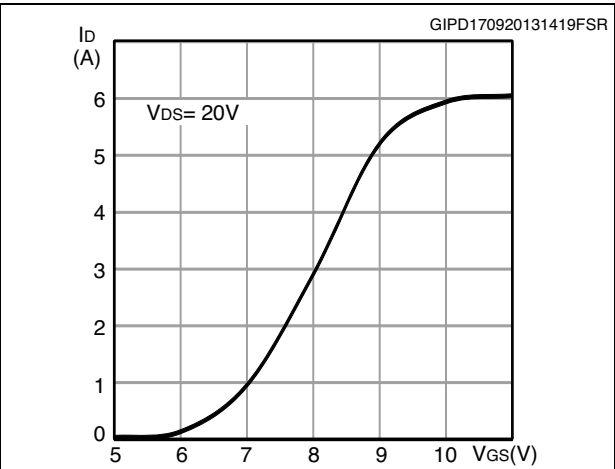


Figure 10. Gate charge vs gate-source voltage

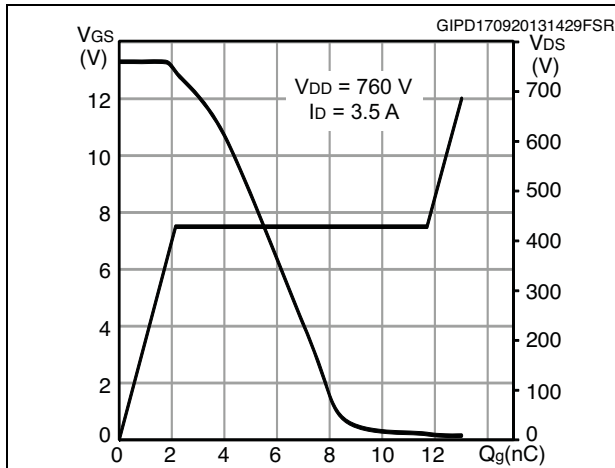


Figure 11. Static drain-source on-resistance

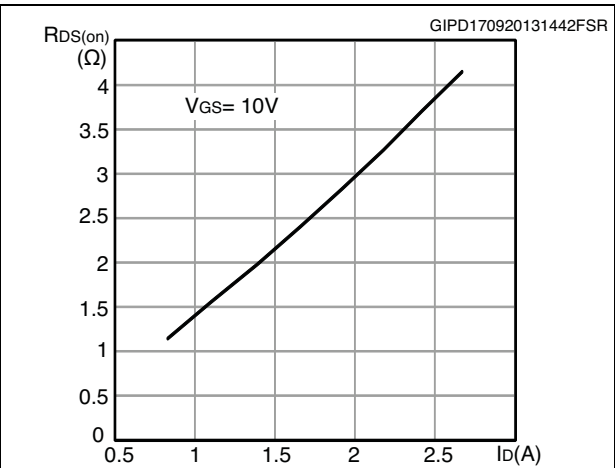


Figure 12. Capacitance variations

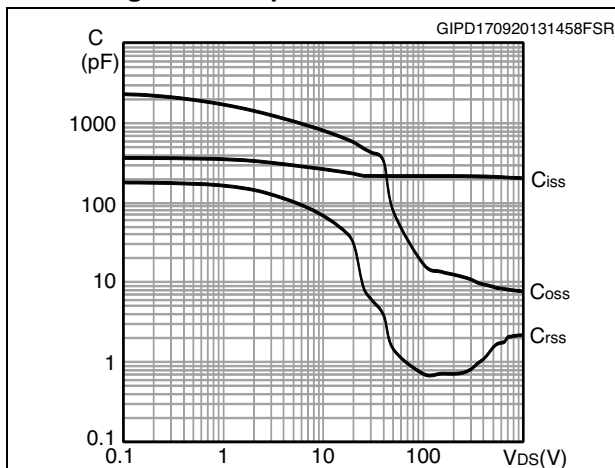


Figure 13. Output capacitance stored energy

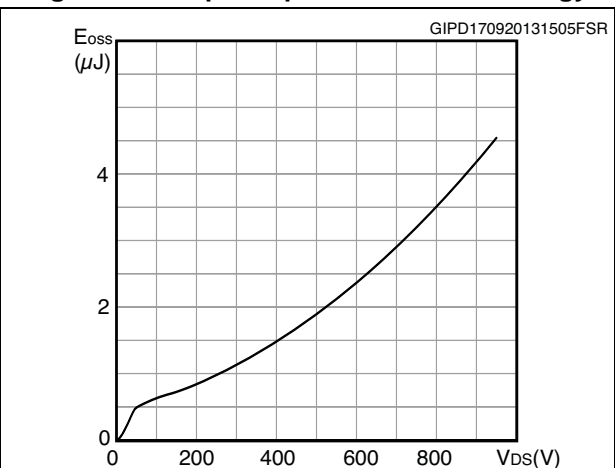


Figure 14. Normalized gate threshold voltage vs temperature

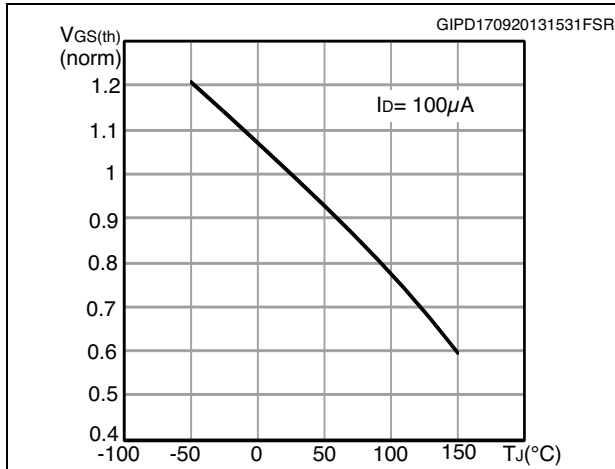


Figure 15. Normalized on-resistance vs temperature

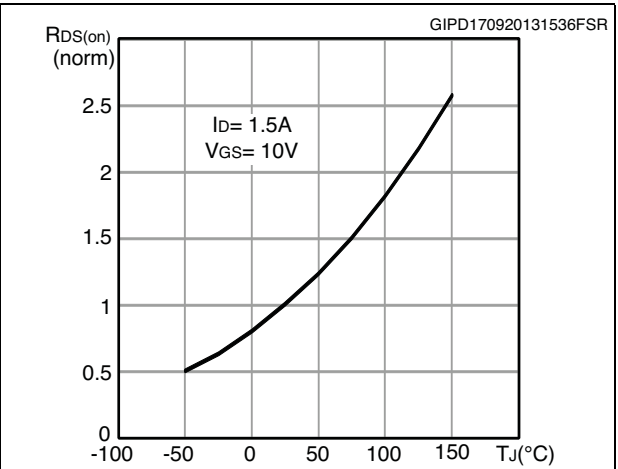


Figure 16. Normalized V_{(BR)DSS} vs temperature

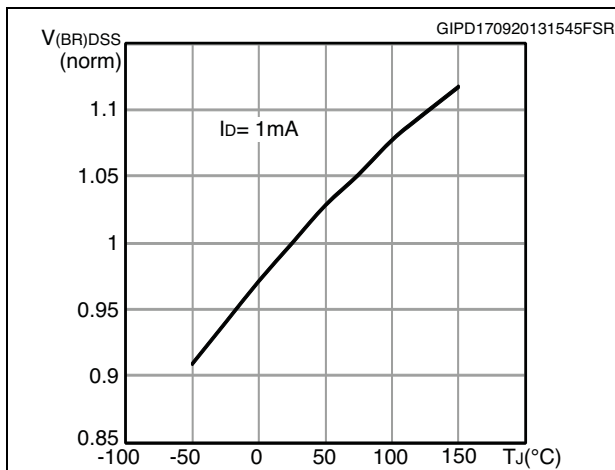
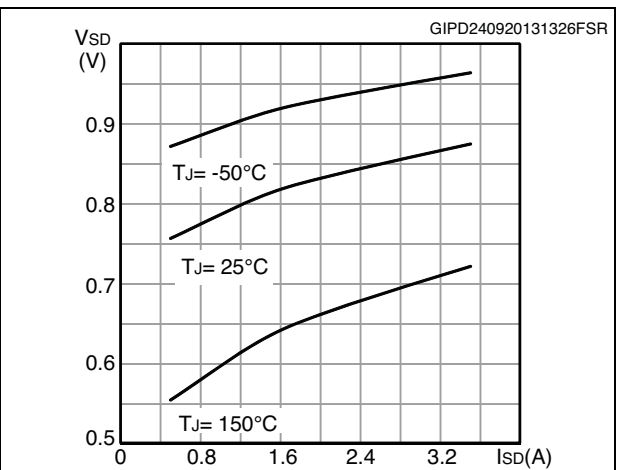


Figure 17. Source-drain diode forward characteristics



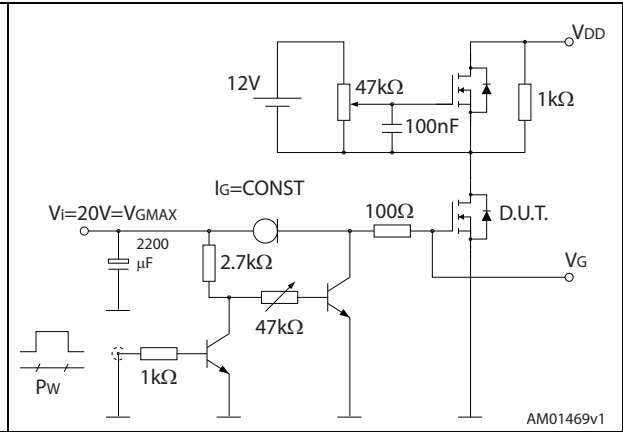
3 Test circuits

Figure 18. Switching times test circuit for resistive load



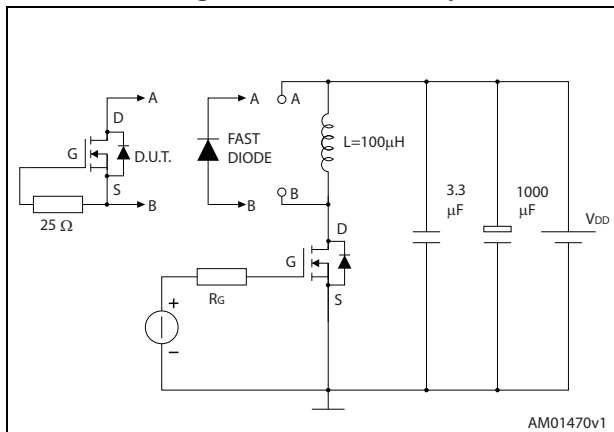
AM01468v1

Figure 19. Gate charge test circuit



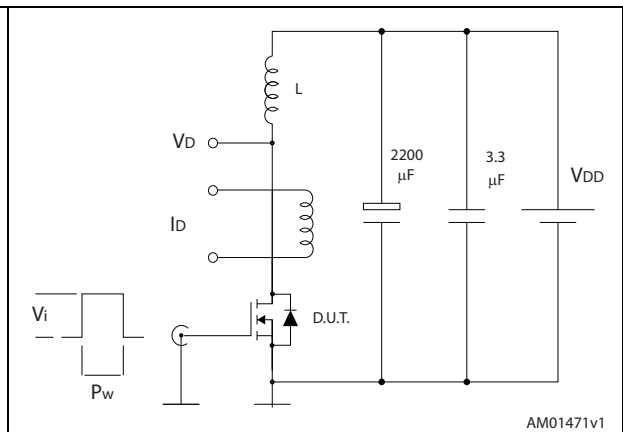
AM01469v1

Figure 20. Test circuit for inductive load switching and diode recovery times



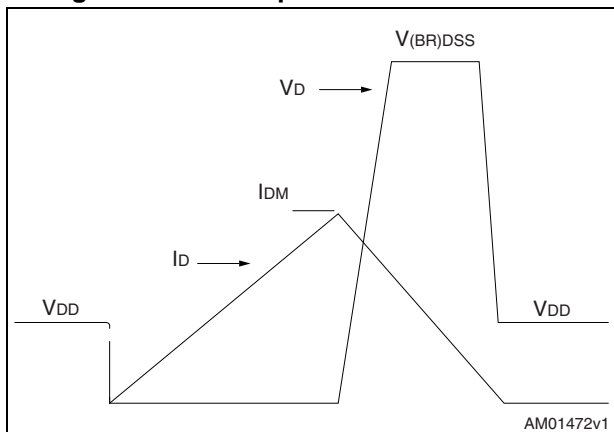
AM01470v1

Figure 21. Unclamped inductive load test circuit



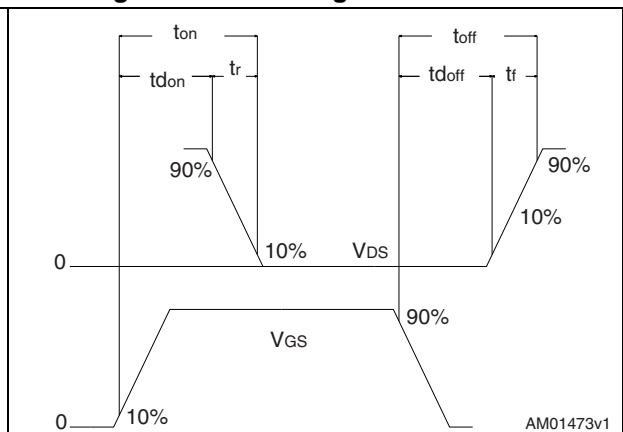
AM01471v1

Figure 22. Unclamped inductive waveform



AM01472v1

Figure 23. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 24. DPAK (TO-252) type A drawing

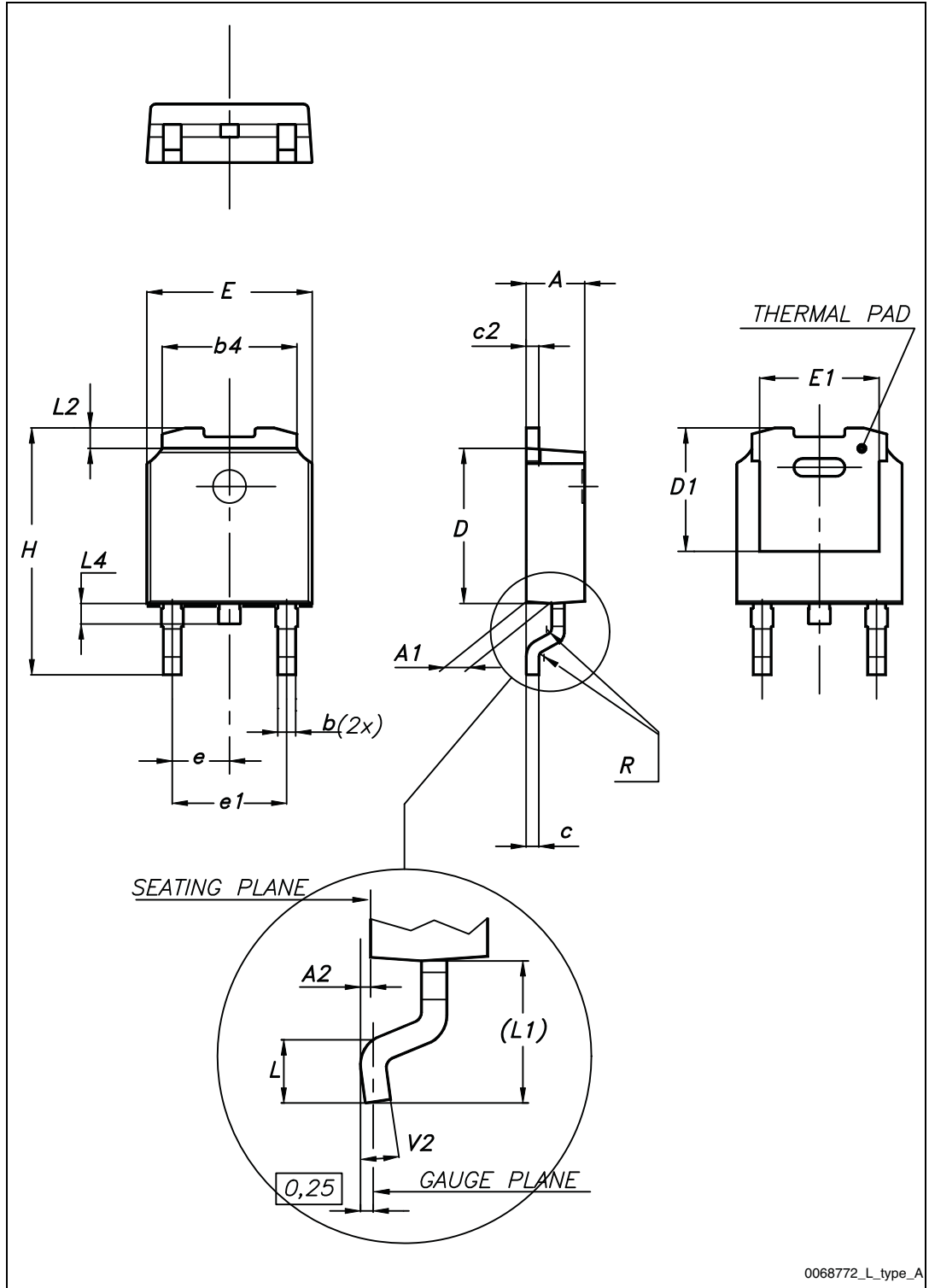
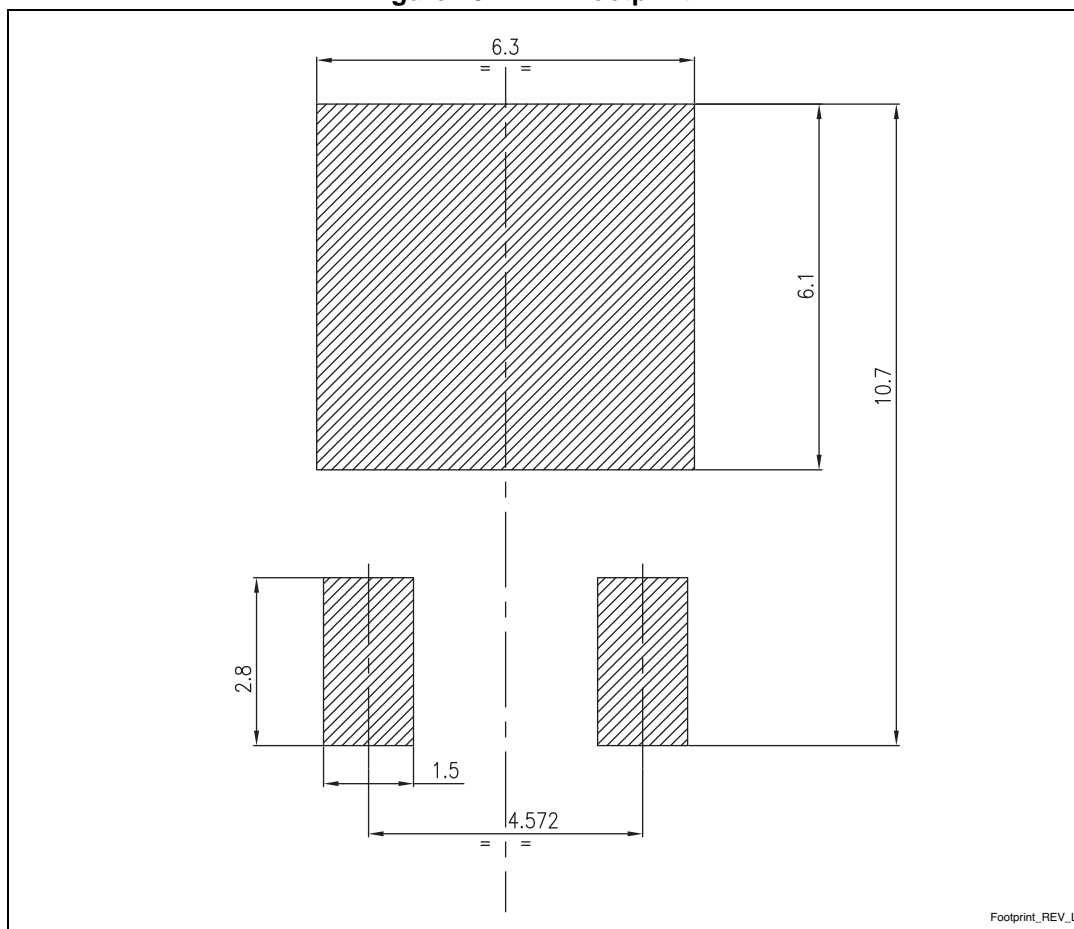


Figure 25. DPAK footprint (a)

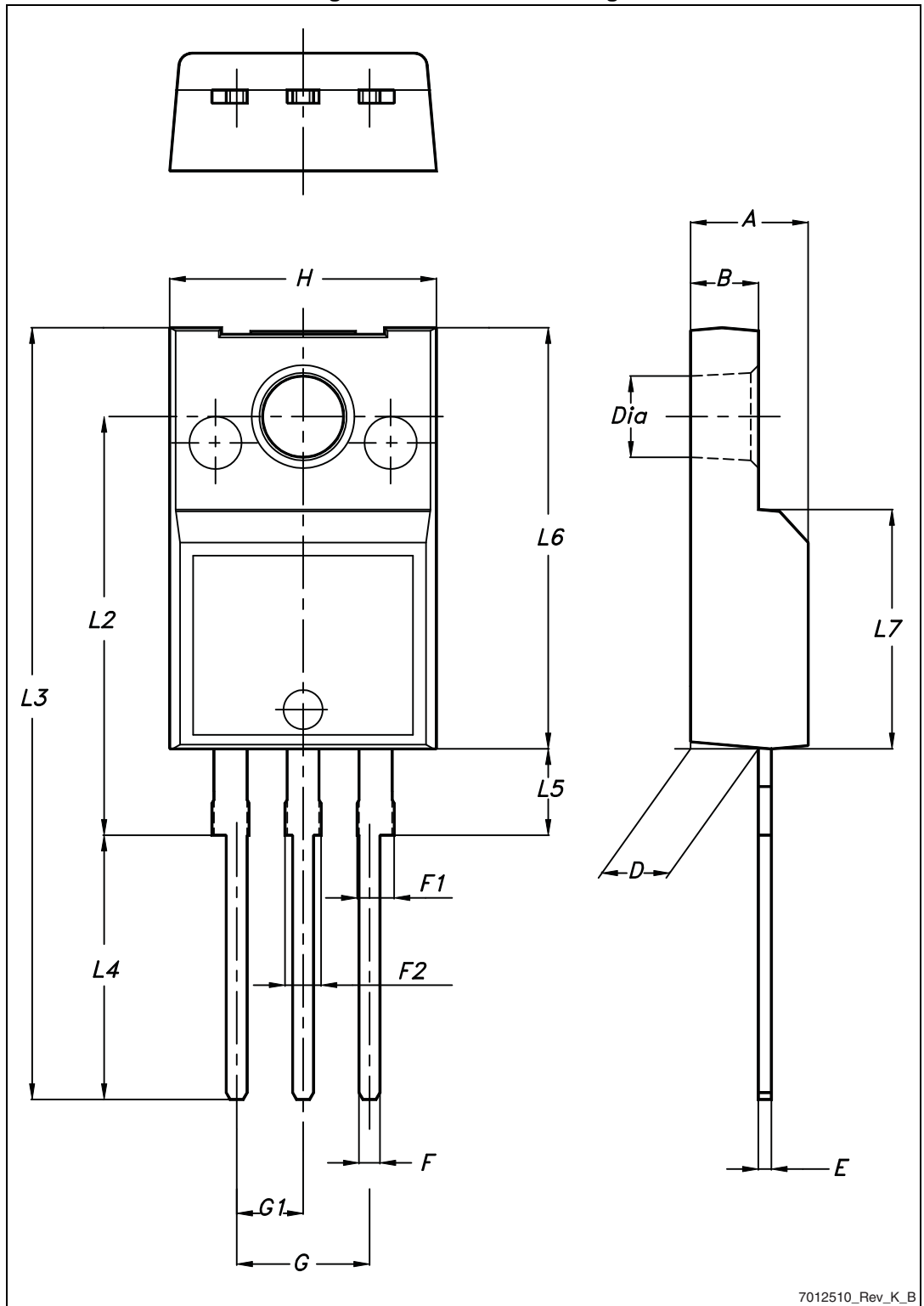


a. All dimensions are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 26. TO-220FP drawing

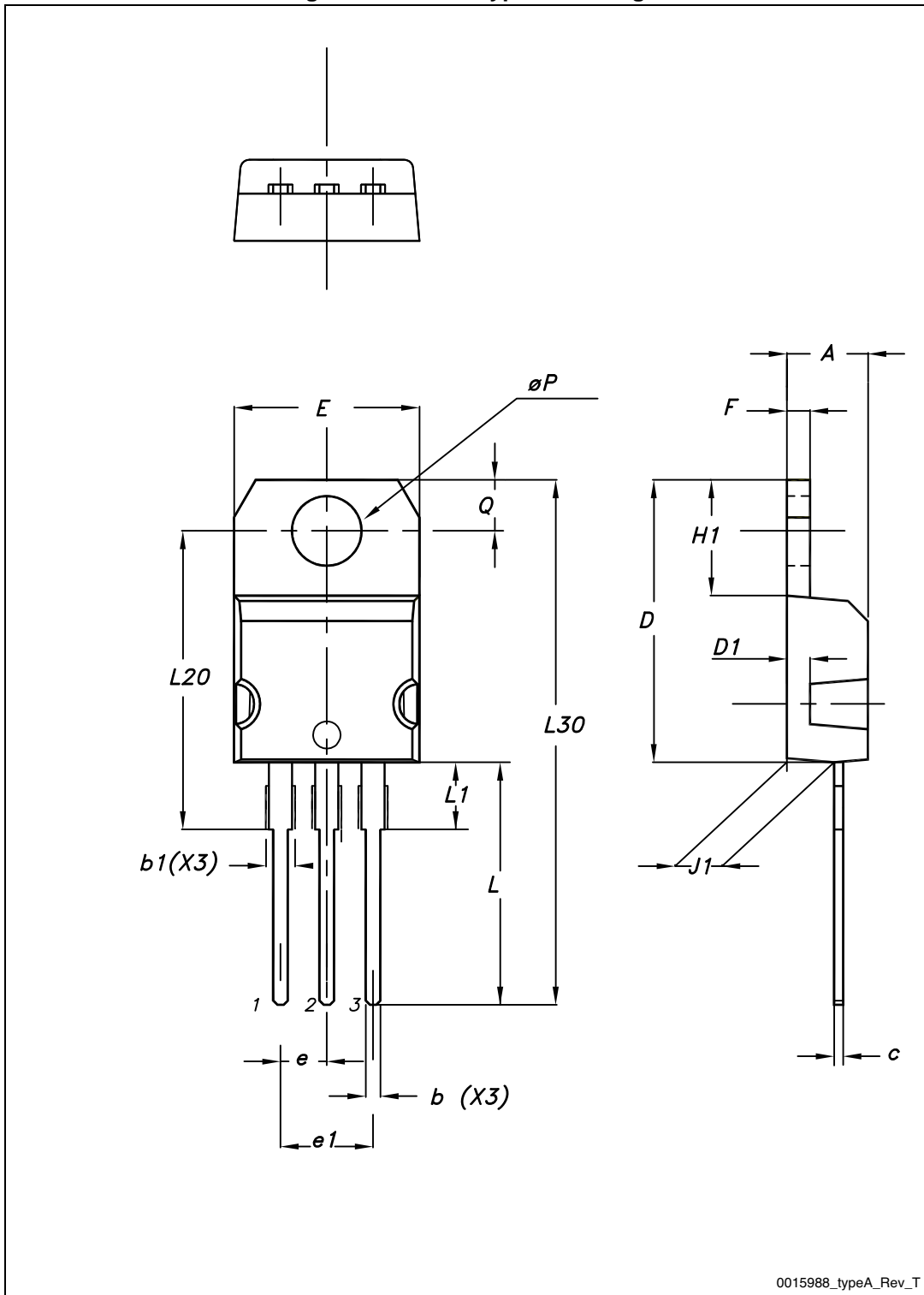


7012510_Rev_K_B

Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing



5 Revision history

Table 12. Document revision history

Date	Revision	Changes
08-May-2013	1	First release.
18-Sep-2013	2	Document status promoted from preliminary to production data. Added Section 2.1: Electrical characteristics (curves) . Updated DPAK mechanical data.
25-Sep-2013	3	Inserted Figure 17: Source-drain diode forward characteristics .

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