BSF035NE2LQ

OptiMOS™ Power-MOSFET

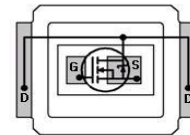
Features

- Optimized for high performance Buck converter
- Low parasitic inductance
- Low profile (<0.7 mm)
- 100% avalanche tested
- 100% R_G Tested
- Double-sided cooling
- Compatible with DirectFET® package SQ footprint and outline [1]
- Qualified according to JEDEC[2] for target applications

Product Summary

V_{DS}	25	V
$R_{DS(on),max}$	3.5	mΩ
I_D	69	A
Q_{oss}	13	nC
Q_g(0V..10V)	19	nC

CanPAK™ S
MG-WDSON-2



Type	Package	Outline	Marking
BSF035NE2LQ	MG-WDSON-2	SQ	04E2

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	69	A
		V_{GS}=10 V, T_C=100 °C	44	
		V_{GS}=10 V, T_A=25 °C, R_{thJA}=45 K/W[3]	22	
Pulsed drain current[4]	$I_{D,pulse}$	T_C=25 °C	276	
Avalanche current, single pulse[5]	I_{AS}	T_C=25 °C	40	
Avalanche energy, single pulse	E_{AS}	I_D=35 A, R_{GS}=25 Ω	50	mJ
Gate source voltage	V_{GS}		±20	V

[1] CanPAK™ uses DirectFET ® technology licensed from International Rectifier Corporation. DirectFET® is a registered trademark of International Rectifier Corporation.

[2] J-STD20 and JESD22

[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[4] See figure 3 for more detailed information

[5] See figure 13 for more detailed information

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Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	28	W
		T_A=25 °C, R_{thJA}=58 K/W	2.2	
Operating and storage temperature	T_j, T_{stg}		-40 … 150	°C
IEC climatic category; DIN IEC 68-1				

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}	bottom	-	1.0	-	K/W
		top	-	-	4.5	
Device on PCB	R_{thJA}	6 cm^2 cooling area[5)]	-	-	58	

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1.2	-	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=25 V, V_{GS}=0 V, T_j=25 °C	-	0.1	10	µA
		V_{DS}=25 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=30 A	-	3.7	4.6	mΩ
		V_{GS}=10 V, I_D=30 A	-	2.9	3.5	
Gate resistance	R_G		0.3	0.6	1.2	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A	55	110	-	S

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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz	-	1400	1862	pF
Output capacitance	C_{oss}		-	630	838	
Reverse transfer capacitance	C_{rss}		-	59	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω	-	1.8	-	ns
Rise time	t_r		-	3.2	-	
Turn-off delay time	$t_{d(off)}$		-	16	-	
Fall time	t_f		-	2.2	-	
Gate Charge Characteristics[6]						
Gate to source charge	Q_{gs}	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	3.1	4.1	nC
Gate charge at threshold	$Q_{g(th)}$		-	2.2	-	
Gate to drain charge	Q_{gd}		-	2.0	3.0	
Switching charge	Q_{sw}		-	3.0	-	
Gate charge total	Q_g		-	9.1	12	
Gate plateau voltage	$V_{plateau}$		-	2.3	-	V
Gate charge total	Q_g	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 10 V	-	19	25	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V	-	7.9	-	
Output charge	Q_{oss}	V_{DD}=12 V, V_{GS}=0 V	-	13	17	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	28	A
Diode pulse current	$I_{S,pulse}$		-	-	112	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=30 A, T_j=25 °C	-	0.84	-	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	10	-	nC

[6] See figure 16 for gate charge parameter definition

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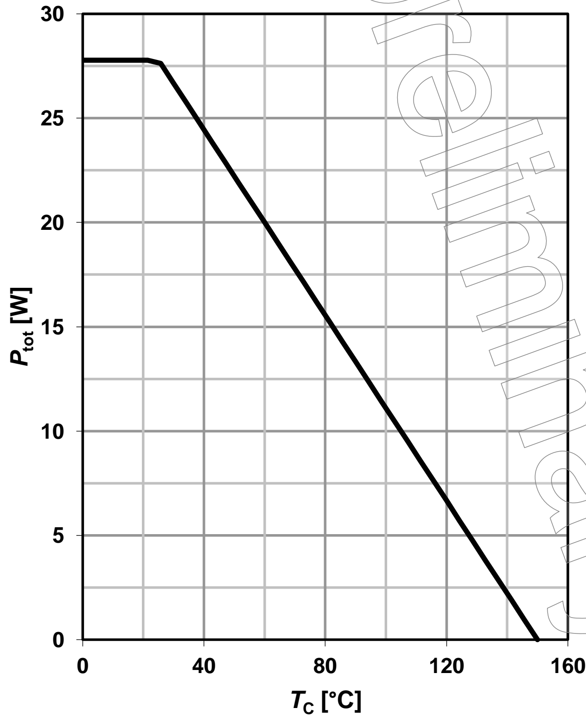
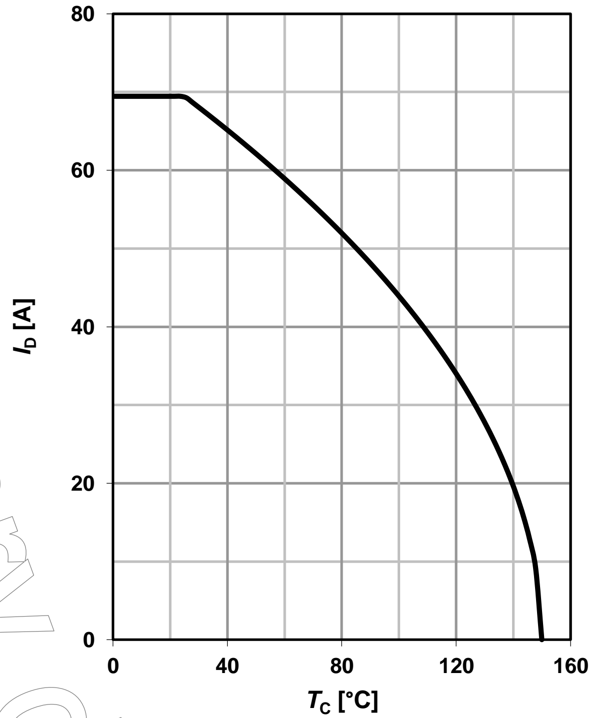
1 Power dissipation

P_{tot}=f(T_C)



2 Drain current

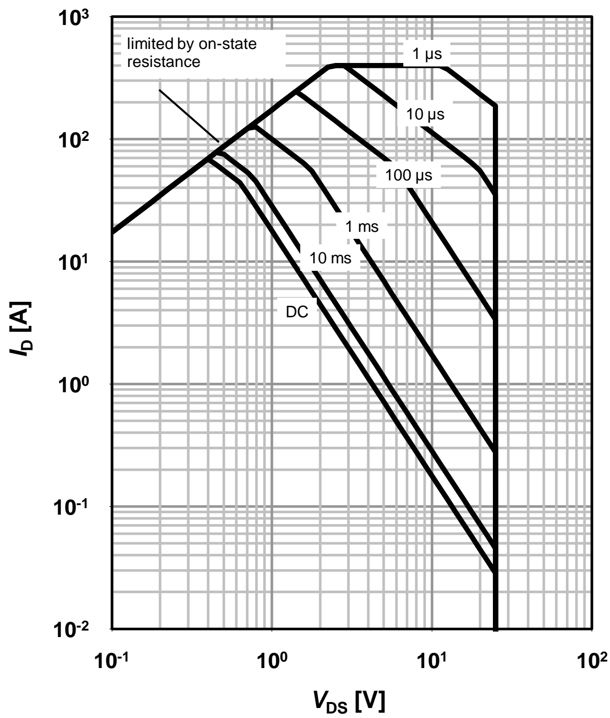
I_D=f(T_C); V_{GS}≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

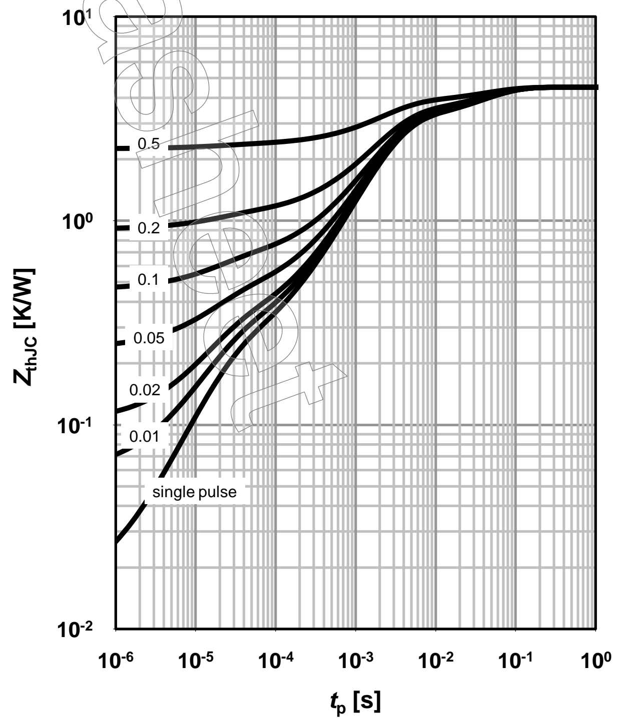
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC}=f(t_p)

parameter: D=t_p/T



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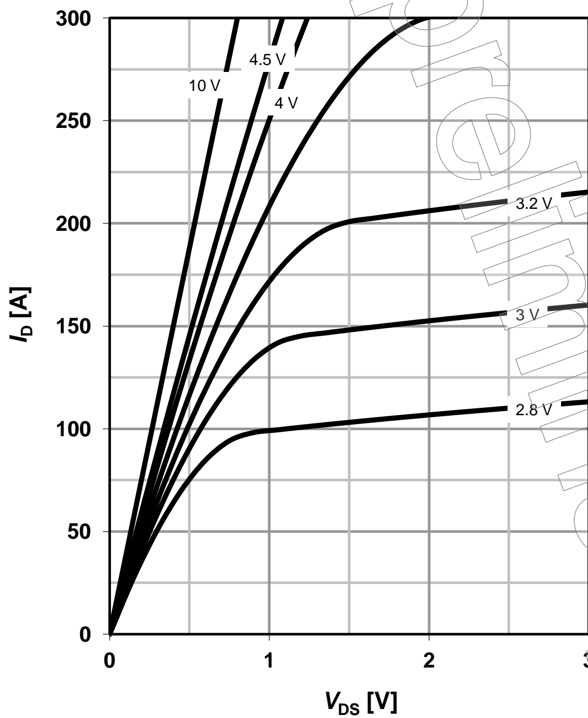
5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

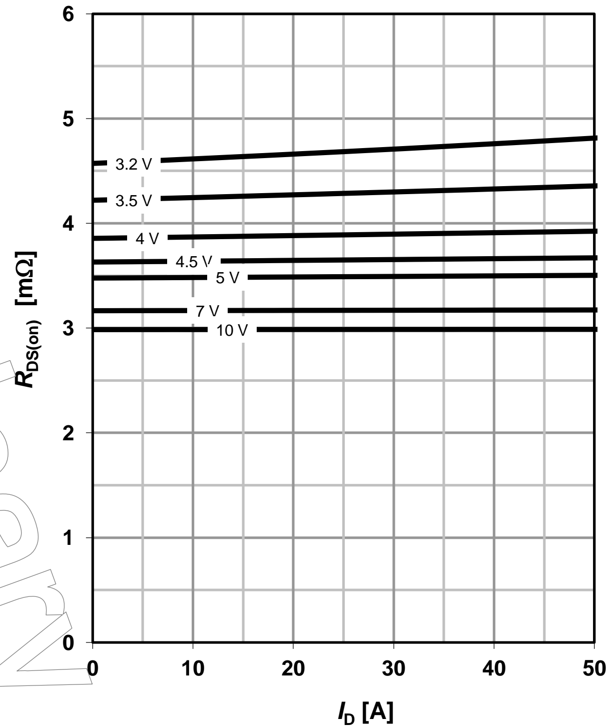
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

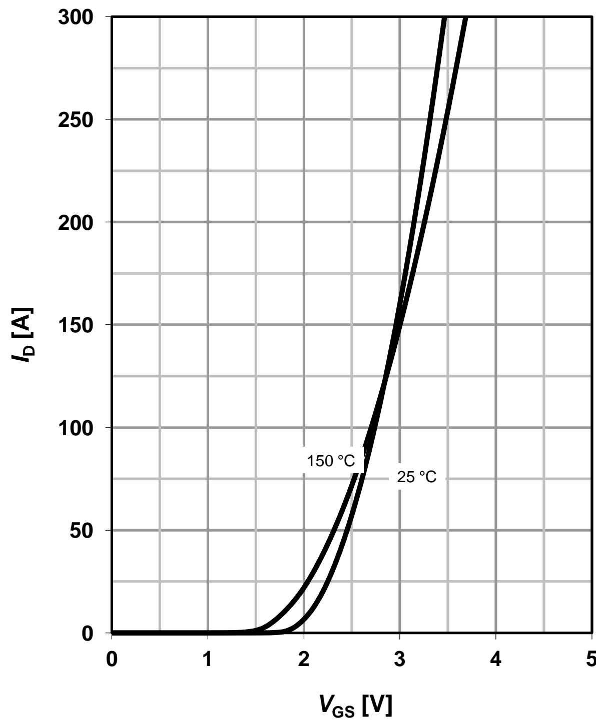
parameter: V_{GS}



7 Typ. transfer characteristics

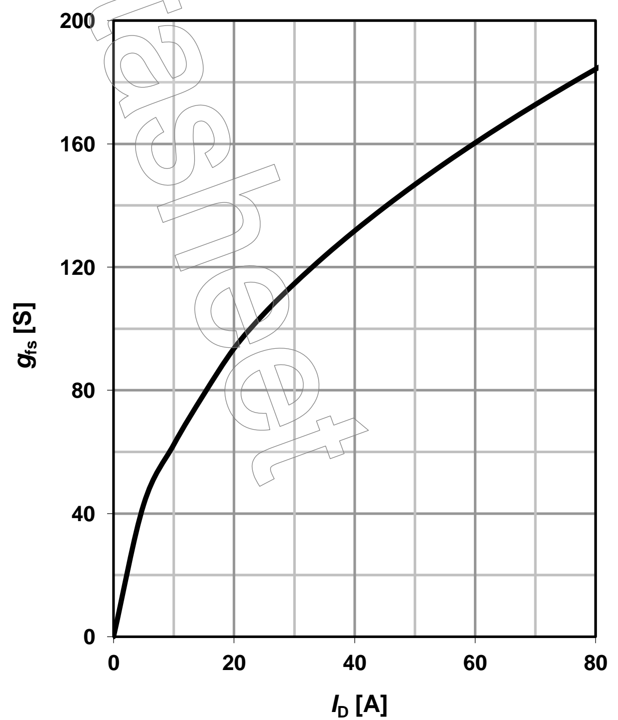
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



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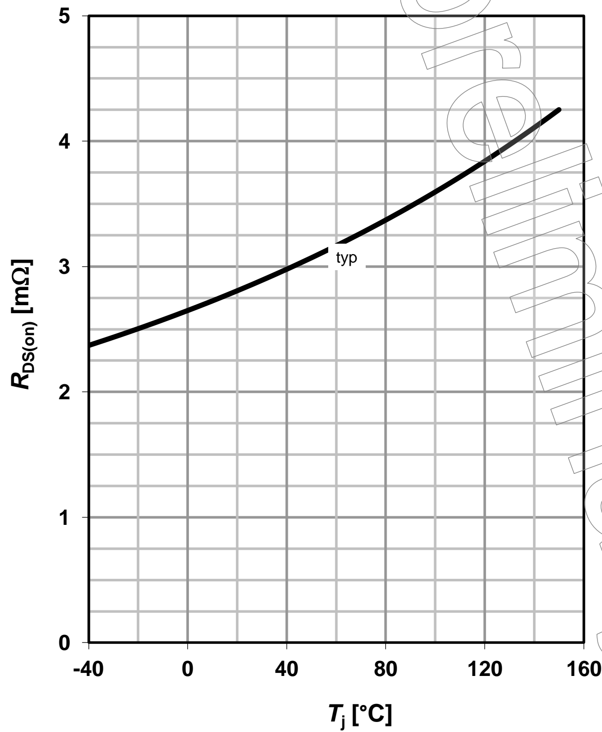
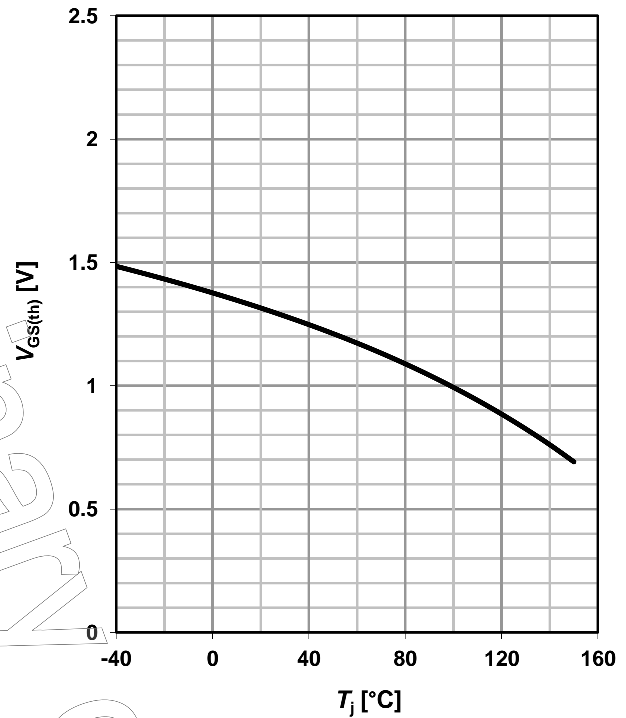
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V



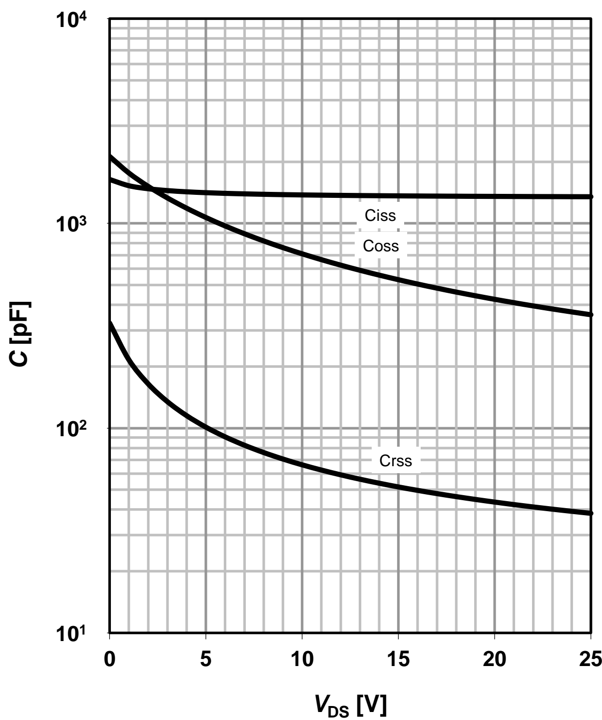
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA



11 Typ. capacitances

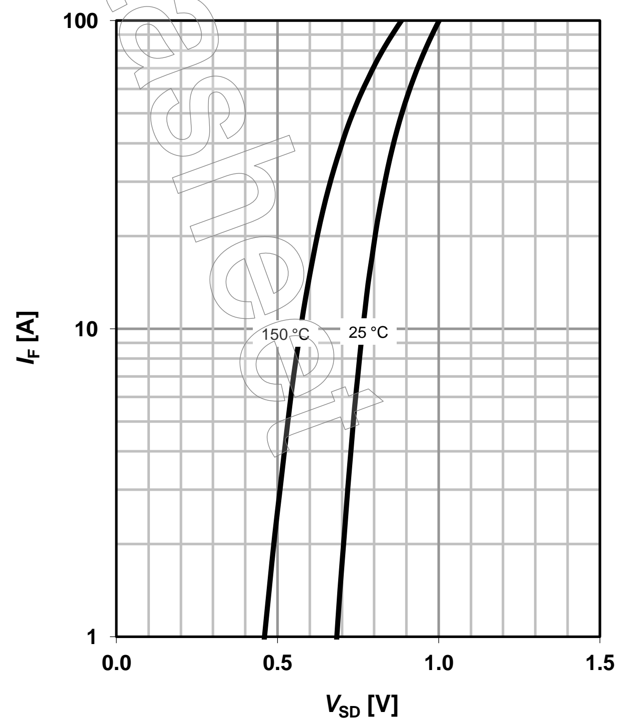
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

parameter: T_j



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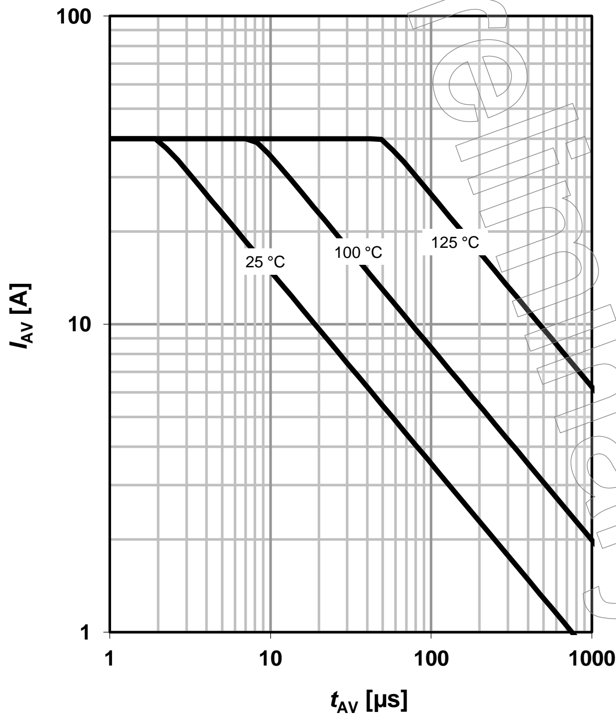
13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

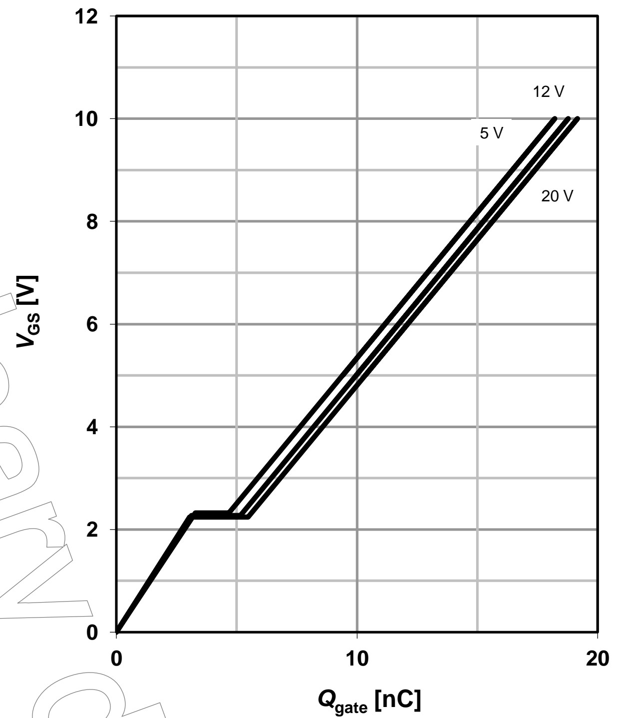
parameter: $T_{j(start)}$



14 Typ. gate charge

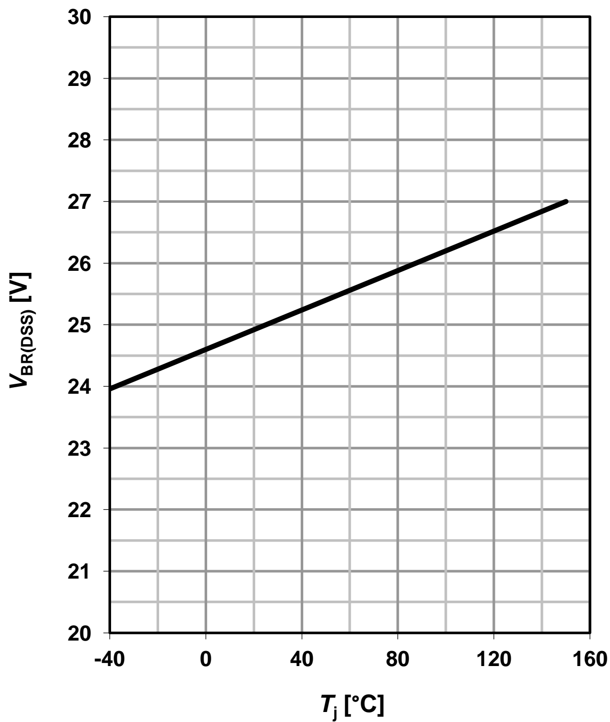
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

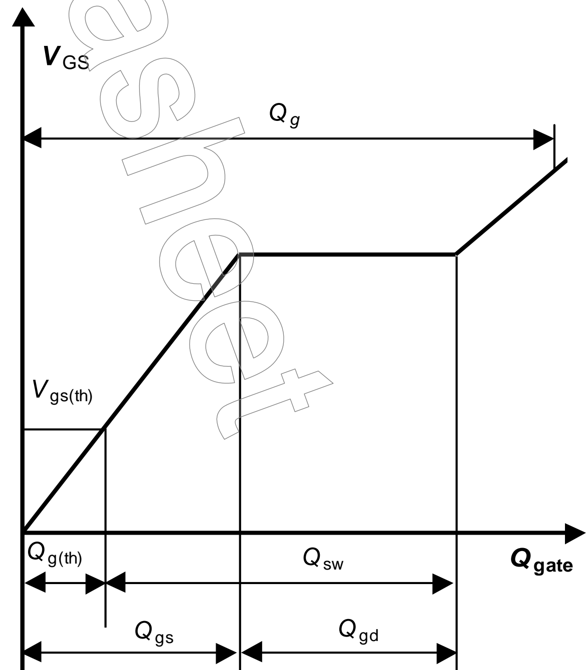


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



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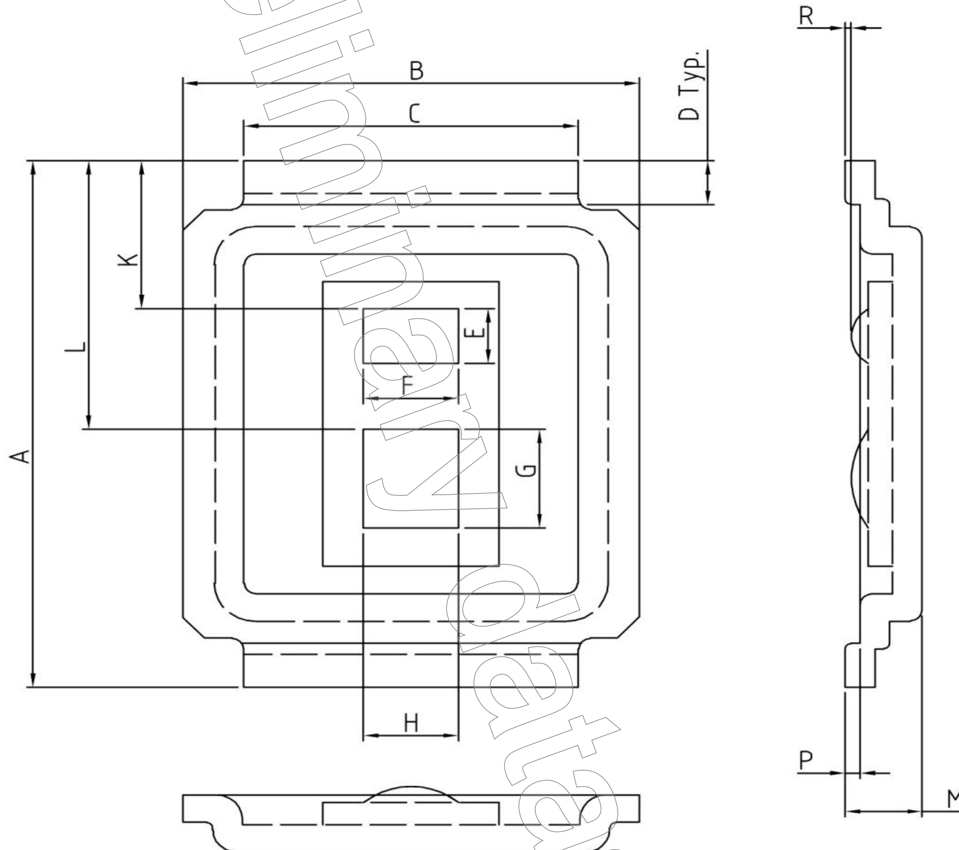
Package Outline

MG-WDSON-2-3/-53



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.75	4.88	0.187	0.192
B	3.70	3.95	0.146	0.156
C	2.75	2.85	0.108	0.112
D	0.35	0.45	0.014	0.018
E	0.48	0.52	0.019	0.020
F	0.78	0.82	0.031	0.032
G	0.88	0.92	0.035	0.036
H	0.78	0.82	0.031	0.032
K	1.25	1.45	0.049	0.057
L	2.35	2.55	0.093	0.100
M	0.60	0.70	0.024	0.028
R	0.00	0.10	0.000	0.004
P	0.08	0.17	0.003	0.007

DOCUMENT NO.
Z8B00134584

SCALE 0 5 7.5mm

EUROPEAN PROJECTION

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02

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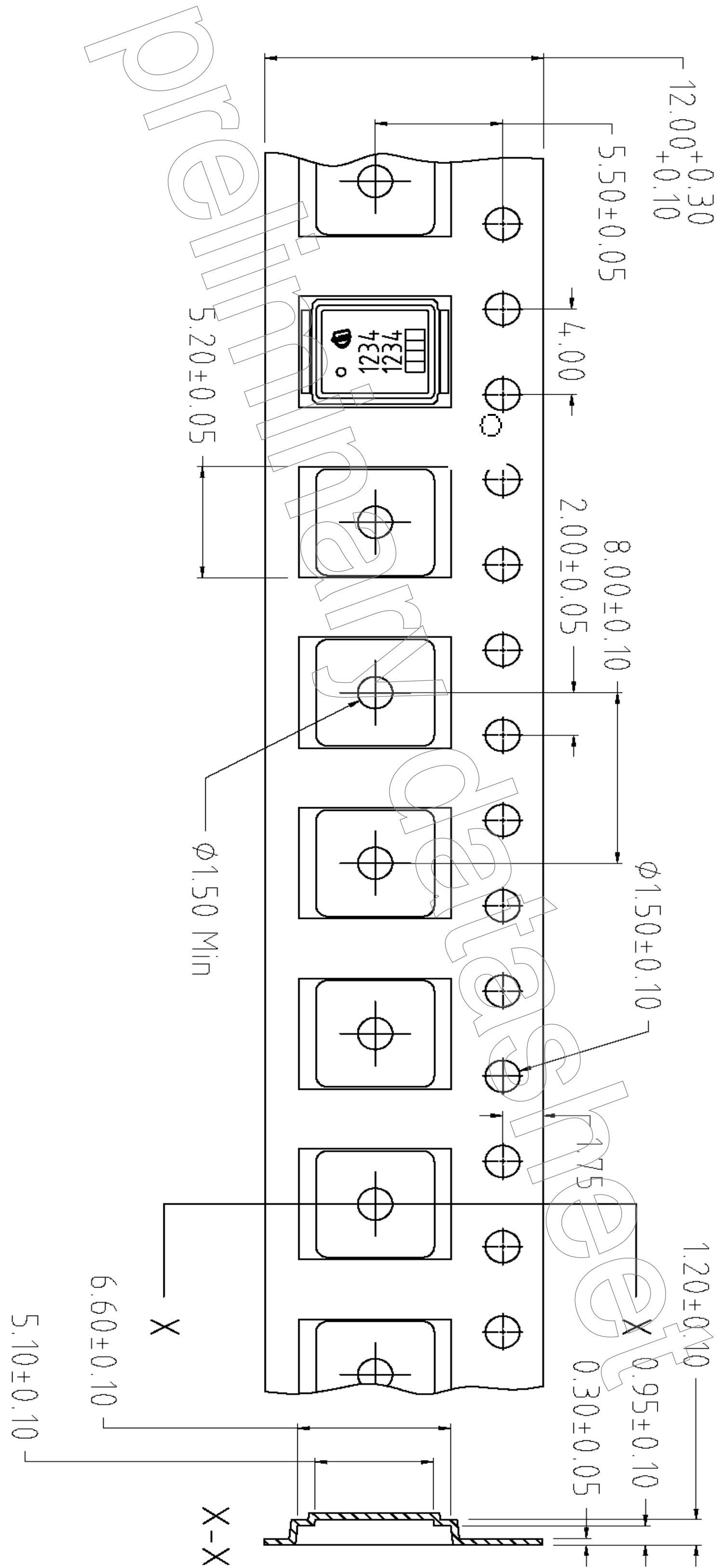
Package Outline **MG-WDSON-2**



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Dimensions in mm

CanPAK SQ: Boardpads & Apertures

SMD

0.900 0.925 0.550 0.550 0.950 1.025 0.900

1.250 0.400 1.250 0.850 2.900

5.800

0.700 1.075 0.450 0.675 0.800 1.200 0.700

1.200 0.500 1.200 0.750 0.750 2.900

5.600

copper solder mask stencil apertures

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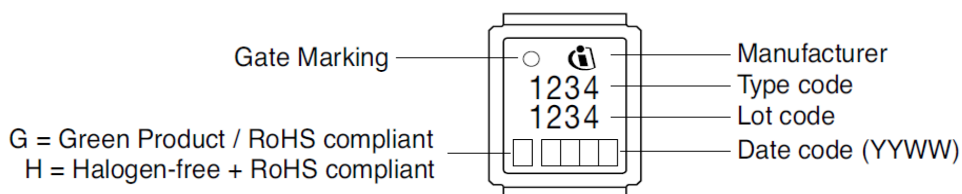
Dimensions in mm

Recommended stencil thickness 150 µm

Marking Layout



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