



# 128Kx24 Asynchronous SRAM, 5V

## FEATURES

- 128Kx24 bit CMOS Static
- Random Access Memory Array
  - Fast Access Times: 12 and 15ns
  - Master Output Enable and Write Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 119 Lead BGA (JEDEC MO-163), No. 391
  - Small Footprint, 14mm x 22mm
  - Multiple Ground Pins for Maximum Noise Immunity
- Single +5V ( $\pm 10\%$ ) Supply Operation
- DSP Memory Solution
  - Motorola DSP5600x™
  - Analog Devices SHARC™

## DESCRIPTION

The EDI8L24128CxxBC is a 5V, three megabit SRAM constructed with three 128Kx8 die mounted on a multi-layer laminate substrate. With 12 to 15ns access times, x24 width and a 5V operating voltage, the EDI8L2418C is ideal for creating a single chip memory solution for the Motorola DSP5600x or a two chip solution for the Analog Devices SHARC™ DSP.

The single or dual chip memory solutions offer improved system performance by reducing the length of board traces and the number of board connections compared to using multiple monolithic devices. For example, the capacitance load on the data lines for the BGA package is 58% less than a monolithic SOJ solution.

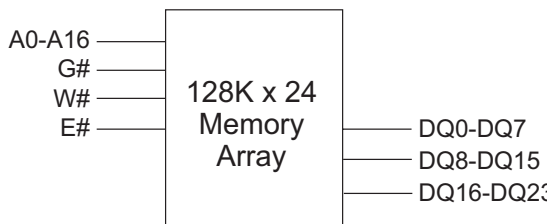
The JEDEC Standard 119 lead BGA provides a 44% space savings over using 128Kx8, 300mm wide SOJs and the BGA package has a height of 100mm compared to 148mm for the SOJ packages.

**FIG. 1 PIN CONFIGURATION**

	1	2	3	4	5	6	7
A	NC	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	NC
B	NC	A <sub>5</sub>	A <sub>6</sub>	E	A <sub>7</sub>	A <sub>8</sub>	NC
C	DQ <sub>12</sub>	NC	NC	NC	NC	NC	DQ <sub>0</sub>
D	DQ <sub>13</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	DQ <sub>1</sub>
E	DQ <sub>14</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	DQ <sub>2</sub>
F	DQ <sub>15</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	DQ <sub>3</sub>
G	DQ <sub>16</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	DQ <sub>4</sub>
H	DQ <sub>17</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	DQ <sub>5</sub>
I	NC	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	NC
J	DQ <sub>18</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	DQ <sub>6</sub>
K	DQ <sub>19</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	DQ <sub>7</sub>
L	DQ <sub>20</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	DQ <sub>8</sub>
M	DQ <sub>21</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	DQ <sub>9</sub>
N	DQ <sub>22</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	DQ <sub>10</sub>
O	DQ <sub>23</sub>	NC	NC	NC	NC	NC	DQ <sub>11</sub>
P	NC	A <sub>9</sub>	A <sub>10</sub>	W	A <sub>11</sub>	A <sub>12</sub>	NC
Q	NC	A <sub>13</sub>	A <sub>14</sub>	G	A <sub>15</sub>	A <sub>16</sub>	NC

**Pin DESCRIPTION**

A0-16	Address Inputs
E#	Chip Enables
W#	Master Write Enable
G3	Master Output Enable
DQ0-23	Common Data
	Input/Output
V <sub>CC</sub>	Power (+5V $\pm 10\%$ )
GND	Ground
NC	No Connection





**Absolute Maximum Ratings\***

Voltage on any pin relative to Vss	-0.5V to 7.0V
Operating Temperature Ts (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	3 Watts
Output Current	20 mA
Junction Temperature, Tj	175°C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Truth Table**

E#	W#	G#	Mode	Output	Power
H	X	X	Standby	High Z	I <sub>CC2</sub> , I <sub>CC3</sub>
L	H	H	Output Deselect	High Z	I <sub>CC1</sub>
L	H	L	Read	Data Out	I <sub>CC1</sub>
L	L	X	Write	Data In	I <sub>CC1</sub>

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Supply Voltage	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	—	+0.8	V

**Capacitance**

(f=1.0MHz, V<sub>IN</sub>=V<sub>CC</sub> OR V<sub>SS</sub>)

Parameter	Symbol	Max	Unit
Address Lines	CL	8	pf
Data Lines	C <sub>D/Q</sub>	10	pf
Write & Output Enable Line	W#, G#	8	pf
Chip Enable Lines	E#	8	pf

**DC Electrical Characteristics**

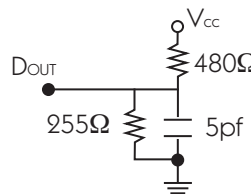
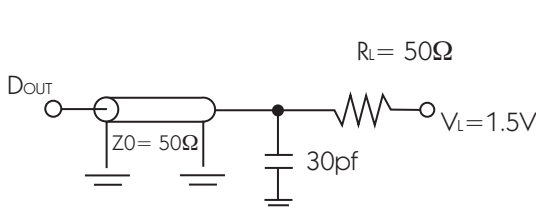
(V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions	Min	Type	Max	Units
Operating Power Supply Current	I <sub>CC1</sub>	W# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA, Min Cycle	200	270		mA
Standby (TTL) Power Supply Current	I <sub>CC2</sub>	E# ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub> , f = 0MHz		45		mA
Full Standby Power CMOS	I <sub>CC3</sub>	E# ≥ V <sub>CC</sub> - 0.2V			10	mA
Supply Current		V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≥ 0.2V				
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0V to V <sub>CC</sub>	—	±10		µA
Output Leakage Current	I <sub>LO</sub>	V <sub>I/O</sub> 0V to V <sub>CC</sub>	—	—	±10	µA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4	—	—	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA	—	—	0.4	V

**AC Test Conditions**

**Fig. 1**

**Fig. 2**



Input Pulse Levels	V <sub>SS</sub> to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

Note: For t<sub>EHQZ</sub>, t<sub>GHQZ</sub> and t<sub>WLQZ</sub>, CL = 5pF Figure 2



## AC Characteristics Read Cycle

Parameter	Symbol		12ns		15ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	12		15		ns
Address Access Time	tAVQV	tAA		12		15	ns
Chip Enable Access Time	tELQV	tACS		12		15	ns
Chip Enable to Output in Low Z <sup>1</sup>	tELQX	tCLZ	3		3		ns
Chip Disable to Output in High Z <sup>1</sup>	tEHQZ	tCHZ		6		7	ns
Output Hold from Address Change	tAVQX	tOH	3		3		ns
Output Enable to Output Valid	tGLQV	tOE		6		7	ns
Output Enable to Output in Low Z <sup>1</sup>	tGLQX	tOLZ	0		0		ns
Output Disable to Output in High Z <sup>1</sup>	tGHQZ	tOHZ		6		7	ns

1. This parameter is guaranteed by design but not tested.

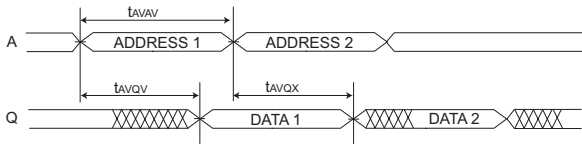
## AC Characteristics Write Cycle

Parameter	Symbol		12ns		15ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	12		15		ns
Chip Enable to End of Write	tELWH	tCW	9		9		ns
	tELEH	tCW	9		9		ns
Address Setup Time	tAVWL	tAS	0		0		ns
	tAVEL	tAS	0		0		ns
Address Valid to End of Write	tAVWH	tAW	9		10		ns
	tAVEH	tAW	9		10		ns
Write Pulse Width	tWLWH	tWP	10		11		ns
	tELEH	tWP	10		11		ns
Write Recovery Time	tWHAX	tWR	0		0		ns
	tEHAX	tWR	0		0		ns
Data Hold Time	tWHDX	tDH	0		0		ns
	tEHDX	tDH	0		0		ns
Write to Output in High Z <sup>1</sup>	tWLQZ	tWHZ	0	6	0	7	ns
Data to Write Time	tDVWH	tDW	6		7		ns
	tDVEH	tDW	6		7		ns
Output Active from End of Write <sup>1</sup>	tWHQX	tWLZ	3		3		ns

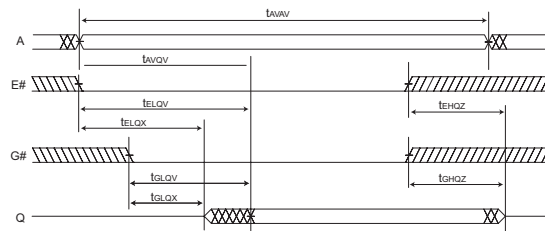
1. This parameter is guaranteed by design but not tested.



**FIG. 2**  
**TIMING WAVEFORM — READ CYCLE**

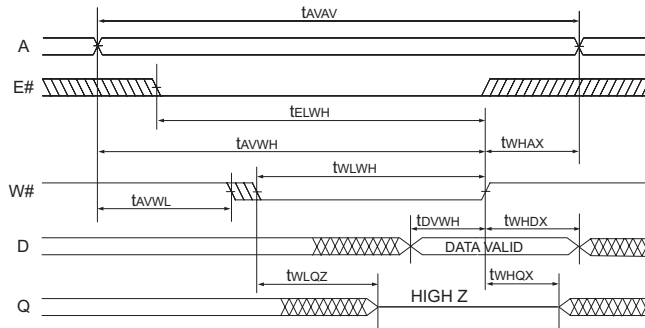


Read Cycle 1 (W# High; G, E Low)

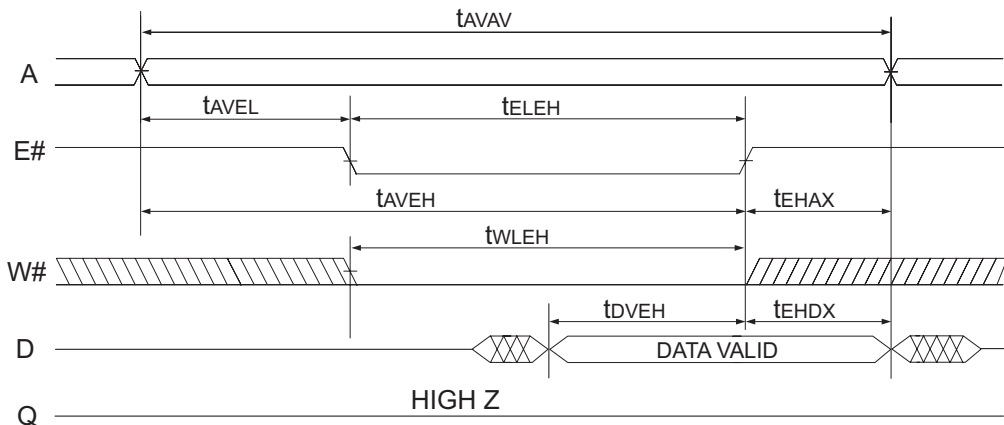


Read Cycle 2 (W# High)

**FIG. 3**  
**WRITE CYCLE — W# CONTROLLED**

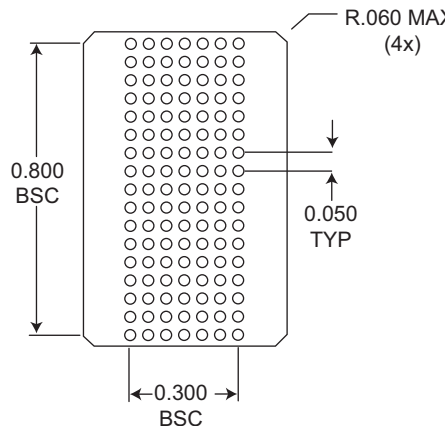
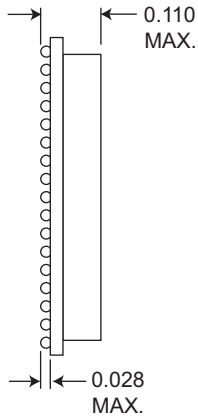
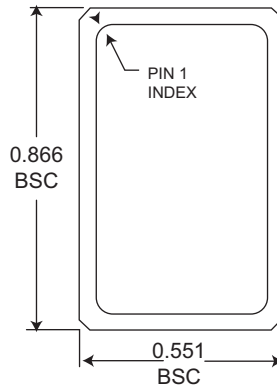


**FIG. 4**  
**WRITE CYCLE — E# CONTROLLED**





**PACKAGE 391:  
119 LEAD BGA JEDEC MO-163**



ALL DIMENSIONS ARE IN INCHES

**ORDERING INFORMATION**

**Commercial (0°C to +70°C)**

Part Number	Speed (ns)	Package No.
EDI8L24128C12BC	12	391
EDI8L24128C15BC	15	391

**Industrial (-40°C to +85°C)**

Part Number	Speed (ns)	Package No.
EDI8L24128C12BI	12	391
EDI8L24128C15BI	15	391