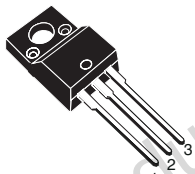
STF11N65K3

N-channel 650 V, 0.765 Ω, 11 A, TO-220FP SuperMESH3™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	P_{tot}
STF11N65K3	650 V	< 0.85 Ω	11 A	35 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Improved diode reverse recovery characteristics
- Zener-protected



TO-220FP

Applications

- Switching applications

Description

This device is an N-channel Zener-protected SuperMESH3™ Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Figure 1. Internal schematic diagram

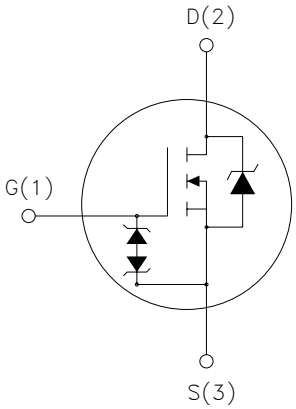


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF11N65K3	11N65K3	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain source voltage (V_{GS}=0)	650	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	11	A
I_D	Drain current (continuous) at T_C = 100 °C	6.3	A
I_{DM} (1)	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at T_C = 25 °C	35	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	7.2	A
E_{AS}	Single pulse avalanche energy (2)	212	mJ
	Derating factor	0.28	W/°C
dv/dt (3)	Peak diode recovery voltage slope	12	V/ns
$V_{ESD(G-S)}$	G-S ESD (HBM C=100 pF, R=1.5 kΩ)	2500	V
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area.
2. Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V
3. I_{SD} ≤11 A, di/dt ≤400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$, $V_{DS\ peak}$ < $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	3.57	°C/W
$Rt_{hj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V V_{DS} = 650 V, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3		4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 3.6 A		0.765	0.85	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	1180 125 14	-	pF pF pF
$C_{oss\ eq.}$	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0	-	77	-	pF
R_G	Intrinsic gate resistnce	f=1 MHz open drain	-	3	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 7.2 A, V_{GS} = 10 V (see *Figure 16*)	-	42 7.4 23	-	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 310 V, I_D = 3.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15*)	-	14.5 14 44 35	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		7.2 28.8	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 7 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7 A, di/dt = 100A/µs V_{DD} = 60 V (see *Figure 20*)	-	320 2 13		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 20*)	-	410 2.9 14		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

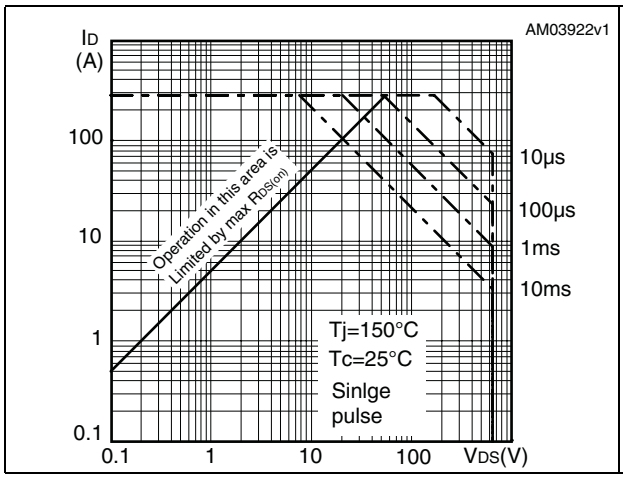


Figure 3. Thermal impedance

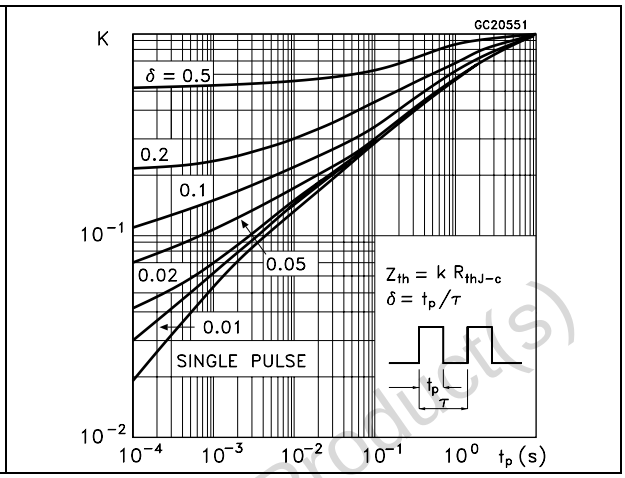


Figure 4. Output characteristics

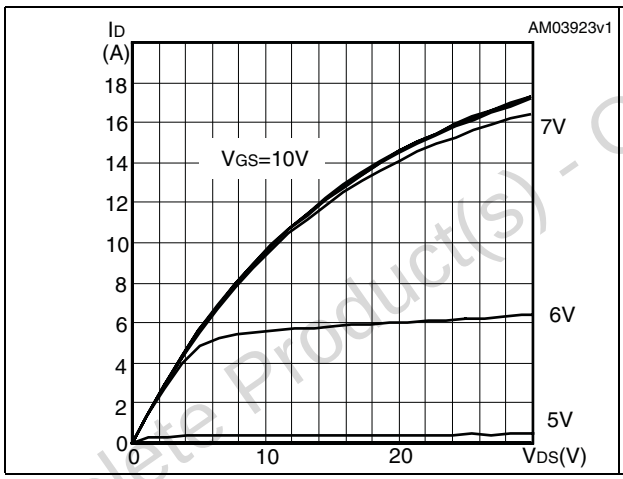


Figure 5. Transfer characteristics

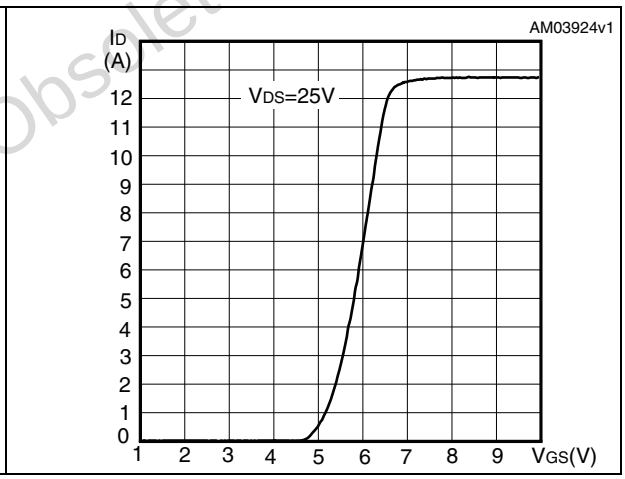


Figure 6. Normalized BV_{DSS} vs temperature

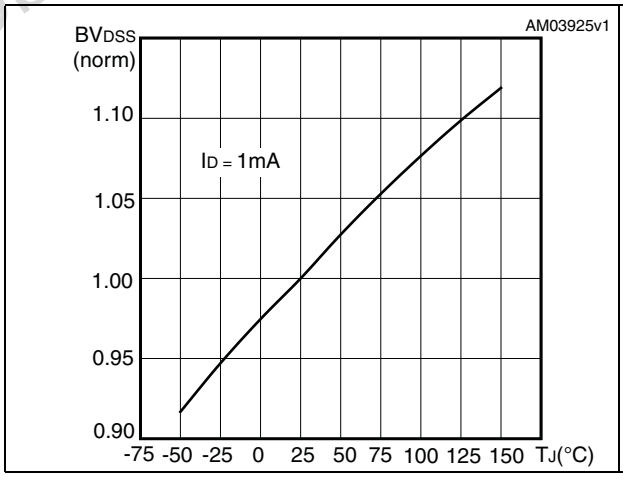


Figure 7. Static drain-source on resistance

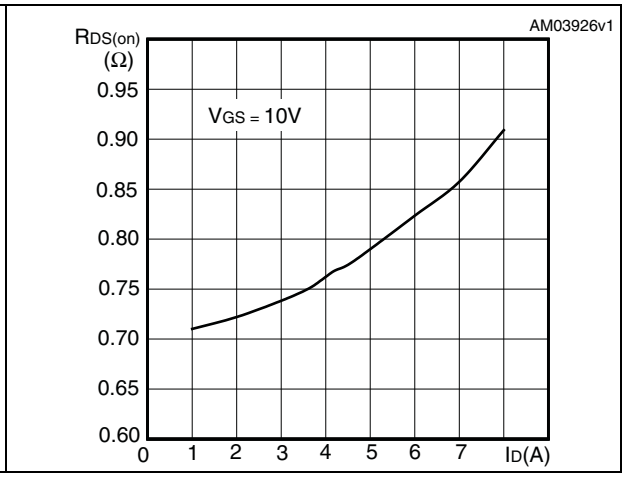


Figure 8. Output capacitance stored energy

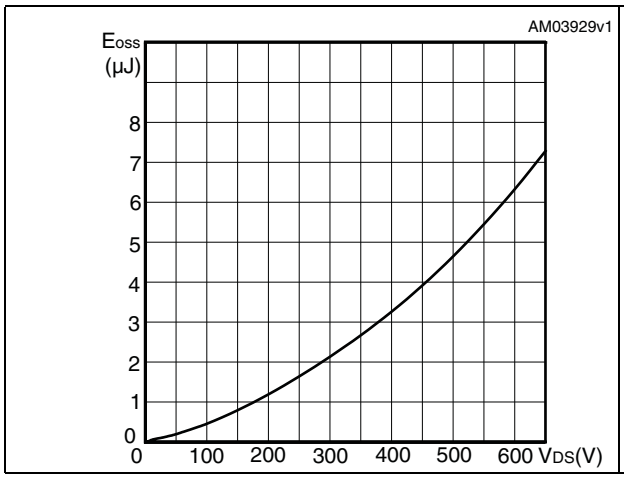


Figure 9. Capacitance variations

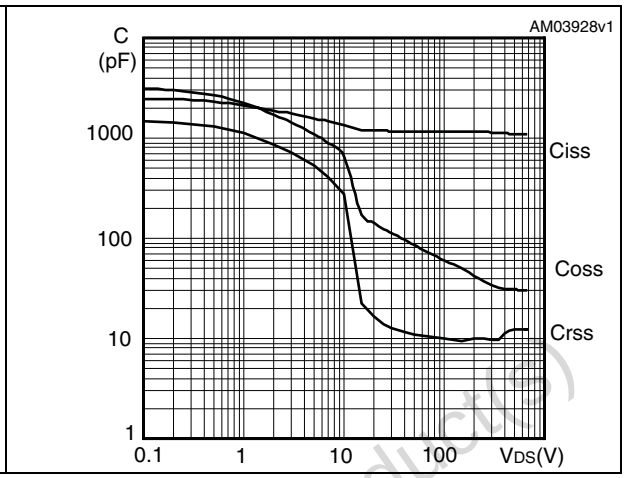


Figure 10. Gate charge vs gate-source voltage

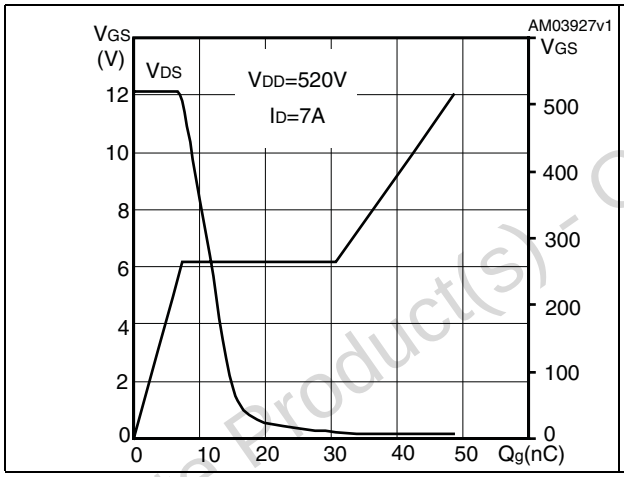


Figure 11. Normalized on resistance vs temperature

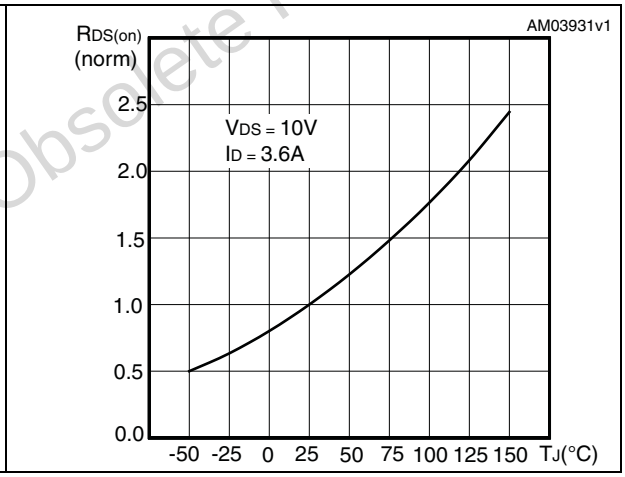


Figure 12. Normalized gate threshold voltage vs temperature

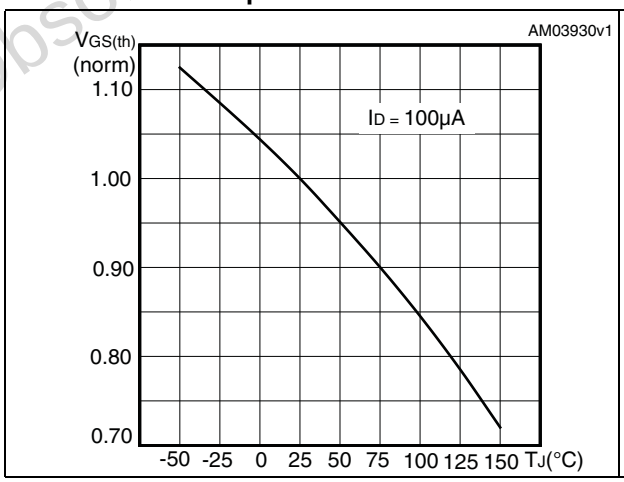


Figure 13. Maximum avalanche energy vs temperature

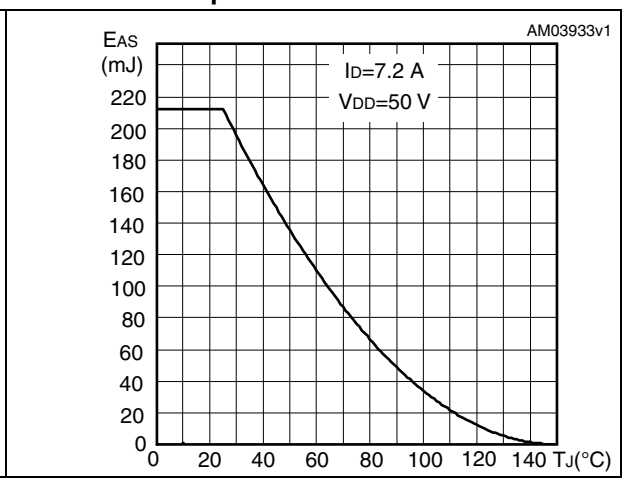
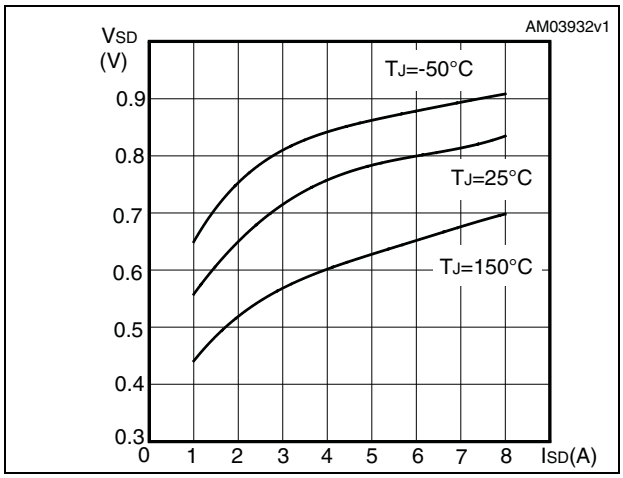


Figure 14. Source-drain diode forward characteristics



3 Test circuits

Figure 15. Switching times test circuit for resistive load

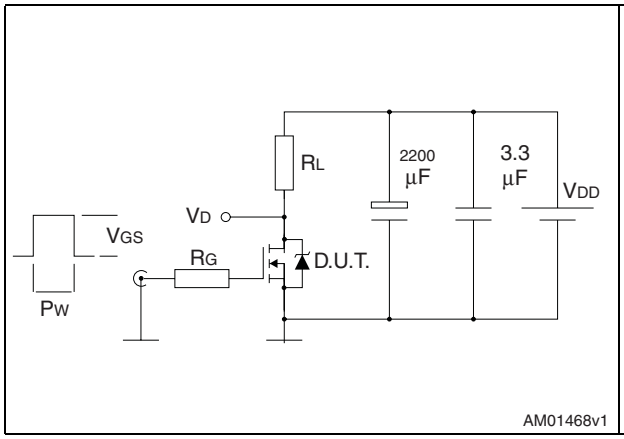


Figure 16. Gate charge test circuit

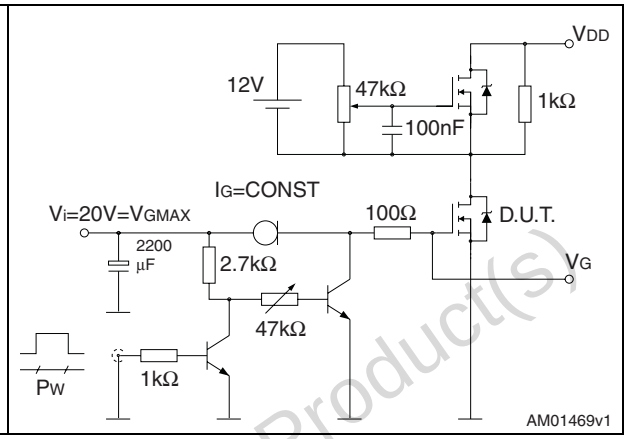


Figure 17. Test circuit for inductive load switching and diode recovery times

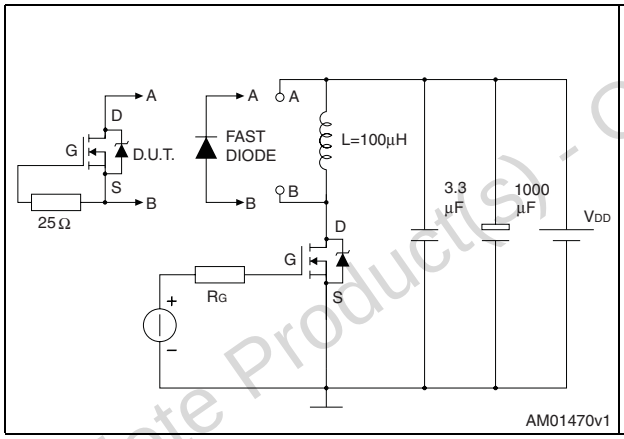


Figure 18. Unclamped inductive load test circuit

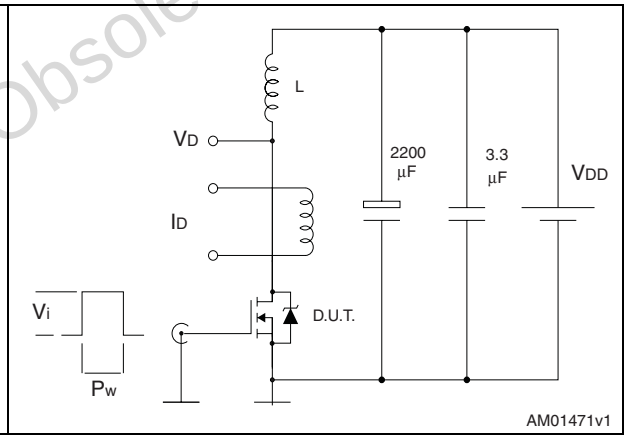


Figure 19. Unclamped inductive waveform

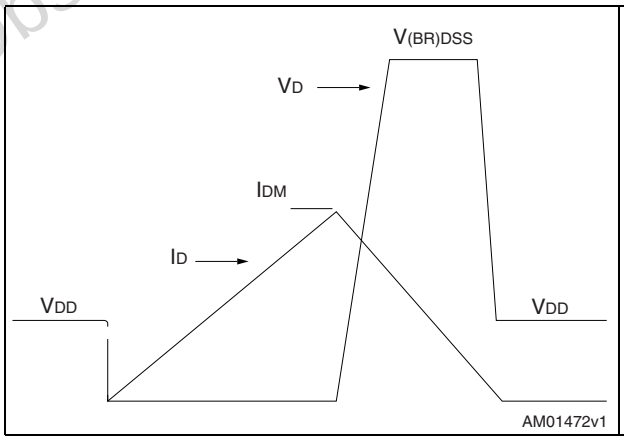
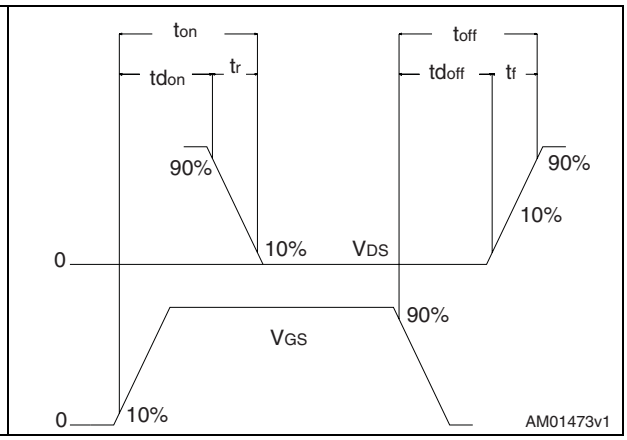


Figure 20. Switching time waveform



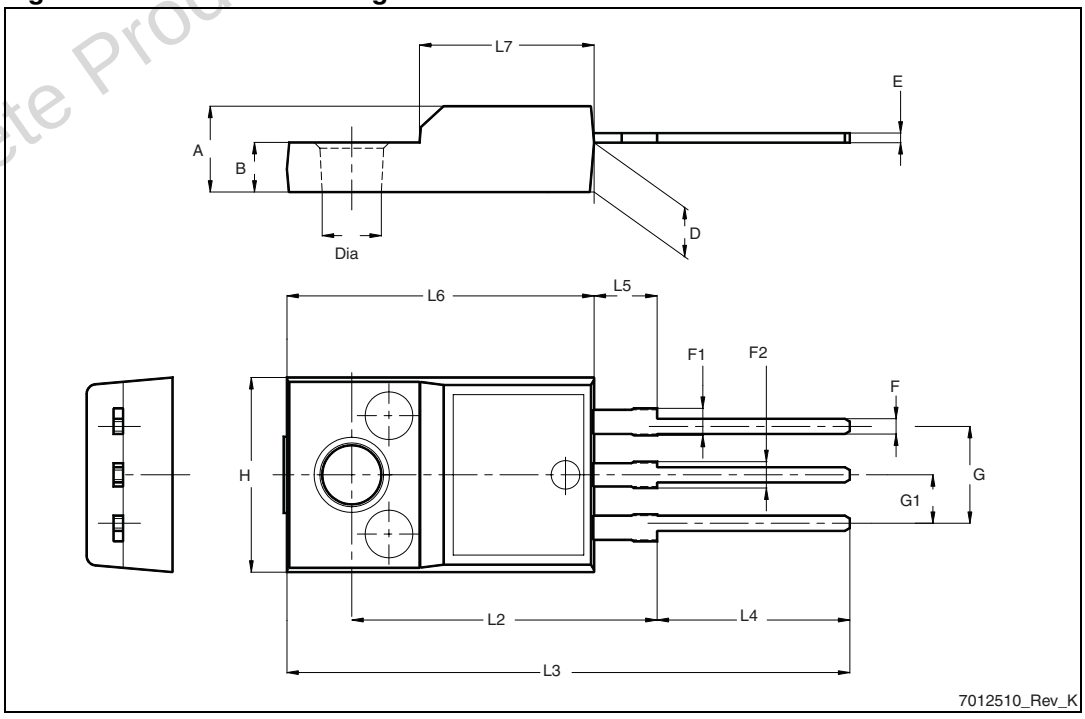
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 21. TO-220FP drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
10-Sep-2010	1	First release
03-Oct-2011	2	Updated *Figure 6: Normalized BV_{DSS} vs temperature*, *Figure 7: Static drain-source on resistance*, *Figure 10: Gate charge vs gate-source voltage*, *Figure 11: Normalized on resistance vs temperature*, *Figure 12: Normalized gate threshold voltage vs temperature*. Minor text changes.

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