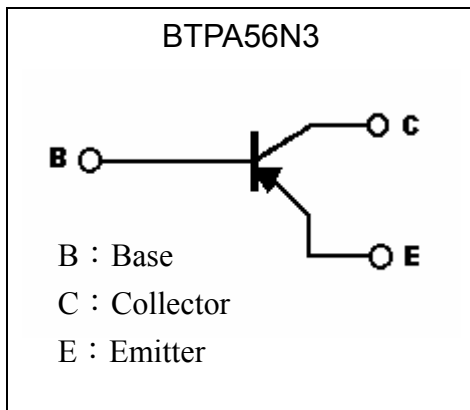
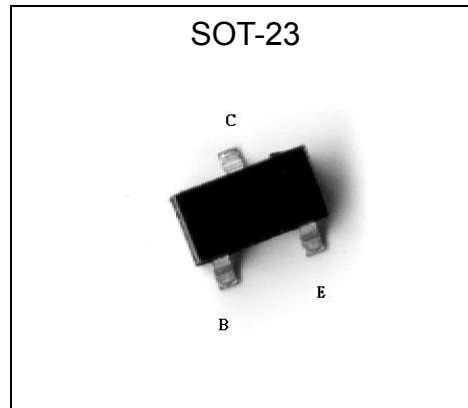


**PNP Epitaxial Planar Transistor**

# BTPA56N3

**Features**

- Low  $V_{CE(sat)}$ ,  $V_{CE(sat)} = -0.07$  V (typ), at  $I_C / I_B = -100\text{mA} / -10\text{mA}$
- Excellent current gain characteristics
- Pb-free lead plating and halogen-free package

**Symbol**

**Outline**

**Absolute Maximum Ratings** ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	$V_{CBO}$	-80	V
Collector-Emitter Voltage	$V_{CEO}$	-80	
Emitter-Base Voltage	$V_{EBO}$	-5	
Collector Current (DC)	$I_C$	-500	mA
Collector Current (Pulse)	$I_{CP}$	-1 (Note 1)	A
Base Current	$I_B$	-200	mA
Power Dissipation	$P_D$	0.225	W
Power Dissipation		0.35 (Note 2)	
Operating Junction and Storage Temperature Range	$T_j ; T_{stg}$	-65~+150	$^\circ\text{C}$

**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	556	°C/W
Thermal Resistance, Junction-to-ambient, max (Note 2)	$R_{th,j-a}$	357	°C/W

Note : 1. Single Pulse ,  $P_w=300\mu s$ , duty cycle $\leq 2\%$ .  
2. Device mounted on FR-4 board 1.6" x 1.6" x 0.06" .

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
$BV_{CBO}$	-80	-	-	V	$I_C=-100\mu A, I_E=0$
$BV_{CEO}$	-80	-	-	V	$I_C=-1mA, I_B=0$
$BV_{EBO}$	-5	-	-	V	$I_E=-100\mu A, I_C=0$
$I_{CBO}$	-	-	-100	nA	$V_{CB}=-80V, I_E=0$
$I_{CES}$	-	-	-100	nA	$V_{CB}=-60V, I_E=0$
$I_{EBO}$	-	-	-100	nA	$V_{EB}=-5V, I_C=0$
* $V_{CE(sat)}$	-	-70	-250	mV	$I_C=-100mA, I_B=-10mA$
* $V_{BE(sat)}$	-	-0.8	-1.2	V	$I_C=-100mA, I_B=-10mA$
* $V_{BE(on)}$	-	-0.73	-1.2	V	$V_{CE}=-1V, I_C=-100mA$
* $h_{FE 1}$	100	-	-	-	$V_{CE}=-1V, I_C=-10mA$
* $h_{FE 2}$	100	-	-	-	$V_{CE}=-1V, I_C=-100mA$
$f_T$	50	200	-	MHz	$V_{CE}=-1V, I_C=-100mA, f=100MHz$
Cob	-	7	-	pF	$V_{CB}=-10V, f=1MHz$

\*Pulse Test : Pulse Width  $\leq 380\mu s$ , Duty Cycle $\leq 2\%$

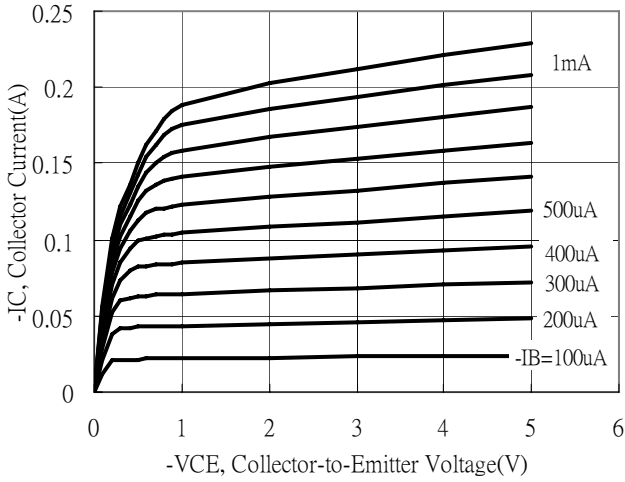
**Ordering Information**

Device	Package	Shipping
BTPA56N3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel

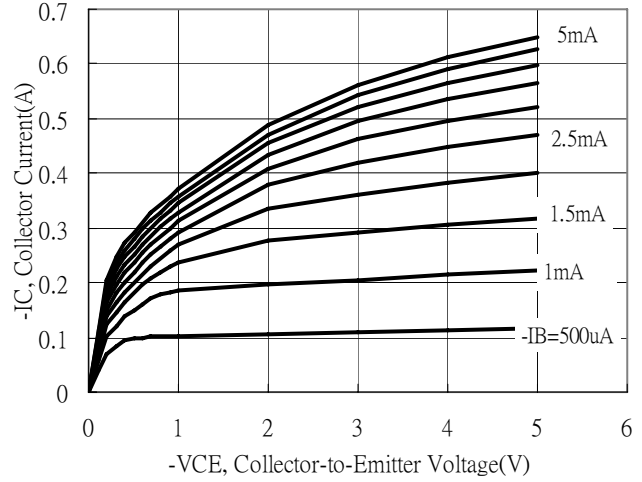


### Typical Characteristics

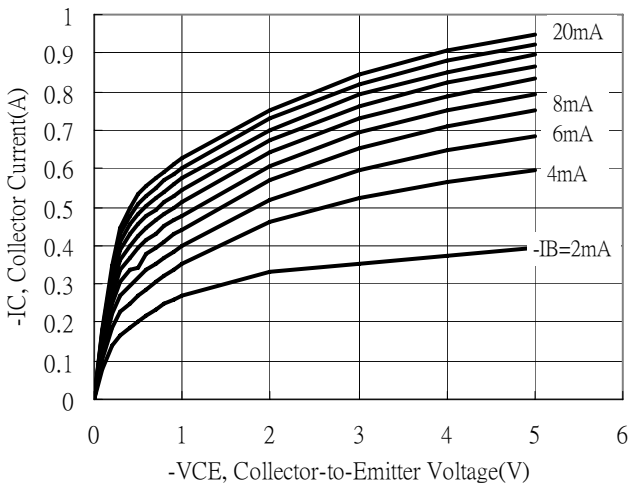
Emitter Grounded Output Characteristics



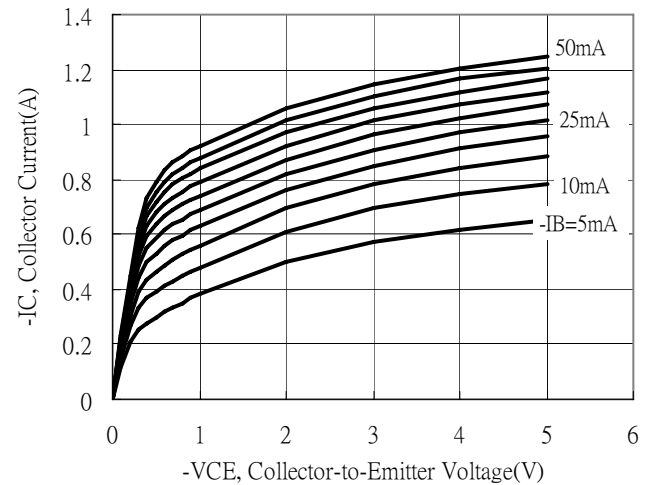
Emitter Grounded Output Characteristics



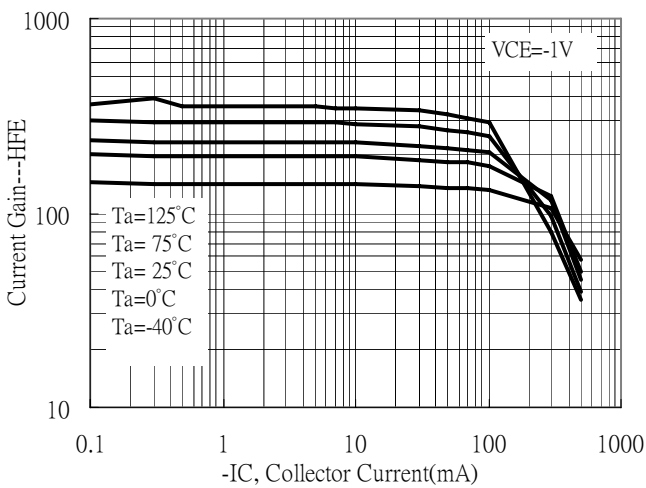
Emitter Grounded Output Characteristics



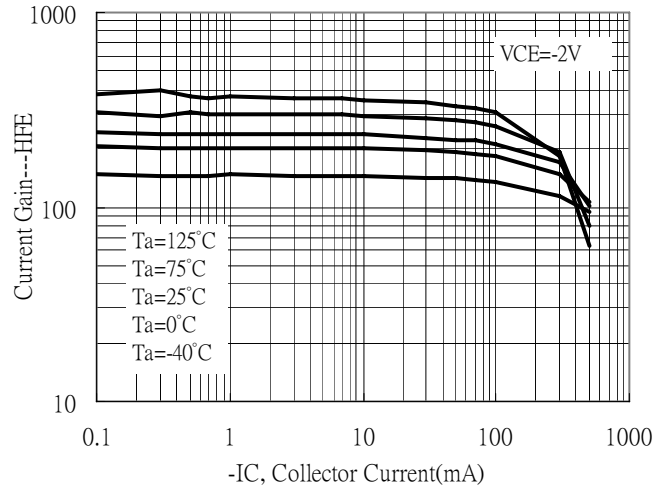
Emitter Grounded Output Characteristics



Current Gain vs Collector Current



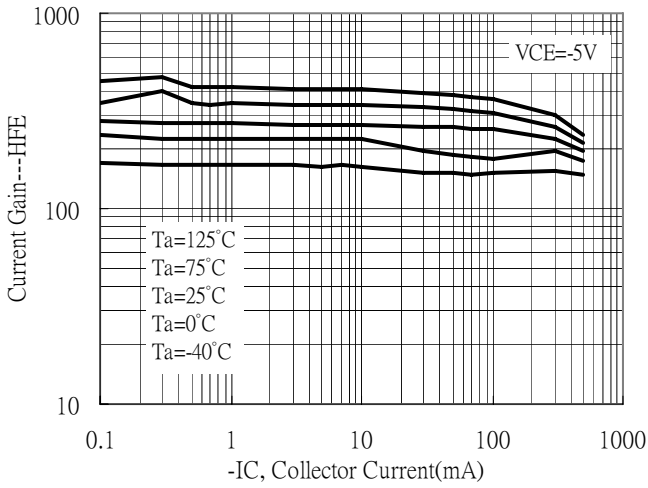
Current Gain vs Collector Current



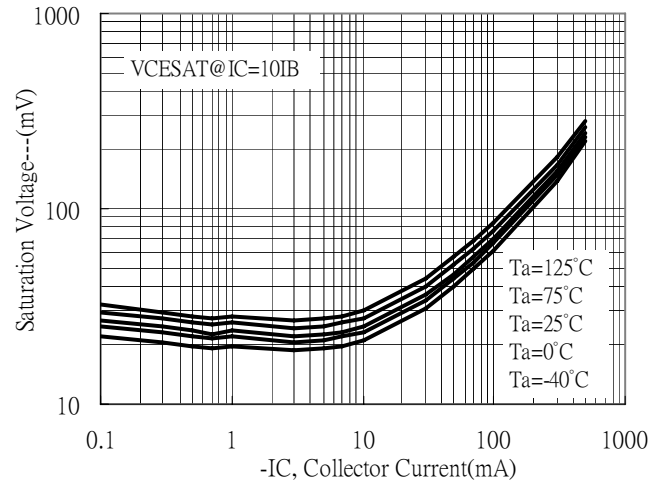


### Typical Characteristics(Cont.)

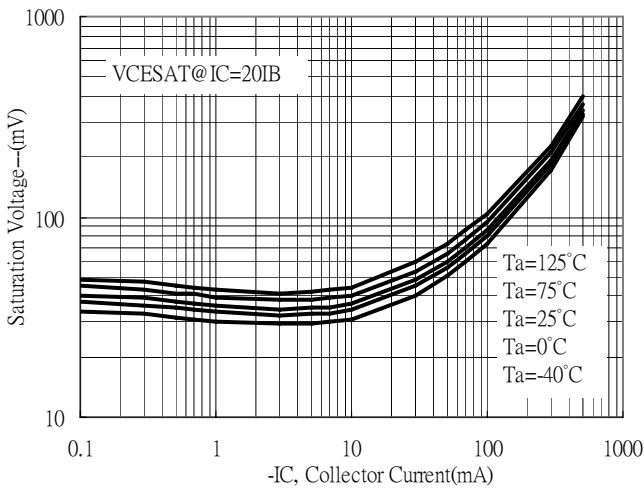
Current Gain vs Collector Current



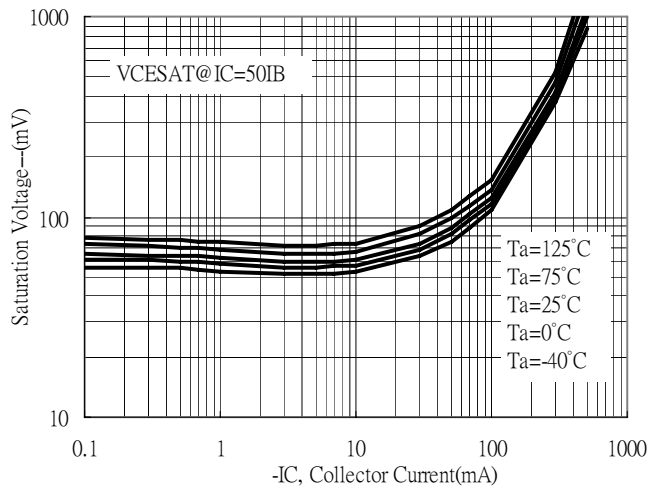
Saturation Voltage vs Collector Current



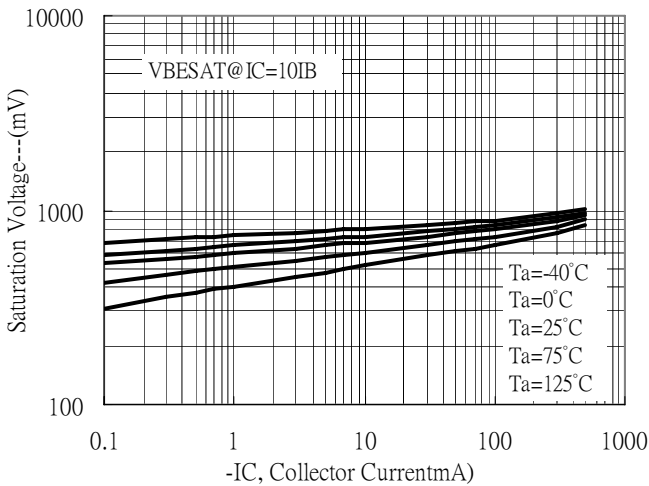
Saturation Voltage vs Collector Current



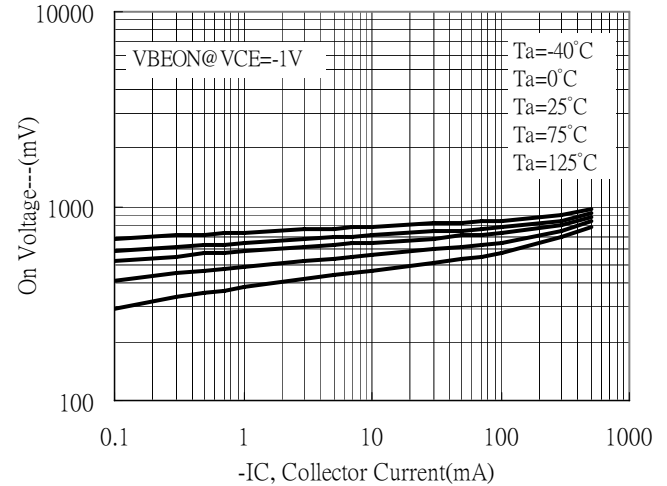
Saturation Voltage vs Collector Current



Saturation Voltage vs Collector Current



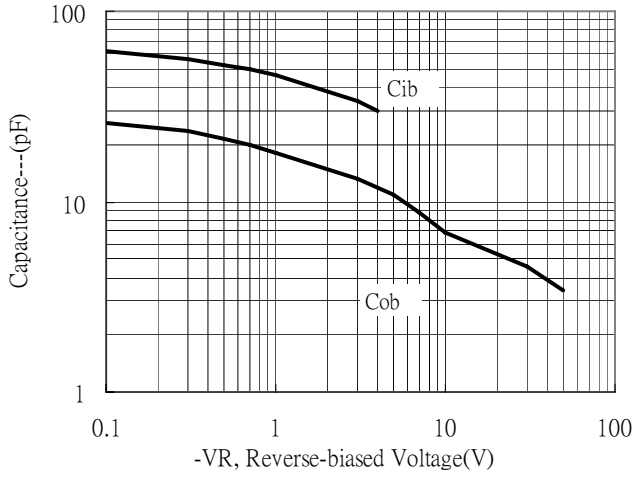
On Voltage vs Collector Current



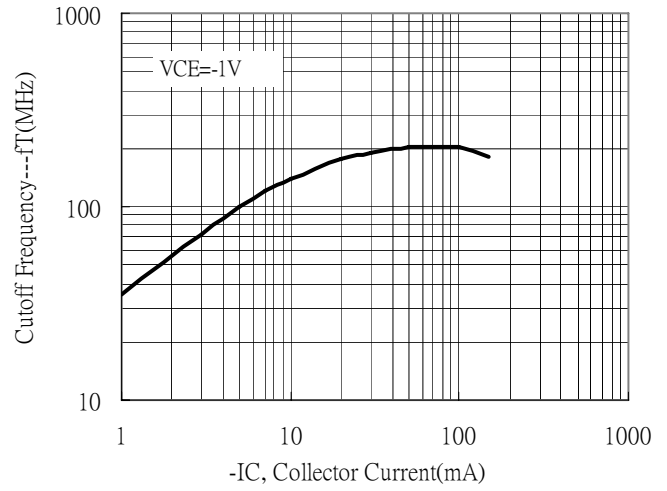


### Typical Characteristics(Cont.)

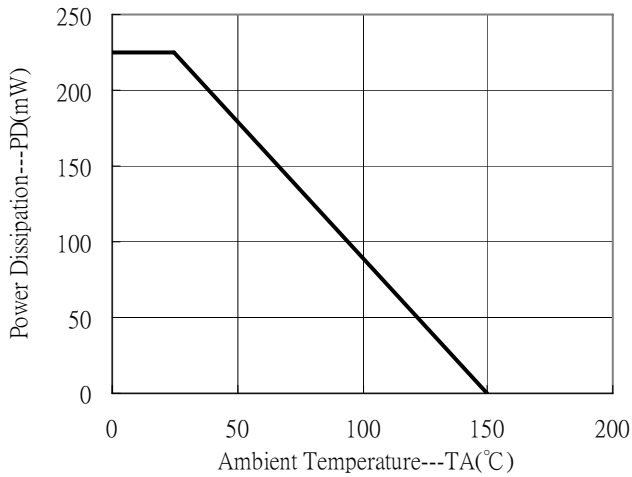
Capacitance vs Reverse-biased Voltage



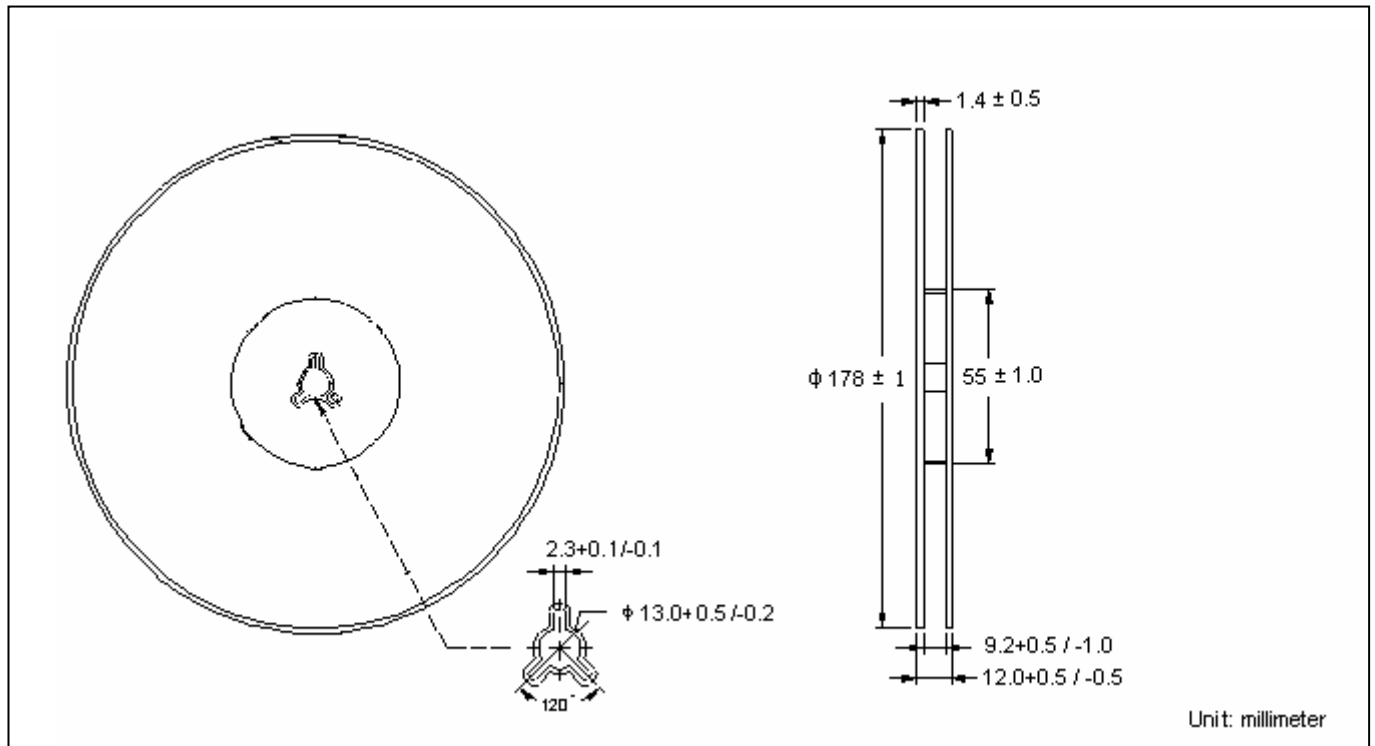
Cutoff Frequency vs Collector Current



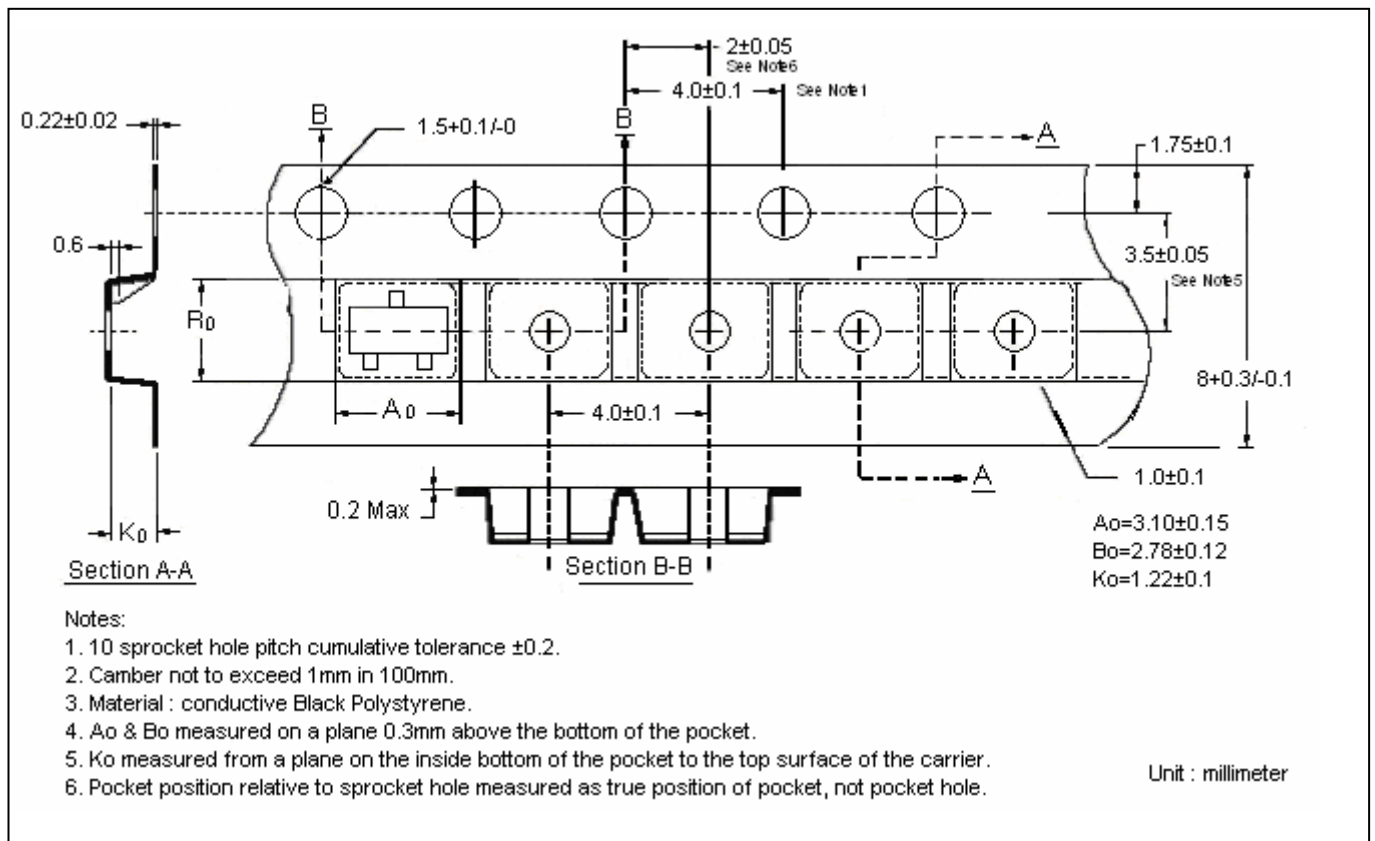
Power Derating Curve



### Reel Dimension



### Carrier Tape Dimension

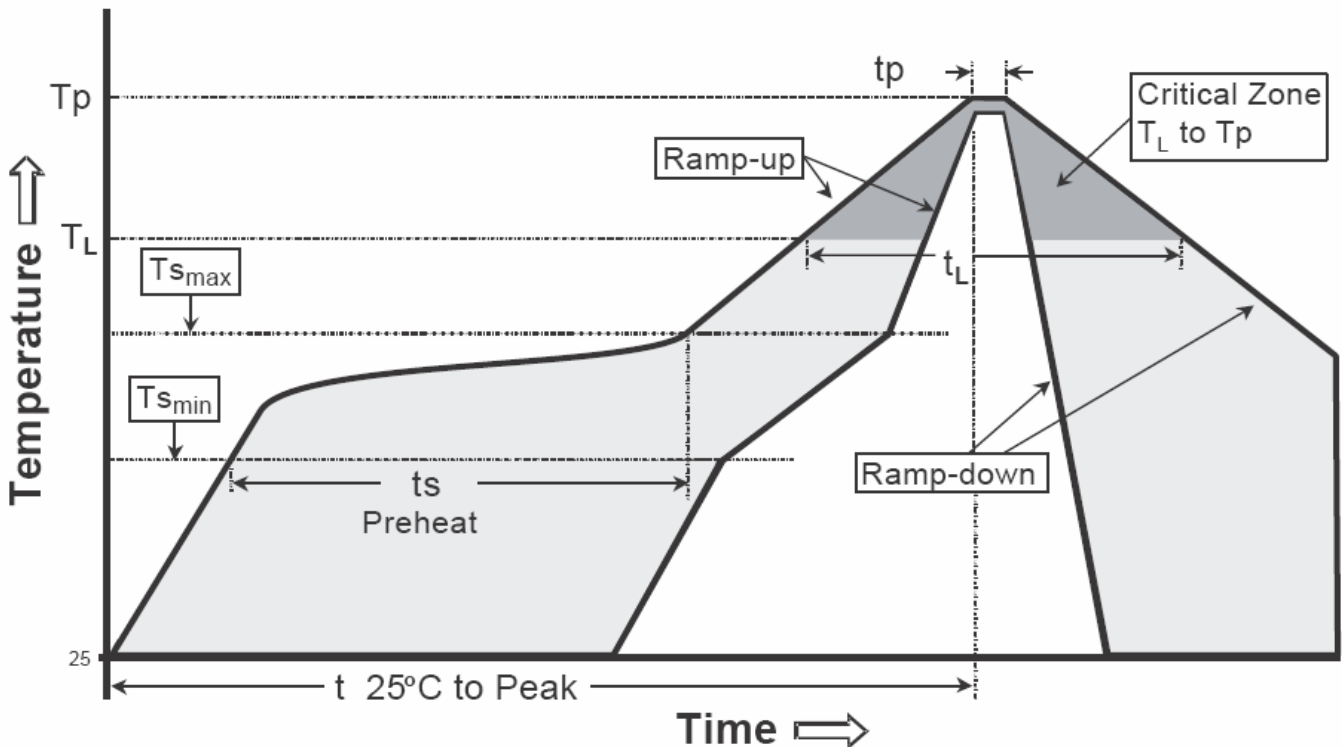




**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

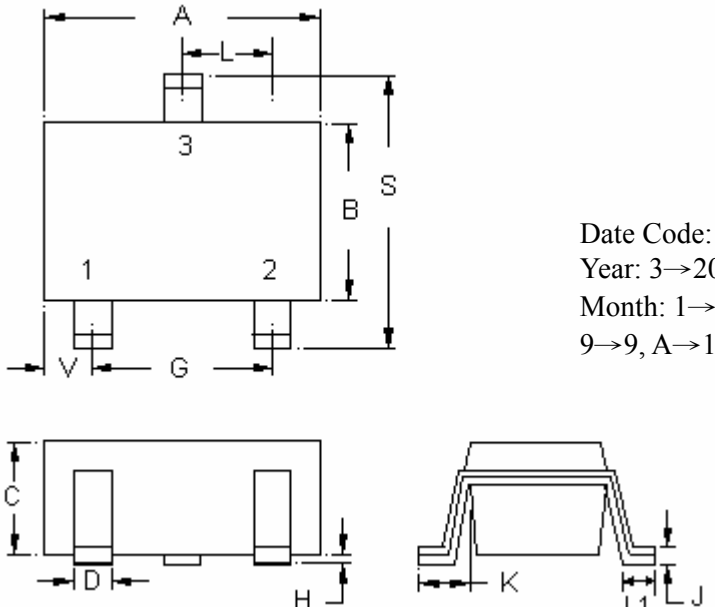
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

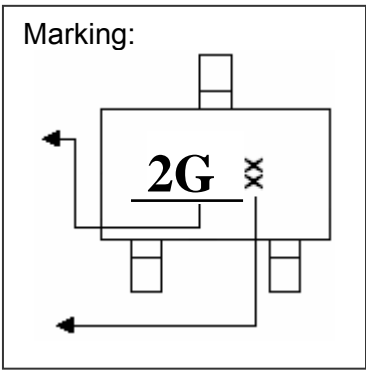
Note : All temperatures refer to topside of the package, measured on the package body surface.

**SOT-23 Dimension**



The diagram shows three views of the SOT-23 package: a top view with dimensions A, L, B, S, 1, 2, 3, V, and G; a side view with dimensions C, D, H, and J; and a perspective view with dimensions K, L1, and L2. The top view labels 1, 2, and 3 correspond to the pin locations.

**Marking:**



The marking diagram shows a rectangular package with three pins. The top pin is labeled '2G' with a small 'x' to its right. Arrows point to the top and bottom pins.

**Product Code**

**Date Code: Year+Month**  
 Year: 3→2003, 4→2004  
 Month: 1→1, 2→2, . . .  
 9→9, A→10, B→11, C→12

**3-Lead SOT-23 Plastic Surface Mounted Package**  
 CYStek Package Code: N3

**Style : Pin 1.Base 2.Emitter 3.Collector**

\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0032	0.0079	0.08	0.20
B	0.0472	0.0669	1.20	1.70	K	0.0118	0.0266	0.30	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0000	0.0040	0.00	0.10	L1	0.0118	0.0197	0.30	0.50

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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