

DESCRIPTION

The M37920S4CGP is a single-chip microcomputers designed with high-performance CMOS silicon gate technology. These are housed in 100-pin plastic molded QFP. This microcomputer supports the 7900 Series instruction set, which are enhanced and expanded instruction set and are upper-compatible with the 7700/7751 Series instruction set.

The CPU of this microcomputer is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. Also, the bus interface unit of this microcomputer enhance the memory access efficiency to execute instructions fast. This microcomputer include the 4-channel DMA controller and the DRAM controller with enhanced fast page mode. Therefore, this microcomputer are suitable for office, business, and industrial equipment controller that require fast processing of large data.

DISTINCTIVE FEATURES

<Microcomputer mode>

- Number of basic machine instructions 203
- Memory
 - RAM 2048 bytes
 - ROM External

• Instruction execution time

The fastest instruction at 20 MHz frequency 50 ns

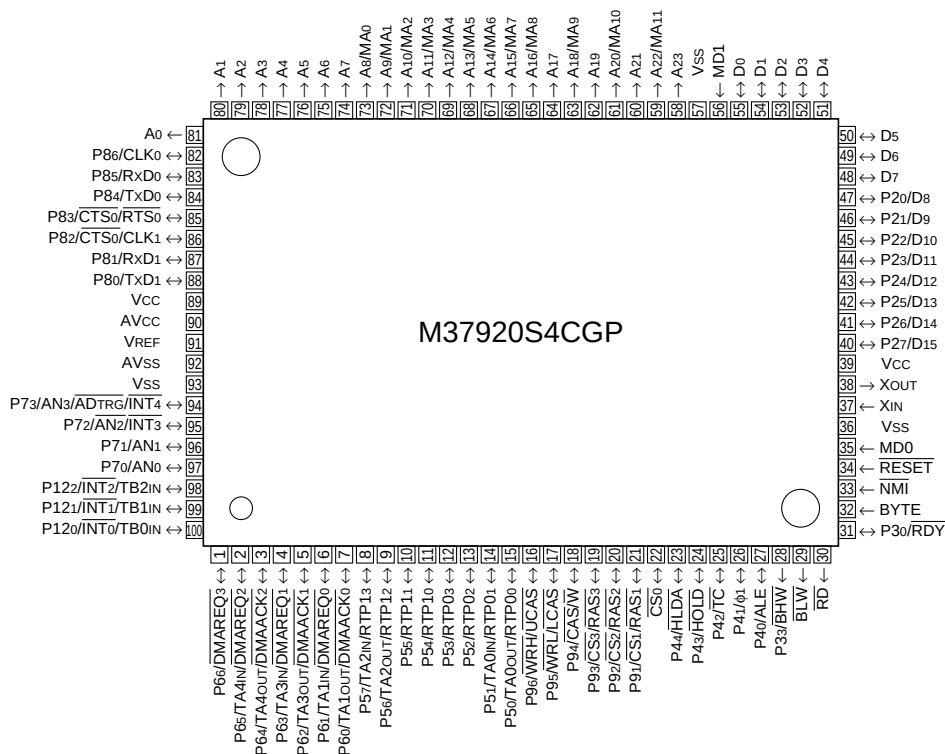
- Single power supply 5 V $\pm$ 0.5 V
- Interrupts 6 external sources, 17 internal sources, 7 levels
- Multi-functional 16-bit timer 5 + 3
- Serial I/O (UART or Clock synchronous) 2
- 10-bit A-D converter 4-channel inputs
- DMA controller 4-channels
- DRAM controller
- Real-time output
 - 4 bits $\times$ 2 channels, or 6 bits $\times$ 1 channel + 2 bits $\times$ 1 channel
- 12-bit watchdog timer
- Programmable input/output (ports P2–P9, P12) 49

APPLICATION

Telecommunications equipment such as copiers, printers, typewriters, facsimiles, optical disk drives, HDD, mobile radio communication equipment, ISDN terminals

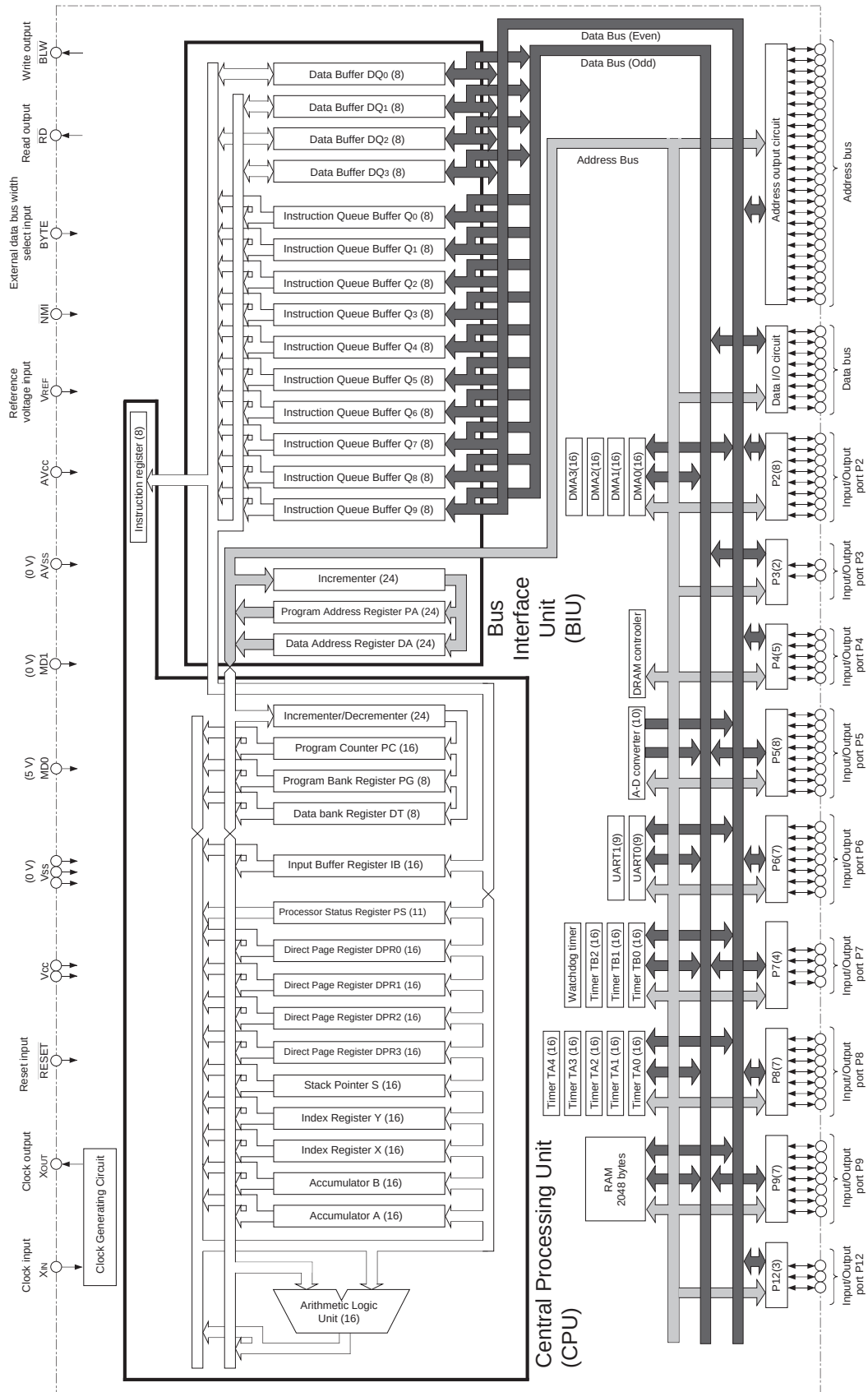
Control devices for office automation equipment such as personal computers

M37920S4CGP PIN CONFIGURATION (TOP VIEW)



Outline 100P6S-A

BLOCK DIAGRAM



PRELIMINARY
 Notice: This is not a final specification.
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FUNCTIONS (Microcomputer mode)

Parameter		Functions
Number of basic machine instructions		203
Instruction execution time		50 ns (the fastest instruction at $f(X_{IN}) = 20$ MHz)
External clock input frequency $f(X_{IN})$		20 MHz (Max.)
Memory size	ROM	External
	RAM	2048 bytes
Programmable input/output ports	P2, P5	8-bit X 2
	P3	2-bit X 1
	P4	5-bit X 1
	P6, P8	7-bit X 2
	P7	4-bit X 1
	P9	6-bit X 1
	P12	3-bit X 1
Multi-functional timers	TA0–TA4	16-bit X 5
	TB0–TB2	16-bit X 3
Serial I/O	UART0 and UART1	(UART or Clock synchronous serial I/O) X 2
A-D converter		10-bit successive approximation method X 1 (4 channels)
Watchdog timer		12-bit X 1
DMA controller		4 channels Maximum transfer rate 20 Mbytes/sec. (at $f(X_{IN}) = 20$ MHz, 0 wait, 1-bus cycle transfer) 10 Mbytes/sec. (at $f(X_{IN}) = 20$ MHz, 0 wait, 2-bus cycles transfer)
DRAM controller		1 channel Supports fast page access mode. Incorporates 8-bit refresh timer. Supports CAS before RAS refresh method or self refresh method.
Chip-select wait control		Chip select area X 4 ($\overline{CS_0}$ – $\overline{CS_3}$). A wait number and bus width can be set for each chip select area.
Real-time output		4 bits X 2 channels; or 6 bits X 1 channel + 2 bits X 1 channel
Interrupts		6 external types, 17 internal types. Each interrupt except $\overline{NMI}$ can be set to a priority level within the range of 0–7 by software.
Clock generating circuit		Built-in (externally connected to a ceramic resonator or quartz crystal resonator).
Power supply voltage		5 V ± 10 %
Power dissipation		135 mW (at $f(X_{IN}) = 20$ MHz, typ.)
Ports' input/output characteristics	Input/Output withstand voltage	5 V
	Output current	5 mA
Memory expansion		Up to 16 Mbytes. Note that bank FF16 is a reserved area.
Operating temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		100-pin plastic molded QFP

PIN DESCRIPTION (Microcomputer mode)

Pin	Name	Input/ Output	Functions
Vcc, Vss	Power supply input	—	Apply 5 V $\pm$ 10 % to Vcc, and 0 V to Vss.
MD0	MD0	Input	This pin controls the processor mode. Connect this pin to Vcc.
MD1	MD1	Input	Connect this pin to Vss.
$\overline{\text{RESET}}$	Reset input	Input	The microcomputer is reset when "L" level is applies to this pin.
XIN	Clock input	Input	These are input and output pins of the internal clock generating circuit. Connect a ceramic or quartz- crystal resonator between the XIN and XOUT pins. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
BYTE	External data bus width select input	Input	This pin determines whether the external data bus has an 8-bit width or 16-bit width for the memory expansion mode or microprocessor mode. The width is 16 bits when "L" signal is input, and 8 bits when "H" signal is input.
AVcc, AVss	Analog power supply input	—	Power supply input pin for the A-D converter. Connect AVcc to Vcc, and AVss to Vss externally.
VREF	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
A0–A7	Low-order address	Output	The low-order 8 bits of address (A0–A7) are output.
A8–A15/ MA0–MA7	Middle-order address/ DRAM address	Output	The middle-order 8 bits of address (A8–A15) are input/output. While DRAM space is accessed, multiplexed address (MA0–MA7) is output.
A16–A23/ MA8–MA11	High-order address/ DRAM address	Output	The high-order 8 bits of address (A16–A23) are output. While DRAM space is accessed, multiplexed address (MA8–MA11) is output.
D0–D7	Low-order data	I/O	The low-order 8 bits of data (D0–D7) are input/output.
P20/D8– P27/D15	I/O port P2/ High-order data	I/O	■ When 8-bit external data bus is used (BYTE = "H" level) Port P2 is an 8-bit I/O port. ■ When 16-bit external data bus is used (BYTE = "L" level) The high-order 8 bits (D8–D15) are input/output.
P30/ $\overline{\text{RDY}}$, $\overline{\text{RD}}$, BLW, P33/BHW	Memory control signal I/O	Input Output Output Output	While the input level at pin $\overline{\text{RDY}}$ is "L", the microcomputer is placed in the ready state. While pin $\overline{\text{RD}}$ is at "L" level, the microcomputer reads out data and instruction codes. Also, pin $\overline{\text{RDY}}$ can function as a programmable I/O port pin (P30) by software. ■ When 8-bit external data bus is used (BYTE = "H" level) While pin BLW is at "L" level, the microcomputer writes data. ■ When 16-bit external data bus is used (BYTE = "L" level) While pin BLW is at "L" level, the microcomputer writes data into an even-numbered address. While pin BHW is at "L" level, the microcomputer writes data into an odd-numbered address.
P40/ALE, P41/ ϕ 1, P42/TC, P43/HOLD, P44/HLDA	I/O port P4	Output Output I/O Input Output	Signal ALE is used to latch an address. ϕ 1 has the same period as internal clock ϕ . Pin P42 functions as a programmable I/O port pin. While the input level at pin HOLD is at "L" level, the microcomputer is placed in the hold state. Signal HLDA is used to inform the external that the microcomputer enters the hold state. By software, pin ALE, clock ϕ 1 output pin, and pins HOLD, HLDA function as programmable I/O port pins (P40, P41, P43, P44). Pin P42 also functions as pin TC.
P50–P57	I/O port P5	I/O	Port P5 is an 8-bit I/O port. These pins also function as I/O pins for timers A0, A2, and pulse output pins for the real-time output.
P60–P66	I/O port P6	I/O	Port P6 is a 7-bit I/O port. These pins also function as I/O pins for timers A1, A3, A4, input pins for DMA requests, and output pins for DMA acknowledge signals.

PRELIMINARY
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Pin	Name	Input/ Output	Functions
P70–P73	I/O port P7	I/O	Port P7 is a 4-bit I/O port. P72 and P73 also function as input pins for $\overline{\text{INT}}_3$ and $\overline{\text{INT}}_4$. According to the software setting, these pins also function as input pins for the A-D converter.
P80–P86	I/O port P8	I/O	Port P8 is a 7-bit I/O port. These pins also function as I/O pins for UART0, UART1.
$\overline{\text{CS}}_0$	Chip-select output	Output	This is an output pin for $\overline{\text{CS}}_0$.
P91–P96	I/O port P9	I/O	Port P9 is a 6-bit I/O port. According to the software setting, P91–P93 also function as chip select output pins. While DRAM space is selected, P94–P96 function as output pins for DRAM control signals.
P120–P122	I/O port P12	I/O	Port P12 is a 3-bit I/O port. These pins also function as input pins for $\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$, $\overline{\text{INT}}_2$. According to software setting, these pins also function as input pins for timers B0–B2.
$\overline{\text{NMI}}$	Non-maskable interrupt	Input	This pin is for a non-maskable interrupt.

BASIC FUNCTION BLOCKS

The M37920S4CGP is the same functions as the M37920F8CGP except for the following.

Therefore, refer to the datasheet of the M37920F8CGP.

- The M37920S4CGP does not include the internal flash memory.
- The M37920S4CGP operates only in the microprocessor mode.
- The M37920S4CGP does not have the flash memory control register (address 9E₁₆).
- Some of programmable I/O ports of the M37920S4CGP differ from those of the M37920FGCGP.

MEMORY

Figure 1 shows the memory map.

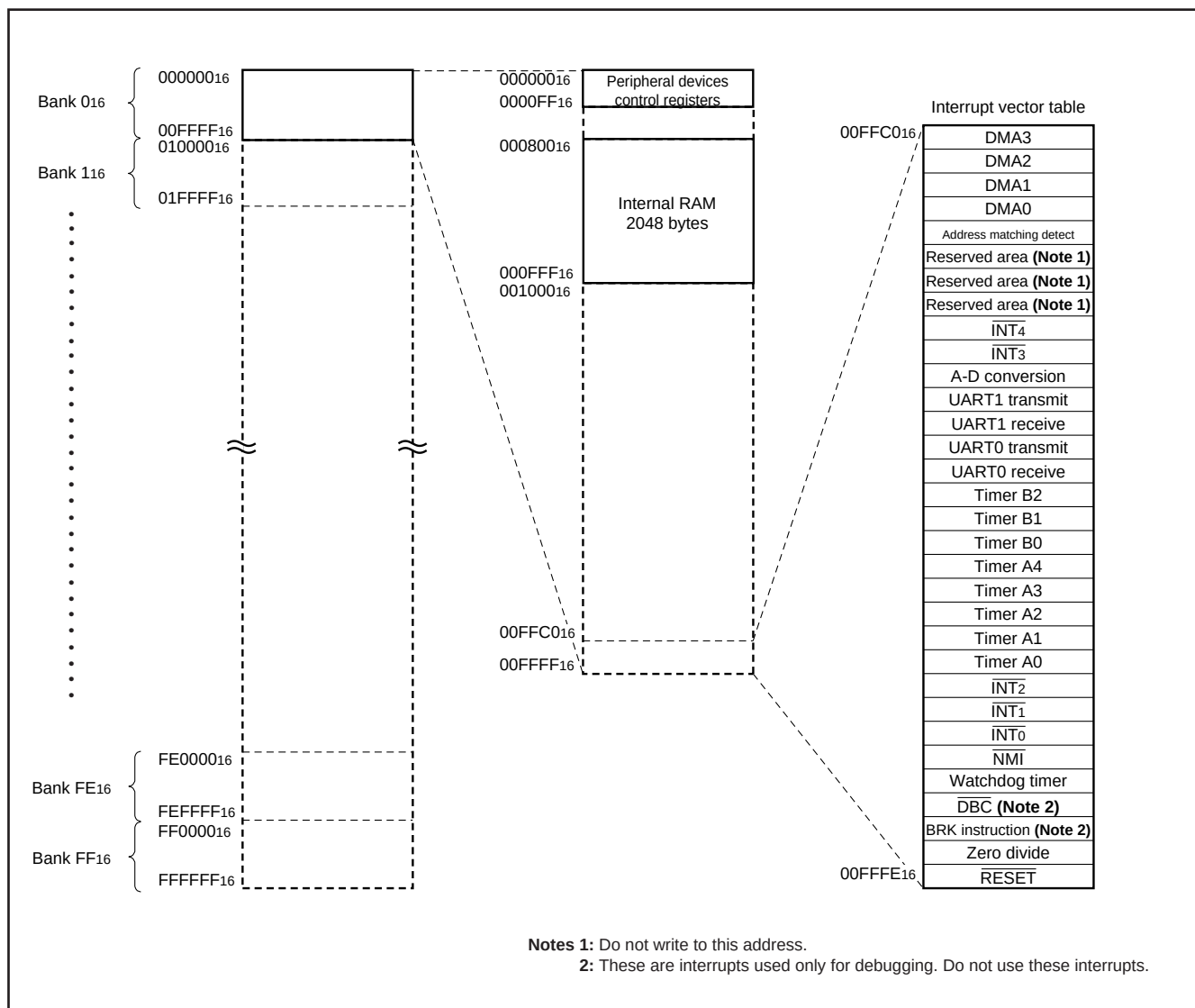


Fig. 1 Memory map

PRELIMINARY
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Address (Hexadecimal notation)

000000 ₁₆	Reserved area (Note 1)
000001 ₁₆	Reserved area (Note 1)
000002 ₁₆	[Port P0 register] (Note 2)
000003 ₁₆	[Port P1 register] (Note 2)
000004 ₁₆	[Port P0 direction register] (Note 2)
000005 ₁₆	[Port P1 direction register] (Note 2)
000006 ₁₆	Port P2 register
000007 ₁₆	Port P3 register
000008 ₁₆	Port P2 direction register
000009 ₁₆	Port P3 direction register
00000A ₁₆	Port P4 register
00000B ₁₆	Port P5 register
00000C ₁₆	Port P4 direction register
00000D ₁₆	Port P5 direction register
00000E ₁₆	Port P6 register
00000F ₁₆	Port P7 register
000010 ₁₆	Port P6 direction register
000011 ₁₆	Port P7 direction register
000012 ₁₆	Port P8 register
000013 ₁₆	Port P9 register
000014 ₁₆	Port P8 direction register
000015 ₁₆	Port P9 direction register
000016 ₁₆	[Port P10 register] (Note 2)
000017 ₁₆	[Port P11 register] (Note 2)
000018 ₁₆	[Port P10 direction register] (Note 2)
000019 ₁₆	[Port P11 direction register] (Note 2)
00001A ₁₆	Port P12 register
00001B ₁₆	
00001C ₁₆	Port P12 direction register
00001D ₁₆	
00001E ₁₆	A-D control register 0
00001F ₁₆	A-D control register 1
000020 ₁₆	A-D register 0
000021 ₁₆	
000022 ₁₆	A-D register 1
000023 ₁₆	
000024 ₁₆	A-D register 2
000025 ₁₆	
000026 ₁₆	A-D register 3
000027 ₁₆	
000028 ₁₆	
000029 ₁₆	
00002A ₁₆	
00002B ₁₆	
00002C ₁₆	
00002D ₁₆	
00002E ₁₆	
00002F ₁₆	
000030 ₁₆	UART0 transmit/receive mode register
000031 ₁₆	UART0 baud rate register (BRG0)
000032 ₁₆	UART0 transmit buffer register
000033 ₁₆	
000034 ₁₆	UART0 transmit/receive control register 0
000035 ₁₆	UART0 transmit/receive control register 1
000036 ₁₆	
000037 ₁₆	UART0 receive buffer register
000038 ₁₆	
000039 ₁₆	UART1 transmit/receive mode register
00003A ₁₆	UART1 baud rate register (BRG1)
00003B ₁₆	UART1 transmit buffer register
00003C ₁₆	
00003D ₁₆	UART1 transmit/receive control register 0
00003E ₁₆	UART1 transmit/receive control register 1
00003F ₁₆	UART1 receive buffer register

Address (Hexadecimal notation)

000040 ₁₆	Count start register
000041 ₁₆	
000042 ₁₆	One-shot start register
000043 ₁₆	
000044 ₁₆	Up-down register
000045 ₁₆	Timer A clock division select register
000046 ₁₆	Timer A0 register
000047 ₁₆	
000048 ₁₆	Timer A1 register
000049 ₁₆	
00004A ₁₆	Timer A2 register
00004B ₁₆	
00004C ₁₆	Timer A3 register
00004D ₁₆	
00004E ₁₆	Timer A4 register
00004F ₁₆	
000050 ₁₆	Timer B0 register
000051 ₁₆	
000052 ₁₆	Timer B1 register
000053 ₁₆	
000054 ₁₆	Timer B2 register
000055 ₁₆	
000056 ₁₆	Timer A0 mode register
000057 ₁₆	Timer A1 mode register
000058 ₁₆	Timer A2 mode register
000059 ₁₆	Timer A3 mode register
00005A ₁₆	Timer A4 mode register
00005B ₁₆	Timer B0 mode register
00005C ₁₆	Timer B1 mode register
00005D ₁₆	Timer B2 mode register
00005E ₁₆	Processor mode register 0
00005F ₁₆	Processor mode register 1
000060 ₁₆	Watchdog timer register
000061 ₁₆	Watchdog timer frequency select register
000062 ₁₆	Particular function select register 0
000063 ₁₆	Particular function select register 1
000064 ₁₆	Particular function select register 2
000065 ₁₆	Reserved area (Note 1)
000066 ₁₆	Debug control register 0
000067 ₁₆	Debug control register 1
000068 ₁₆	
000069 ₁₆	Address comparison register 0
00006A ₁₆	
00006B ₁₆	
00006C ₁₆	Address comparison register 1
00006D ₁₆	
00006E ₁₆	INT3 interrupt control register
00006F ₁₆	INT4 interrupt control register
000070 ₁₆	A-D conversion interrupt control register
000071 ₁₆	UART0 transmit interrupt control register
000072 ₁₆	UART0 receive interrupt control register
000073 ₁₆	UART1 transmit interrupt control register
000074 ₁₆	UART1 receive interrupt control register
000075 ₁₆	Timer A0 interrupt control register
000076 ₁₆	Timer A1 interrupt control register
000077 ₁₆	Timer A2 interrupt control register
000078 ₁₆	Timer A3 interrupt control register
000079 ₁₆	Timer A4 interrupt control register
00007A ₁₆	Timer B0 interrupt control register
00007B ₁₆	Timer B1 interrupt control register
00007C ₁₆	Timer B2 interrupt control register
00007D ₁₆	INT0 interrupt control register
00007E ₁₆	INT1 interrupt control register
00007F ₁₆	INT2 interrupt control register

Notes 1: Do not read/write to this address.

2: These registers are used in the bus fixation of the power saving function. For details, refer to the section on the power saving function of the M37920F8CGP datasheet.

Fig. 2 Location of peripheral devices' control registers (1)

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Address (Hexadecimal notation)

000080 ₁₆	CS ₀ control register L
000081 ₁₆	CS ₀ control register H
000082 ₁₆	CS ₁ control register L
000083 ₁₆	CS ₁ control register H
000084 ₁₆	CS ₂ control register L
000085 ₁₆	CS ₂ control register H
000086 ₁₆	CS ₃ control register L
000087 ₁₆	CS ₃ control register H
000088 ₁₆	
000089 ₁₆	
00008A ₁₆	Area CS ₀ start address register
00008B ₁₆	
00008C ₁₆	Area CS ₁ start address register
00008D ₁₆	
00008E ₁₆	Area CS ₂ start address register
00008F ₁₆	
000090 ₁₆	Area CS ₃ start address register
000091 ₁₆	
000092 ₁₆	
000093 ₁₆	
000094 ₁₆	
000095 ₁₆	
000096 ₁₆	
000097 ₁₆	
000098 ₁₆	
000099 ₁₆	
00009A ₁₆	
00009B ₁₆	
00009C ₁₆	Reserved area (Note 1)
00009D ₁₆	Reserved area (Note 1)
00009E ₁₆	Reserved area (Note 1)
00009F ₁₆	
0000A0 ₁₆	Real-time output control register
0000A1 ₁₆	
0000A2 ₁₆	Pulse output data register 0
0000A3 ₁₆	
0000A4 ₁₆	Pulse output data register 1
0000A5 ₁₆	
0000A6 ₁₆	Reserved area (Note 1)
0000A7 ₁₆	
0000A8 ₁₆	DRAM control register
0000A9 ₁₆	Refresh timer
0000AA ₁₆	
0000AB ₁₆	
0000AC ₁₆	CTS/RTS separate select register
0000AD ₁₆	
0000AE ₁₆	
0000AF ₁₆	
0000B0 ₁₆	DMAC control register L
0000B1 ₁₆	DMAC control register H
0000B2 ₁₆	DMA0 interrupt control register
0000B3 ₁₆	DMA1 interrupt control register
0000B4 ₁₆	DMA2 interrupt control register
0000B5 ₁₆	DMA3 interrupt control register
0000B6 ₁₆	
0000B7 ₁₆	
0000B8 ₁₆	
0000B9 ₁₆	
0000BA ₁₆	
0000BB ₁₆	
0000BC ₁₆	Reserved area (Note 1)
0000BD ₁₆	Reserved area (Note 1)
0000BE ₁₆	Reserved area (Note 1)
0000BF ₁₆	Reserved area (Note 1)

Address (Hexadecimal notation)

0000C0 ₁₆	Source address register 0 L
0000C1 ₁₆	Source address register 0 M
0000C2 ₁₆	Source address register 0 H
0000C3 ₁₆	
0000C4 ₁₆	Destination address register 0 L
0000C5 ₁₆	Destination address register 0 M
0000C6 ₁₆	Destination address register 0 H
0000C7 ₁₆	
0000C8 ₁₆	Transfer counter register 0 L
0000C9 ₁₆	Transfer counter register 0 M
0000CA ₁₆	Transfer counter register 0 H
0000CB ₁₆	
0000CC ₁₆	DMA0 mode register L
0000CD ₁₆	DMA0 mode register H
0000CE ₁₆	DMA0 control register
0000CF ₁₆	
0000D0 ₁₆	Source address register 1 L
0000D1 ₁₆	Source address register 1 M
0000D2 ₁₆	Source address register 1 H
0000D3 ₁₆	
0000D4 ₁₆	Destination address register 1 L
0000D5 ₁₆	Destination address register 1 M
0000D6 ₁₆	Destination address register 1 H
0000D7 ₁₆	
0000D8 ₁₆	Transfer counter register 1 L
0000D9 ₁₆	Transfer counter register 1 M
0000DA ₁₆	Transfer counter register 1 H
0000DB ₁₆	
0000DC ₁₆	DMA1 mode register L
0000DD ₁₆	DMA1 mode register H
0000DE ₁₆	DMA1 control register
0000DF ₁₆	
0000E0 ₁₆	Source address register 2 L
0000E1 ₁₆	Source address register 2 M
0000E2 ₁₆	Source address register 2 H
0000E3 ₁₆	
0000E4 ₁₆	Destination address register 2 L
0000E5 ₁₆	Destination address register 2 M
0000E6 ₁₆	Destination address register 2 H
0000E7 ₁₆	
0000E8 ₁₆	Transfer counter register 2 L
0000E9 ₁₆	Transfer counter register 2 M
0000EA ₁₆	Transfer counter register 2 H
0000EB ₁₆	
0000EC ₁₆	DMA2 mode register L
0000ED ₁₆	DMA2 mode register H
0000EE ₁₆	DMA2 control register
0000EF ₁₆	
0000F0 ₁₆	Source address register 3 L
0000F1 ₁₆	Source address register 3 M
0000F2 ₁₆	Source address register 3 H
0000F3 ₁₆	
0000F4 ₁₆	Destination address register 3 L
0000F5 ₁₆	Destination address register 3 M
0000F6 ₁₆	Destination address register 3 H
0000F7 ₁₆	
0000F8 ₁₆	Transfer counter register 3 L
0000F9 ₁₆	Transfer counter register 3 M
0000FA ₁₆	Transfer counter register 3 H
0000FB ₁₆	
0000FC ₁₆	DMA3 mode register L
0000FD ₁₆	DMA3 mode register H
0000FE ₁₆	DMA3 control register
0000FF ₁₆	

Note 1: Do not read/write to this address.

Fig. 3 Location of peripheral devices' control registers (2)

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Processor mode

The M37920S4CGP operates only in the microprocessor mode exclusive for the external ROM. Be sure to fix the level at pin MD0 to Vcc and the level at pin MD1 to Vss. Also, be sure to fix bits 1, 0 at address 5E16 (the processor mode register 0) to "1" and "0", respectively.

Table 1. Relationship between pins MD0, MD1 and processor mode

Pin MD0	Pin MD1	Processor mode
Vcc level (5 V)	Vss level (5 V)	After reset, the microcomputer starts its operation in the microprocessor mode. (Be sure to pin MD0 to Vcc level.)

Microprocessor mode

When the microcomputer starts its operation after reset with the level at pin MD0 = Vcc level (5 V), the microcomputer is placed in the microprocessor mode.

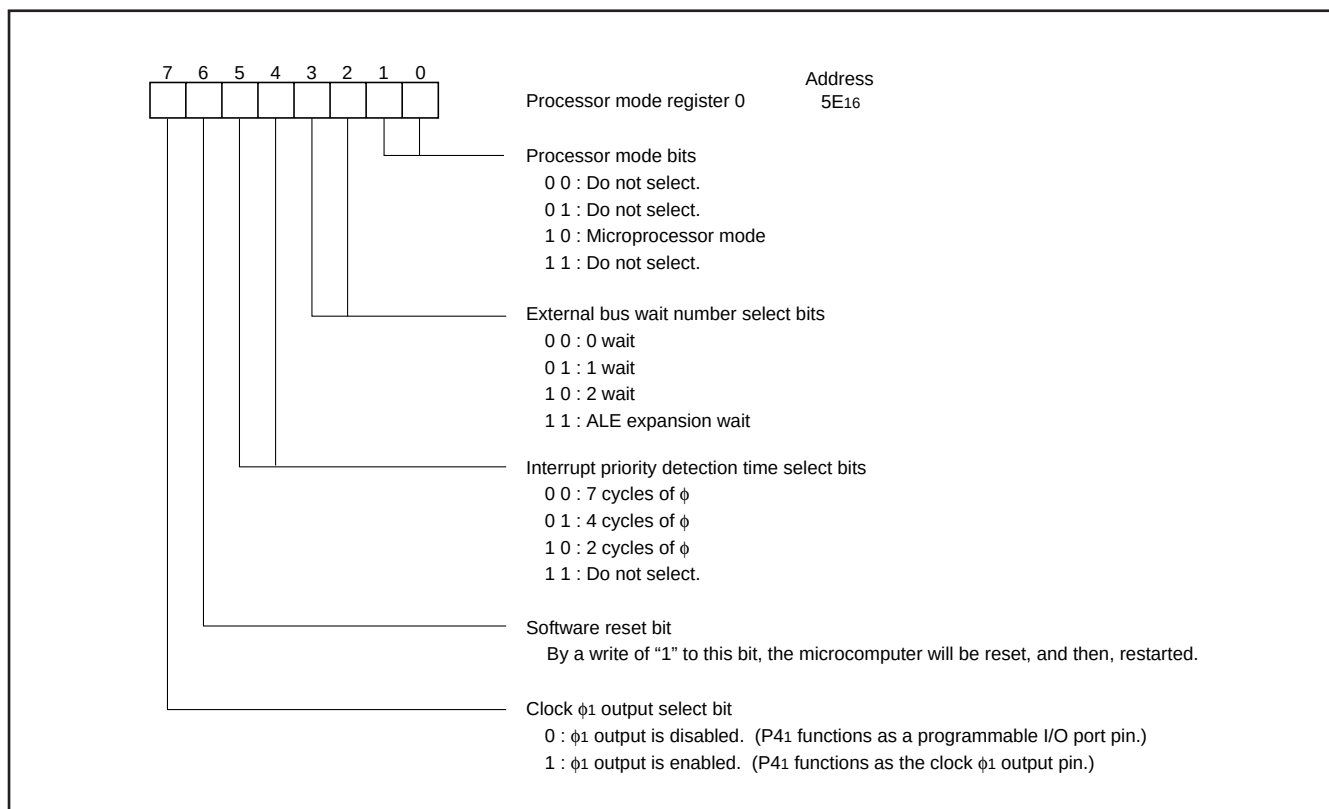


Fig. 4 Processor mode register 0's bit configuration

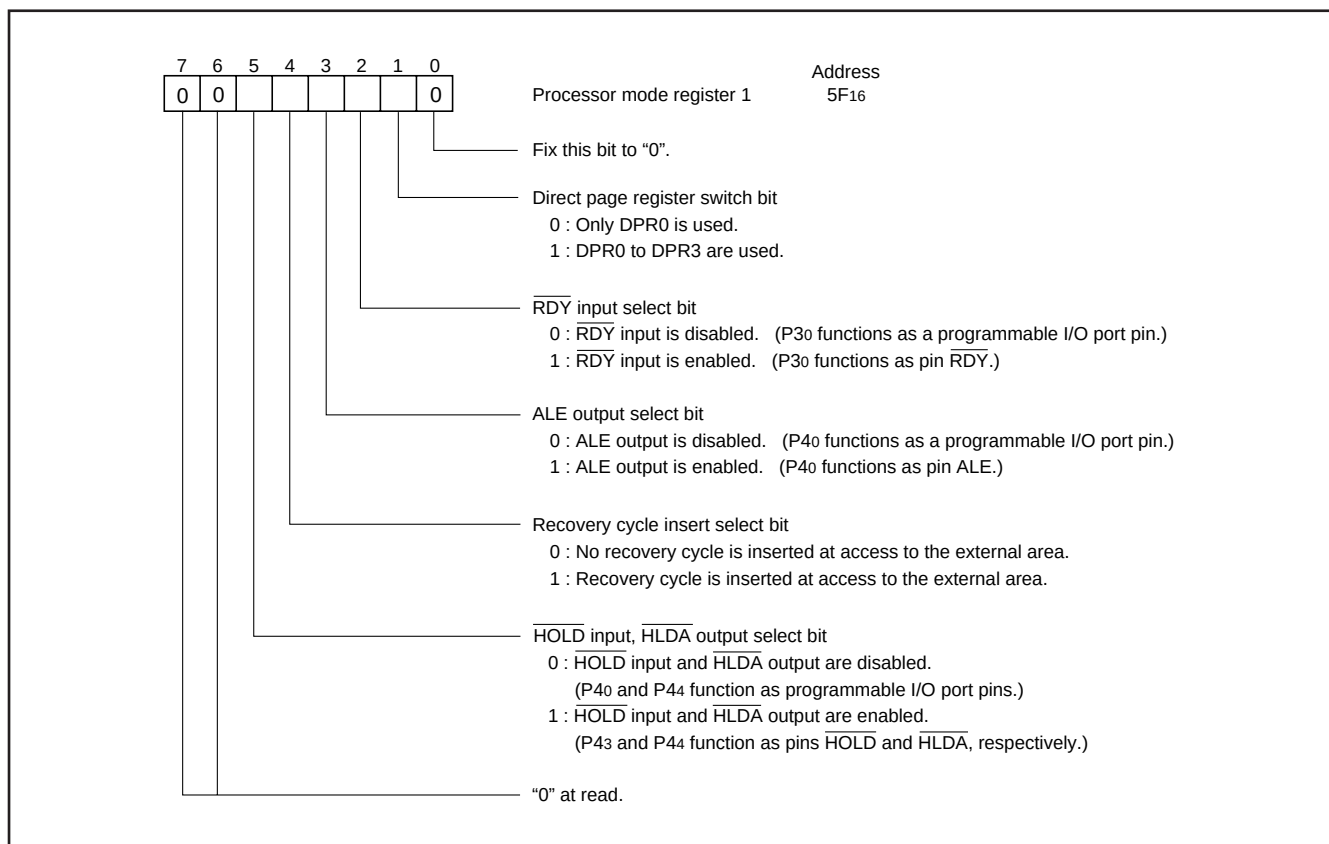


Fig. 5 Processor mode register 1's bit configuration

PRELIMINARY
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Address		Address																				
Port P0 direction register	(04 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Processor mode register 0	(5E ₁₆)... <table border="1"><tr><td>Note 2</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Note 2</td><td>0</td></tr></table>	Note 2	0	0	0	1	0	Note 2	0			
00 ₁₆																						
Note 2	0	0	0	1	0	Note 2	0															
Port P1 direction register	(05 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Processor mode register 1	(5F ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>(Note 2)</td><td>0</td><td>0</td></tr></table>	0	0	(Note 2)	0	0						
00 ₁₆																						
0	0	(Note 2)	0	0																		
Port P2 direction register	(08 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Watchdog timer	(60 ₁₆)... <table border="1"><tr><td colspan="8">FFF₁₆</td></tr></table>	FFF ₁₆										
00 ₁₆																						
FFF ₁₆																						
Port P3 direction register	(09 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0	Watchdog timer frequency select register	(61 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td></tr></table>	X	X	X	X	X	X	X	0			
X	X	X	X	0	0	0	0															
X	X	X	X	X	X	X	0															
Port P4 direction register	(0C ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	0	0	0	0	0	Particular function select register 0	(62 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td></tr></table>	X	X	X	X	X	X	0	0			
X	X	X	0	0	0	0	0															
X	X	X	X	X	X	0	0															
Port P5 direction register	(0D ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Particular function select register 1	(63 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>(Note 3)</td><td></td></tr></table>	X	X	X	X	0	0	(Note 3)				
00 ₁₆																						
X	X	X	X	0	0	(Note 3)																
Port P6 direction register	(10 ₁₆)... <table border="1"><tr><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	0	0	0	0	0	0	0	Debug control register 0	(66 ₁₆)... <table border="1"><tr><td>1</td><td>(Note 3)</td><td colspan="6"></td></tr></table>	1	(Note 3)									
X	0	0	0	0	0	0	0															
1	(Note 3)																					
Port P7 direction register	(11 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0	Debug control register 1	(67 ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>0</td><td>0</td><td>0</td><td>Note 3</td></tr></table>	0	0	0	Note 3	0	0	0	Note 3			
X	X	X	X	0	0	0	0															
0	0	0	Note 3	0	0	0	Note 3															
Port P8 direction register	(14 ₁₆)... <table border="1"><tr><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	0	0	0	0	0	0	0	INT ₃ interrupt control register	(6E ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
X	0	0	0	0	0	0	0															
X	X	X	X	0	0	0	0															
Port P9 direction register	(15 ₁₆)... <table border="1"><tr><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	0	0	0	0	0	0	0	INT ₄ interrupt control register	(6F ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
X	0	0	0	0	0	0	0															
X	X	X	X	0	0	0	0															
Port P10 direction register	(18 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								A-D conversion interrupt control register	(70 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>?</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	?	0	0	0			
00 ₁₆																						
X	X	X	X	?	0	0	0															
Port P11 direction register	(19 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								UART 0 transmit interrupt control register	(71 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
00 ₁₆																						
X	X	X	X	0	0	0	0															
Port P12 direction register	(1C ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	X	0	0	0	UART 0 receive interrupt control register	(72 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
X	X	X	X	X	0	0	0															
X	X	X	X	0	0	0	0															
A-D control register 0	(1E ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>?</td><td>?</td><td>?</td></tr></table>	0	0	0	0	0	?	?	?	UART 1 transmit interrupt control register	(73 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
0	0	0	0	0	?	?	?															
X	X	X	X	0	0	0	0															
A-D control register 1	(1F ₁₆)... <table border="1"><tr><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr></table>	X	0	0	0	0	0	0	1	UART 1 receive interrupt control register	(74 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
X	0	0	0	0	0	0	1															
X	X	X	X	0	0	0	0															
UART 0 Transmit/Receive mode register	(30 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Timer A0 interrupt control register	(75 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
00 ₁₆																						
X	X	X	X	0	0	0	0															
UART 1 Transmit/Receive mode register	(38 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Timer A1 interrupt control register	(76 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
00 ₁₆																						
X	X	X	X	0	0	0	0															
UART 0 Transmit/Receive control register 0	(34 ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	1	0	0	0	Timer A2 interrupt control register	(77 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
0	0	0	0	1	0	0	0															
X	X	X	X	0	0	0	0															
UART 1 Transmit/Receive control register 0	(3C ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	1	0	0	0	Timer A3 interrupt control register	(78 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
0	0	0	0	1	0	0	0															
X	X	X	X	0	0	0	0															
UART 0 Transmit/Receive control register 1	(35 ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table>	0	0	0	0	0	0	1	0	Timer A4 interrupt control register	(79 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
0	0	0	0	0	0	1	0															
X	X	X	X	0	0	0	0															
UART 1 Transmit/Receive control register 1	(3D ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table>	0	0	0	0	0	0	1	0	Timer B0 interrupt control register	(7A ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
0	0	0	0	0	0	1	0															
X	X	X	X	0	0	0	0															
Count start register	(40 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Timer B1 interrupt control register	(7B ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
00 ₁₆																						
X	X	X	X	0	0	0	0															
One-shot start register	(42 ₁₆)... <table border="1"><tr><td>0</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	X	X	0	0	0	0	0	Timer B2 interrupt control register	(7C ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0			
0	X	X	0	0	0	0	0															
X	X	X	X	0	0	0	0															
Up-down register	(44 ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	INT ₀ interrupt control register	(7D ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	0	0	0	0	0	0			
0	0	0	0	0	0	0	0															
X	X	0	0	0	0	0	0															
Timer A clock division select register	(45 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td></tr></table>	X	X	X	X	X	X	0	0	INT ₁ interrupt control register	(7E ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	0	0	0	0	0	0			
X	X	X	X	X	X	0	0															
X	X	0	0	0	0	0	0															
Timer A0 mode register	(56 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								INT ₂ interrupt control register	(7F ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	0	0	0	0	0	0			
00 ₁₆																						
X	X	0	0	0	0	0	0															
Timer A1 mode register	(57 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Processor status register PS	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>?</td><td>?</td><td>0</td><td>0</td><td>0</td><td>1</td><td>?</td><td>?</td></tr></table>	0	0	0	?	?	0	0	0	1	?	?
00 ₁₆																						
0	0	0	?	?	0	0	0	1	?	?												
Timer A2 mode register	(58 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Program bank register PG	<table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆										
00 ₁₆																						
00 ₁₆																						
Timer A3 mode register	(59 ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Program counter PC _H	<table border="1"><tr><td colspan="8">Contents at address FFFF₁₆</td></tr></table>	Contents at address FFFF ₁₆										
00 ₁₆																						
Contents at address FFFF ₁₆																						
Timer A4 mode register	(5A ₁₆)... <table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆								Program counter PC _L	<table border="1"><tr><td colspan="8">Contents at address FFFE₁₆</td></tr></table>	Contents at address FFFE ₁₆										
00 ₁₆																						
Contents at address FFFE ₁₆																						
Timer B0 mode register	(5B ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>?</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	?	X	0	0	0	0	Direct page registers DPR0 to DPR3	<table border="1"><tr><td colspan="8">0000₁₆</td></tr></table>	0000 ₁₆										
0	0	?	X	0	0	0	0															
0000 ₁₆																						
Timer B1 mode register	(5C ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>?</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	?	X	0	0	0	0	Data bank register DT	<table border="1"><tr><td colspan="8">00₁₆</td></tr></table>	00 ₁₆										
0	0	?	X	0	0	0	0															
00 ₁₆																						
Timer B2 mode register	(5D ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>?</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	?	X	0	0	0	0	Stack pointer	<table border="1"><tr><td colspan="8">FFF₁₆</td></tr></table>	FFF ₁₆										
0	0	?	X	0	0	0	0															
FFF ₁₆																						

Notes 1: The contents of the other registers and RAM are undefined at reset and must be initialized by software.

2: The status just after reset depends on the voltage level applied to pin MD0.

3: At power-on reset, these bits are clear to "0". At hardware or software reset, on the other hand, these bits retain the state just before reset.

Fig. 6 Microcomputer internal status just after reset (1)

	Address		Address																
$\overline{CS}_0$ control register L	(80 ₁₆)... <table><tr><td>Note 2</td><td>1</td><td>0</td><td>X</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table>	Note 2	1	0	X	0	Note 3	1	0	DMA0 interrupt control register	(B2 ₁₆)... <table><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0
Note 2	1	0	X	0	Note 3	1	0												
X	X	X	X	0	0	0	0												
$\overline{CS}_0$ control register H	(81 ₁₆)... <table><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td></tr></table>	X	X	X	X	X	0	0	1	DMA1 interrupt control register	(B3 ₁₆)... <table><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0
X	X	X	X	X	0	0	1												
X	X	X	X	0	0	0	0												
$\overline{CS}_1$ control register L	(82 ₁₆)... <table><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table>	0	1	0	0	0	Note 3	1	0	DMA2 interrupt control register	(B4 ₁₆)... <table><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0
0	1	0	0	0	Note 3	1	0												
X	X	X	X	0	0	0	0												
$\overline{CS}_1$ control register H	(83 ₁₆)... <table><tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr></table>	0	X	X	X	X	0	0	0	DMA3 interrupt control register	(B5 ₁₆)... <table><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0
0	X	X	X	X	0	0	0												
X	X	X	X	0	0	0	0												
$\overline{CS}_2$ control register L	(84 ₁₆)... <table><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table>	0	1	0	0	0	Note 3	1	0	DMA0 mode register L	(CC ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
0	1	0	0	0	Note 3	1	0												
0	0	0	0	0	0	0	0												
$\overline{CS}_2$ control register H	(85 ₁₆)... <table><tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr></table>	0	X	X	X	X	0	0	0	DMA0 mode register H	(CD ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
0	X	X	X	X	0	0	0												
0	0	0	0	0	0	0	0												
$\overline{CS}_3$ control register L	(86 ₁₆)... <table><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table>	0	1	0	0	0	Note 3	1	0	DMA0 control register	(CE ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
0	1	0	0	0	Note 3	1	0												
0	0	0	0	0	0	0	0												
$\overline{CS}_3$ control register H	(87 ₁₆)... <table><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	X	0	0	0	DMA1 mode register L	(DC ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
X	X	X	X	X	0	0	0												
0	0	0	0	0	0	0	0												
Area $\overline{CS}_0$ start address register	(8A ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	1	0	0	0	0	DMA1 mode register H	(DD ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0												
0	0	0	0	0	0	0	0												
Area $\overline{CS}_1$ start address register	(8C ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA1 control register	(DE ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0												
0	0	0	0	0	0	0	0												
Area $\overline{CS}_2$ start address register	(8E ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA2 mode register L	(EC ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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0	0	0	0	0	0	0	0												
Area $\overline{CS}_3$ start address register	(90 ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA2 mode register H	(ED ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0												
0	0	0	0	0	0	0	0												
Real-time output control register	(A0 ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA2 control register	(EE ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0												
0	0	0	0	0	0	0	0												
DRAM control register	(A8 ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA3 mode register L	(FC ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0												
0	0	0	0	0	0	0	0												
$\overline{CTS}/\overline{RTS}$ separate select register	(AC ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA3 mode register H	(FD ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0												
0	0	0	0	0	0	0	0												
DMAC control register L	(B0 ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA3 control register	(FE ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0												
0	0	0	0	0	0	0	0												
DMAC control register H	(B1 ₁₆)... <table><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0										
0	0	0	0	0	0	0	0												

Notes 1: The contents of the other registers and RAM are undefined at reset and must be initialized by software.

2: The status just after reset depends on the voltage level applied to pin MD0.

3: While Vss level voltage is applied to pin BYTE, these bits are "0". While Vcc level voltage is applied to pin BYTE, on the other hand, these bits are "1".

Fig. 7 Microcomputer internal registers' status just after reset (2)

INPUT/OUTPUT PINS

Each of ports P3 to P9 and P12 has an direction register, and each bit can be programmed for input or output. A pin becomes an output pin when the corresponding bit of direction register is "1", and an input pin when it is "0".

When a pin is programmed as an output pin, the data written to its port latch is output to the output pin. When a pin is programmed as an output pin, the contents of the port latch are read out instead of the value of the pin. Accordingly, a previously output value can be read out correctly even when the output "H" voltage is lowered or the output "L" voltage is raised, owing to an external load, etc.

A pin programmed as an input pin is placed in the floating state, and the value input to the pin can be read out correctly. When a pin is programmed as an input pin, the data can be written only in the port latch, and the pin remains floating.

Each of Figures 8 and 9 shows the block diagram for each port pin.

Table 2. Correspondence between external buses, bus control signals, and programmable I/O port pins

External buses, Bus control signals	Standby state select bit	
	0	1
A0 to A7, A8 to A15, A16 to A23	A0 to A7, A8 to A15, A16 to A23	P10 ₀ to P10 ₇ (Note 2), P11 ₀ to P11 ₇ (Note 2), P0 ₀ to P0 ₇ (Note 2)
D0 to D7, D8 to D15	D0 to D7, D8 to D15 (Note 1)	P1 ₀ to P1 ₇ (Note 2), P2 ₀ to P2 ₇
RD, BLW, BHW	RD, BLW, BHW (Note 1)	P3 ₁ , P3 ₂ (Note 2), P3 ₃
CS ₀	CS ₀	P9 ₀ (Note 2)

Notes 1: When the external data bus width = 8 bits (BYTE = V_{CC} level), this becomes a programmable I/O port pin, regardless of the standby state select bit's contents.

2: Pin functions of port pins P0, P1, P3₁, P3₂, P9₀, P10, P11 are not shown in the pin configuration. However, relationship with corresponding bus signals and ports is listed in Table 2. For the addresses of these port's registers and direction registers, refer to the location of the peripheral devices' control registers (Figures 2 and 3).



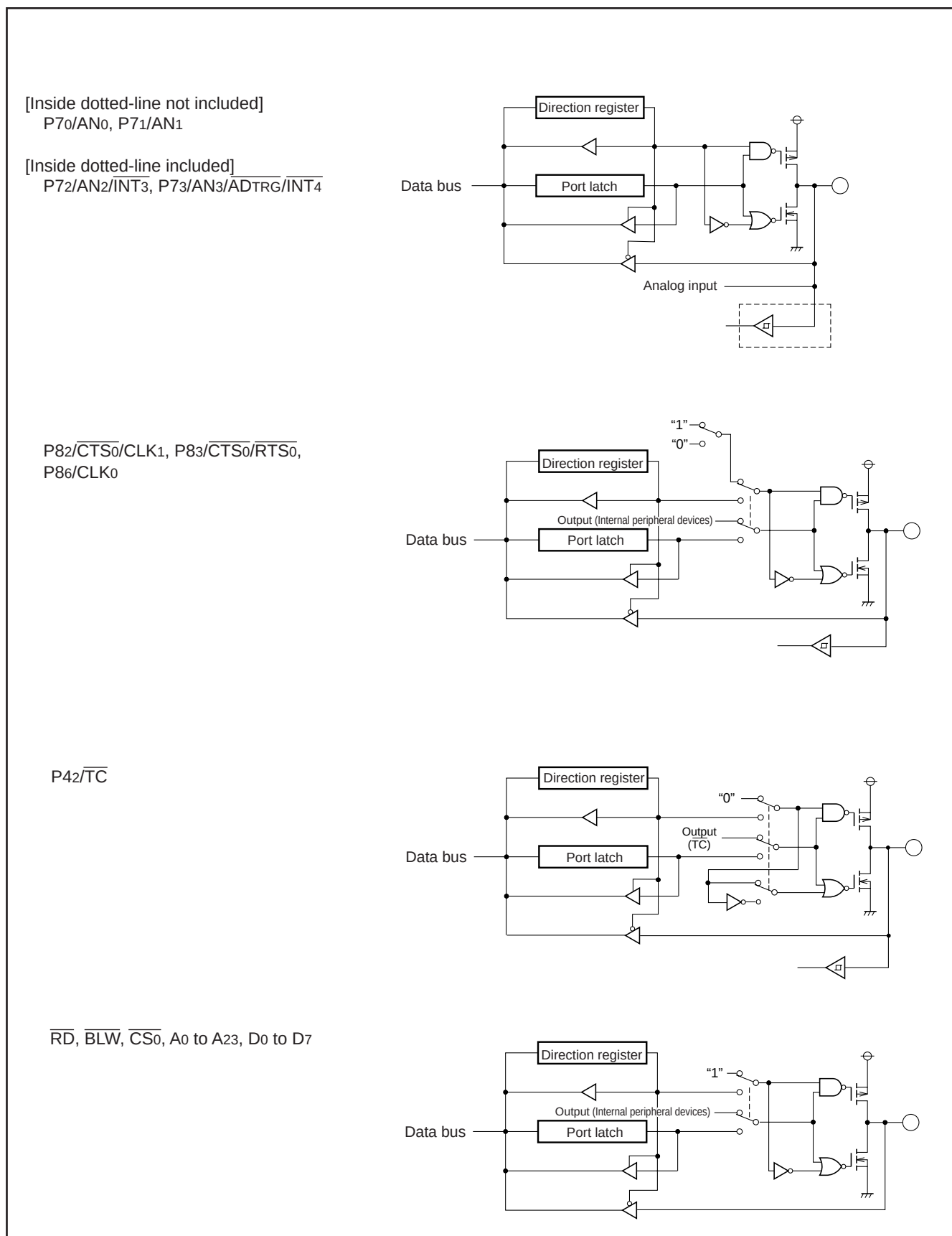


Fig. 9 Block diagram for each port pin (2)

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V _{CC}	Power source voltage	−0.3 to 6.5	V
AV _{CC}	Analog power source voltage	−0.3 to 6.5	V
V _I	Input voltage D ₀ –D ₇ , D ₈ /P ₂₀ –D ₁₅ /P ₂₇ , P ₃₀ , P ₃₃ , P ₄₀ –P ₄₄ , P ₅₀ –P ₅₇ , P ₆₀ –P ₆₆ , P ₇₀ –P ₇₃ , P ₈₀ –P ₈₆ , P ₉₁ –P ₉₆ , P ₁₂₀ –P ₁₂₂ , V _{REF} , X _{IN} , $\overline{\text{RESET}}$, BYTE, MD ₀ , MD ₁ , NMI	−0.3 to V _{CC} +0.3	V
V _O	Output voltage A ₀ –A ₂₃ , $\overline{\text{RD}}$, $\overline{\text{BLW}}$, BHW/P ₃₃ , $\overline{\text{CS}}$ ₀ , D ₀ –D ₇ , D ₈ /P ₂₀ –D ₁₅ /P ₂₇ , P ₃₀ , P ₄₀ –P ₄₄ , P ₅₀ –P ₅₇ , P ₆₀ –P ₆₆ , P ₇₀ –P ₇₃ , P ₈₀ –P ₈₆ , P ₉₁ –P ₉₆ , P ₁₂₀ –P ₁₂₂ , X _{OUT}	−0.3 to V _{CC} +0.3	V
P _d	Power dissipation	300	mW
T _{opr}	Operating temperature	−20 to 85	°C
T _{stg}	Storage temperature	−40 to 150	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5 V, T_a = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Power source voltage	4.5	5	5.5	V
AV _{CC}	Analog power source voltage		V _{CC}		V
V _{SS}	Power source voltage		0		V
AV _{SS}	Analog power source voltage		0		V
V _{IH}	High-level input voltage P ₂₀ –P ₂₇ , P ₃₀ , P ₃₃ , P ₄₀ –P ₄₄ , P ₅₀ –P ₅₇ , P ₆₀ –P ₆₆ , P ₇₀ –P ₇₃ , P ₈₀ –P ₈₆ , P ₉₁ –P ₉₆ , P ₁₂₀ –P ₁₂₂ , X _{IN} , $\overline{\text{RESET}}$, BYTE, MD ₀ , MD ₁ , NMI	0.8V _{CC}		V _{CC}	V
V _{IH}	High-level input voltage D ₀ –D ₇ , D ₈ –D ₁₅	0.5V _{CC}		V _{CC}	V
V _{IL}	Low-level input voltage P ₂₀ –P ₂₇ , P ₃₀ , P ₃₃ , P ₄₀ –P ₄₄ , P ₅₀ –P ₅₇ , P ₆₀ –P ₆₆ , P ₇₀ –P ₇₃ , P ₈₀ –P ₈₆ , P ₉₁ –P ₉₆ , P ₁₂₀ –P ₁₂₂ , X _{IN} , $\overline{\text{RESET}}$, BYTE, MD ₀ , MD ₁ , NMI	0		0.2V _{CC}	V
V _{IL}	Low-level input voltage D ₀ –D ₇ , D ₈ –D ₁₅	0		0.16V _{CC}	V
I _{OH} (peak)	High-level peak output current A ₀ –A ₂₃ , $\overline{\text{RD}}$, $\overline{\text{BLW}}$, BHW/P ₃₃ , $\overline{\text{CS}}$ ₀ , D ₀ –D ₇ , D ₈ /P ₂₀ –D ₁₅ /P ₂₇ , P ₃₀ , P ₄₀ –P ₄₄ , P ₅₀ –P ₅₇ , P ₆₀ –P ₆₆ , P ₇₀ –P ₇₃ , P ₈₀ –P ₈₆ , P ₉₁ –P ₉₆ , P ₁₂₀ –P ₁₂₂			−10	mA
I _{OH} (avg)	High-level average output current A ₀ –A ₂₃ , $\overline{\text{RD}}$, $\overline{\text{BLW}}$, BHW/P ₃₃ , $\overline{\text{CS}}$ ₀ , D ₀ –D ₇ , D ₈ /P ₂₀ –D ₁₅ /P ₂₇ , P ₃₀ , P ₄₀ –P ₄₄ , P ₅₀ –P ₅₇ , P ₆₀ –P ₆₆ , P ₇₀ –P ₇₃ , P ₈₀ –P ₈₆ , P ₉₁ –P ₉₆ , P ₁₂₀ –P ₁₂₂			−5	mA
I _{OL} (peak)	Low-level peak output current A ₀ –A ₂₃ , $\overline{\text{RD}}$, $\overline{\text{BLW}}$, BHW/P ₃₃ , $\overline{\text{CS}}$ ₀ , D ₀ –D ₇ , D ₈ /P ₂₀ –D ₁₅ /P ₂₇ , P ₃₀ , P ₄₀ –P ₄₄ , P ₅₀ –P ₅₇ , P ₆₀ –P ₆₆ , P ₇₀ –P ₇₃ , P ₈₀ –P ₈₆ , P ₉₁ –P ₉₆ , P ₁₂₀ –P ₁₂₂			10	mA
I _{OL} (avg)	Low-level average output current A ₀ –A ₂₃ , $\overline{\text{RD}}$, $\overline{\text{BLW}}$, BHW/P ₃₃ , $\overline{\text{CS}}$ ₀ , D ₀ –D ₇ , D ₈ /P ₂₀ –D ₁₅ /P ₂₇ , P ₃₀ , P ₄₀ –P ₄₄ , P ₅₀ –P ₅₇ , P ₆₀ –P ₆₆ , P ₇₀ –P ₇₃ , P ₈₀ –P ₈₆ , P ₉₁ –P ₉₆ , P ₁₂₀ –P ₁₂₂			5	mA
f(X _{IN})	External clock input frequency			20	MHz

Notes 1: Average output current is the average value of an interval of 100 ms.

2: The sum of I_{OL}(peak) for A₀–A₂₃, D₀–D₇, D₈/P₂₀–D₁₅/P₂₇, ports P₈₀–P₈₆ must be 80 mA or less, the sum of I_{OH}(peak) for A₀–A₂₃, D₀–D₇, D₈/P₂₀–D₁₅/P₂₇, ports P₈₀–P₈₆ must be 80 mA or less, the sum of I_{OL}(peak) for ports P₃₀, $\overline{\text{RD}}$, $\overline{\text{BLW}}$, BHW/P₃₃, $\overline{\text{CS}}$ ₀, P₄₀–P₄₄, P₅₀–P₅₇, P₆₀–P₆₆, P₇₀–P₇₃, P₉₁–P₉₆, P₁₂₀–P₁₂₂ must be 80 mA or less, the sum of I_{OH}(peak) for P₃₀, $\overline{\text{RD}}$, $\overline{\text{BLW}}$, BHW/P₃₃, $\overline{\text{CS}}$ ₀, P₄₀–P₄₄, P₅₀–P₅₇, P₆₀–P₆₆, P₇₀–P₇₃, P₉₁–P₉₆, P₁₂₀–P₁₂₂ must be 80 mA or less.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, V_{SS} = 0 V, T_a = -20 to 85 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{OH}	High-level output voltage A0–A23, $\overline{CS}_0$, D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P93, P120–P122	I _{OH} = -10 mA	3			V
V _{OH}	High-level output voltage A0–A23, $\overline{CS}_0$, D0–D7, D8/P20–D15/P27, P40, P44, P91–P93	I _{OH} = -400 μ A	4.7			V
V _{OH}	High-level output voltage $\overline{RD}$, BLW, $\overline{BHW}$ /P33, P94/CASW, P95/WRL/LCAS, P96/WRH/UCAS	I _{OH} = -10 mA	3.4			V
		I _{OH} = -400 μ A	4.8			
V _{OL}	Low-level output voltage A0–A23, $\overline{CS}_0$, D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P93, P120–P122	I _{OL} = 10 mA			2	V
V _{OL}	Low-level output voltage A0–A23, $\overline{CS}_0$, D0–D7, D8/P20–D15/P27, P40, P44, P91–P93	I _{OL} = 2 mA			0.45	V
V _{OL}	Low-level output voltage $\overline{RD}$, BLW, $\overline{BHW}$ /P33, P94/CASW, P95/WRL/LCAS, P96/WRH/UCAS	I _{OL} = 10 mA			1.6	V
		I _{OL} = 2 mA			0.4	
V _{T+} – V _{T–}	Hysteresis TA0IN–TA4IN, TB0IN–TB2IN, INT0–INT4, DMAREQ0–DMAREQ3, ADTRG, CTS0, CLK0, CLK1, NMI, RDY, HOLD, RxD0, RxD1		0.4		1	V
V _{T+} – V _{T–}	Hysteresis $\overline{RESET}$		0.5		1.5	V
V _{T+} – V _{T–}	Hysteresis X _{IN}		0.1		0.3	V
I _{IH}	High-level input current D0–D7, D8/P20–D15/P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122, X _{IN} , $\overline{RESET}$, BYTE, MD0, MD1, NMI	V _I = 5.0 V			5	μ A
I _{IL}	Low-level input current D0–D7, D8/P20–D15/P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122, X _{IN} , $\overline{RESET}$, BYTE, MD0, MD1, NMI	V _I = 0 V			-5	μ A
V _{RAM}	RAM hold voltage	When clock is stopped.	2			V
I _{CC}	Power source current	At reset in micro-processor mode, output-only pins are open, and the other pins are connected to V _{SS} .	f(X _{IN}) = 20 MHz.	25	50	mA
			T _a = 25 °C when clock is stopped.		1	
			T _a = 80 °C when clock is stopped.		20	

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

A-D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
————	Resolution	$V_{REF} = V_{CC}$		10	Bits
————	Absolute accuracy	$V_{REF} = V_{CC}$	10-bit resolution mode	± 3	LSB
			8-bit resolution mode	± 2	LSB
RLADDER	Ladder resistance	$V_{REF} = V_{CC}$	5		k Ω
tCONV	Conversion time	$f(X_{IN}) \leq 20\text{ MHz}$	10-bit resolution mode	5.9	μs
			8-bit resolution mode	2.45 (Note)	
VREF	Reference voltage	————	2.7	V_{CC}	V
VIA	Analog input voltage	————	0	VREF	V

Note: This is applied when A-D conversion frequency (ϕ_{AD}) = $f_{1(\phi)}$.

PERIPHERAL DEVICE INPUT/OUTPUT TIMING

(VCC = 5 V ± 10 %, VSS = 0 V, Ta = -20 to 85 °C, f(XIN) = 20 MHz unless otherwise noted)

* For limits depending on f(XIN), their calculation formulas are shown below. Also, the values at f(XIN) = 20 MHz are shown in ().

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiN input cycle time	80		ns
tw(TAH)	TAiN input high-level pulse width	40		ns
tw(TAL)	TAiN input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
tc(TA)	TAiN input cycle time	f(XIN) ≤ 20 MHz	$\frac{16 \times 10^9}{f(XIN)}$ (800)		ns
tw(TAH)	TAiN input high-level pulse width	f(XIN) ≤ 20 MHz	$\frac{8 \times 10^9}{f(XIN)}$ (400)		ns
tw(TAL)	TAiN input low-level pulse width	f(XIN) ≤ 20 MHz	$\frac{8 \times 10^9}{f(XIN)}$ (400)		ns

Note : The TAiN input cycle time requires 4 or more cycles of a count source. The TAiN input high-level pulse width and the TAiN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f2 at f(XIN) ≤ 20 MHz.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
tc(TA)	TAiN input cycle time	f(XIN) ≤ 20 MHz	$\frac{8 \times 10^9}{f(XIN)}$ (400)		ns
tw(TAH)	TAiN input high-level pulse width		80		ns
tw(TAL)	TAiN input low-level pulse width		80		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tw(TAH)	TAiN input high-level pulse width	80		ns
tw(TAL)	TAiN input low-level pulse width	80		ns

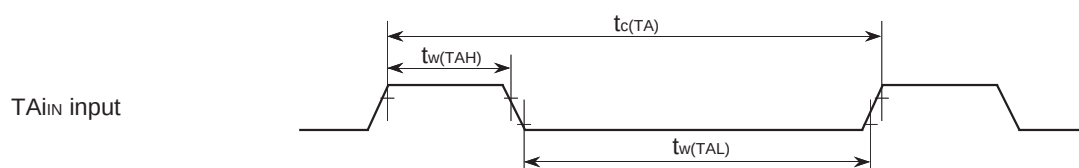
Timer A input (Up-down input and Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high-level pulse width	1000		ns
tw(UPL)	TAiOUT input low-level pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

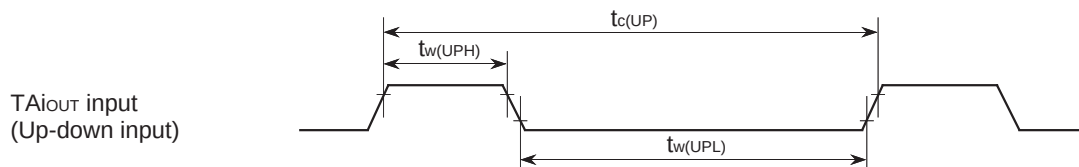
Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(TA)$	TAiN input cycle time	800		ns
$t_{su}(TA_{iN}-TA_{jOUT})$	TAjIN input setup time	200		ns
$t_{su}(TA_{jOUT}-TA_{iN})$	TAjOUT input setup time	200		ns

- Gating input in timer mode
- Count input in event counter mode
- External trigger input in one-shot pulse mode
- External trigger input in pulse width modulation mode



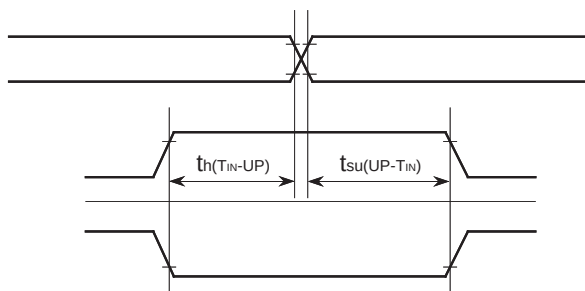
- Up-down input and Count input in event counter mode



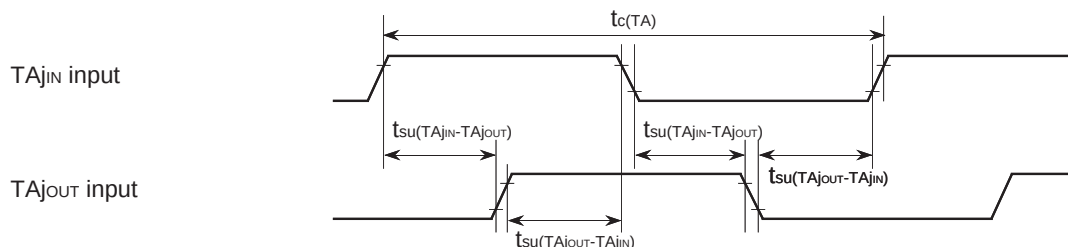
TAiOUT input
(Up-down input)

TAiIN input
(When count at falling)

TAiIN input
(When count at rising)



- Two-phase pulse input in event counter mode



Test conditions

- Vcc = 5 V ± 10 %, Ta = -20 to 85 °C
- Input timing voltage : VIL = 1.0 V, VIH = 4.0 V

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (TB)	TBiIn input cycle time (one edge count)	80		ns
t _w (TBH)	TBiIn input high-level pulse width (one edge count)	40		ns
t _w (TBL)	TBiIn input low-level pulse width (one edge count)	40		ns
t _c (TB)	TBiIn input cycle time (both edge count)	160		ns
t _w (TBH)	TBiIn input high-level pulse width (both edge count)	80		ns
t _w (TBL)	TBiIn input low-level pulse width (both edge count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
t _c (TB)	TBiIn input cycle time	f(X _{IN}) ≤ 20 MHz	$\frac{16 \times 10^9}{f(X_{IN})}$ (800)		ns
t _w (TBH)	TBiIn input high-level pulse width	f(X _{IN}) ≤ 20 MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns
t _w (TBL)	TBiIn input low-level pulse width	f(X _{IN}) ≤ 20 MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns

Note: The TBiIn input cycle time requires 4 or more cycles of a count source. The TBiIn input high-level pulse width and the TBiIn input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f₂ at f(X_{IN}) ≤ 20 MHz.

Timer B input (Pulse width measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
t _c (TB)	TBiIn input cycle time	f(X _{IN}) ≤ 20 MHz	$\frac{16 \times 10^9}{f(X_{IN})}$ (800)		ns
t _w (TBH)	TBiIn input high-level pulse width	f(X _{IN}) ≤ 20 MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns
t _w (TBL)	TBiIn input low-level pulse width	f(X _{IN}) ≤ 20 MHz	$\frac{8 \times 10^9}{f(X_{IN})}$ (400)		ns

Note: The TBiIn input cycle time requires 4 or more cycles of a count source. The TBiIn input high-level pulse width and the TBiIn input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f₂ at f(X_{IN}) ≤ 20 MHz.

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (AD)	ADTRG input cycle time (minimum allowable trigger)	1000		ns
t _w (ADL)	ADTRG input low-level pulse width	125		ns

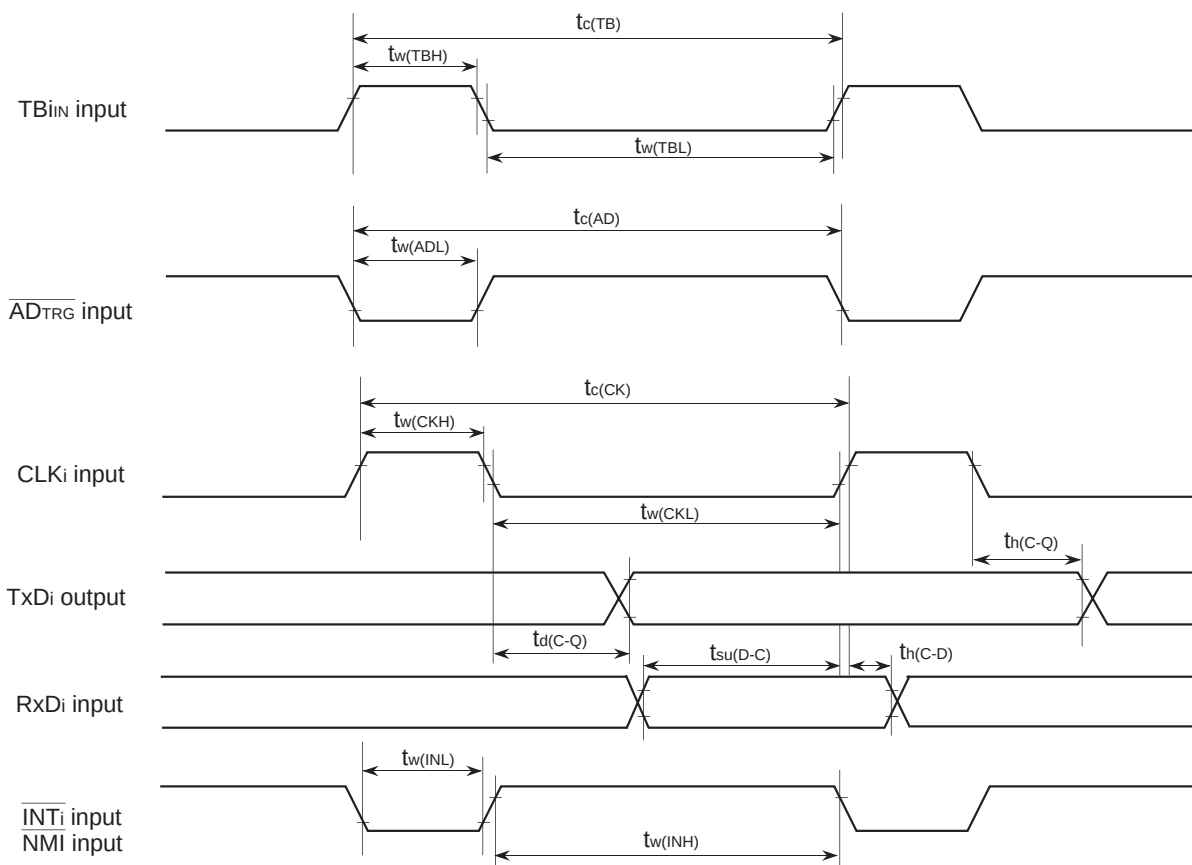
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(\text{CK})$	CLKi input cycle time	200		ns
$t_w(\text{CKH})$	CLKi input high-level pulse width	100		ns
$t_w(\text{CKL})$	CLKi input low-level pulse width	100		ns
$t_d(\text{C-Q})$	TxDi output delay time		80	ns
$t_h(\text{C-Q})$	TxDi hold time	0		ns
$t_{su}(\text{D-C})$	RxDi input setup time	20		ns
$t_h(\text{C-D})$	RxDi input hold time	90		ns

External interrupt ($\overline{\text{INTi}}$) input, $\overline{\text{NMI}}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(\text{INH})$	$\overline{\text{INTi}}$ input/ $\overline{\text{NMI}}$ input high-level pulse width	250		ns
$t_w(\text{INL})$	$\overline{\text{INTi}}$ input/ $\overline{\text{NMI}}$ input low-level pulse width	250		ns



Test conditions

- $V_{CC} = 5 \text{ V} \pm 10 \%$, $T_a = -20 \text{ to } 85 \text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 1.0 \text{ V}$, $V_{IH} = 4.0 \text{ V}$
- Output timing voltage : $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$, $C_L = 50 \text{ pF}$

READY, HOLD TIMING

Timing requirements ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

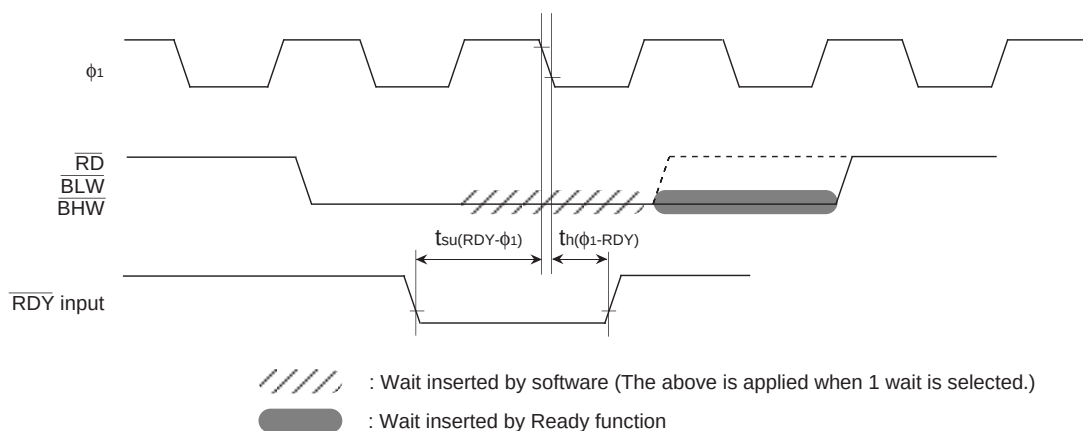
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(RDY-\phi 1)$	$\overline{RDY}$ input setup time	40		ns
$t_{su}(HOLD-\phi 1)$	$\overline{HOLD}$ input setup time	40		ns
$t_h(\phi 1-RDY)$	$\overline{RDY}$ input hold time	0		ns
$t_h(\phi 1-HOLD)$	$\overline{HOLD}$ input hold time	0		ns

Switching characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

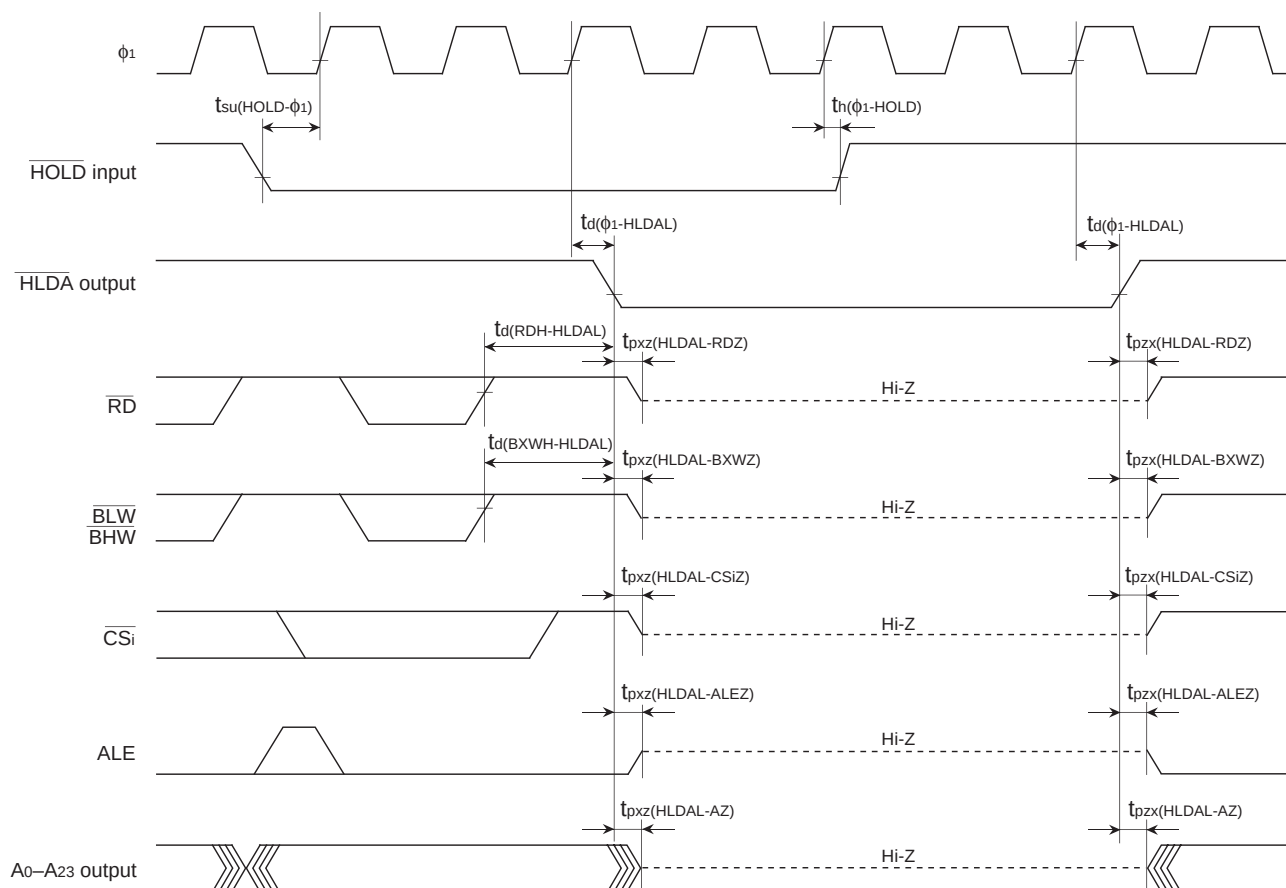
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_d(\phi 1-HLDA)$	$\overline{HLDA}$ output delay time		20	ns
$t_d(RDH-HLDA)$	$\overline{HLDA}$ low-level output delay time after read	$t_c - 15$ (Note)		ns
$t_d(BXWH-HLDA)$	$\overline{HLDA}$ low-level output delay time after write	$t_c - 15$ (Note)		ns
$t_{pxz}(HLDA-RDZ)$	Floating start delay time	-15	10	ns
$t_{pxz}(HLDA-BXWZ)$	Floating start delay time	-15	10	ns
$t_{pxz}(HLDA-CSIZ)$	Floating start delay time	-15	10	ns
$t_{pxz}(HLDA-ALEZ)$	Floating start delay time	-15	10	ns
$t_{pxz}(HLDA-AZ)$	Floating start delay time	-15	10	ns
$t_{pzx}(HLDA-RDZ)$	Floating release delay time	0		ns
$t_{pzx}(HLDA-BXWZ)$	Floating release delay time	0		ns
$t_{pzx}(HLDA-CSIZ)$	Floating release delay time	0		ns
$t_{pzx}(HLDA-ALEZ)$	Floating release delay time	0		ns
$t_{pzx}(HLDA-AZ)$	Floating release delay time	0		ns

Note: $t_c = 1/f(X_{IN})$.

RDY input



HOLD input



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = -20$ to $85\text{ }^\circ\text{C}$
- RDY input, HOLD input : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$
- HLDA output : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$

External bus timing

For limits depending on $f(X_{IN})$, their calculation formulas are shown below.

$W = 0$ (0 wait)

$W = 1$ (1 wait)

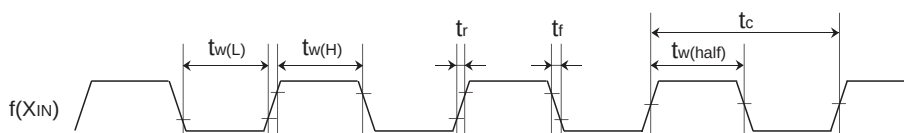
$W = 2$ (2 wait)

$t_c = 1/f(X_{IN})$.

Timing Requirements ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20$ to $85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Limits				Unit
		When 0/1/2 wait is selected		When ALE expansion wait is selected		
		Min.	Max.	Min.	Max.	
tc	External clock input cycle time	50		50		ns
tw(half)	External clock input pulse width with half input-voltage	0.45tc	0.55tc	0.45tc	0.55tc	ns
tw(H)	External clock input high-level pulse width	0.5tc – 8		0.5tc – 8		ns
tw(L)	External clock input low-level pulse width	0.5tc – 8		0.5tc – 8		ns
tr	External clock input rise time		8		8	ns
tf	External clock input fall time		8		8	ns
ta(A-D)	Address access time		(2 + W)tc – 45		4tc – 45	ns
ta(CSiL-D)	Chip select access time		(1.5 + W)tc – 35		3.5tc – 35	ns
ta(RDL-D)	Read access time		(1 + W)tc – 30		2tc – 30	ns
tsu(D-RDL)	Read data setup time	15		15		ns
th(RDH-D)	Data input hold time after read	0		0		ns
ta(BA-D)	Address access time at burst ROM access		(1 + W)tc – 35		2tc – 35	ns
th(BA-D)	Data hold time after address at burst ROM access	0		0		ns

External clock input



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = -20$ to $85\text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$ ($t_{w(H)}$, $t_{w(L)}$, t_r , t_f)
- Input timing voltage : 2.5 V (t_c , $t_{w(\text{half})}$)

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Switching characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

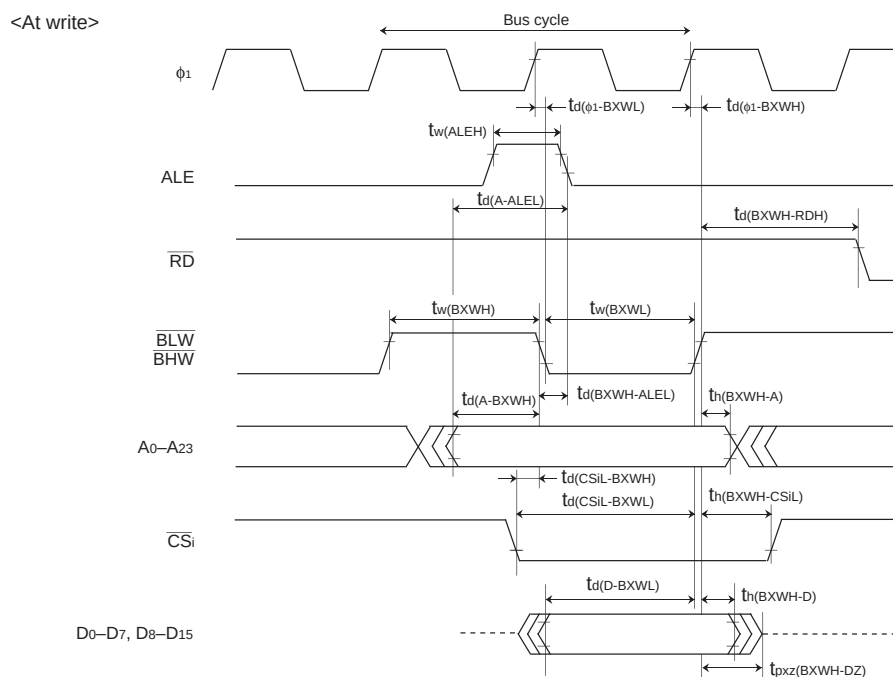
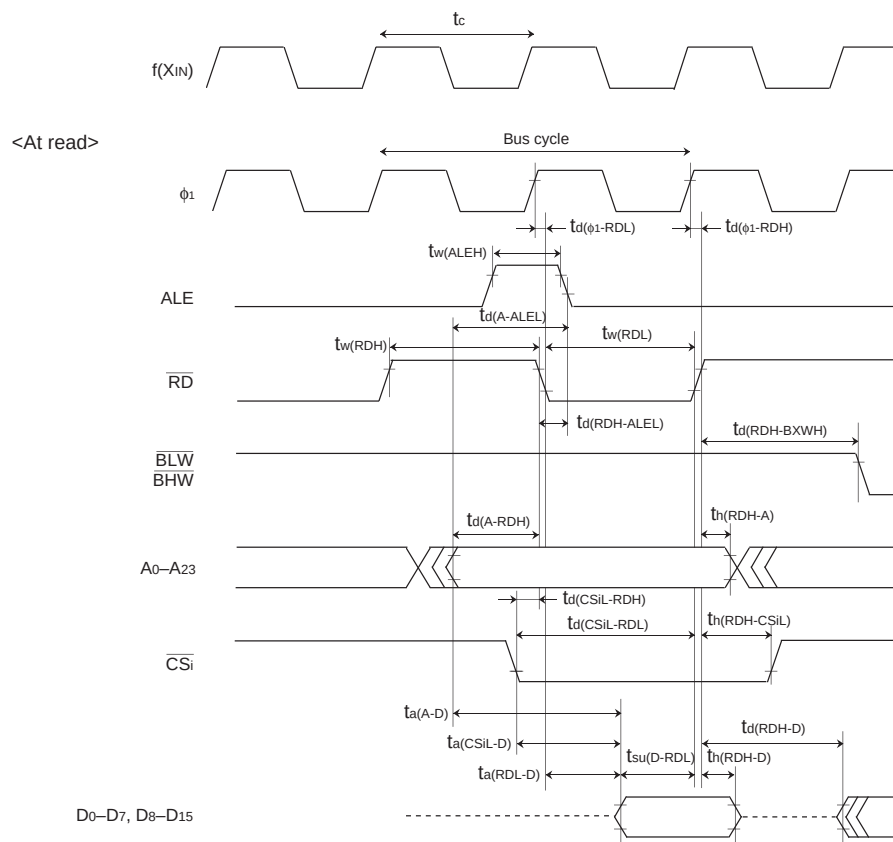
Symbol	Parameter	Limits				Unit
		When 0/1/2 wait is selected		When ALE expansion wait is selected		
		Min.	Max.	Min.	Max.	
td(φ1-RDL)	Read low-level output delay time	−10	15	−10	15	ns
td(φ1-RDH)	Read high-level output delay time	−10	10	−10	10	ns
td(φ1-BXWL)	Write low-level output delay time	−10	15	−10	15	ns
td(φ1-BXWH)	Write high-level output delay time	−10	10	−10	10	ns
tw(ALEH)	ALE pulse width	0.5tc − 20		tc − 20		ns
td(A-ALEL)	ALE completion delay time after address stabilization	tc − 30		1.5tc − 30		ns
tw(RDL)	Read output pulse width	(1 + W)tc − 15		2tc − 15		ns
tw(RDH)	Read output high-level width (Note 1)	tc − 15		2tc − 15		ns
td(RDH-BXWH)	Write disable valid time after read (Note 2)	tc − 15		tc − 15		ns
td(A-RDH)	Address valid time before read	tc − 30		2tc − 30		ns
th(RDH-A)	Address hold time after read (Note 3)	8		8		ns
td(RDH-ALEL)	ALE completion delay time after read start		20			ns
td(ALEL-RDH)	Read disable valid time after ALE completion			0.5tc − 20		ns
td(CSiL-RDH)	Chip select valid time before read	0.5tc − 20		1.5tc − 20		ns
td(CSiL-RDL)	Chip select output valid time before read completion	(1.5 + W)tc − 20		3.5tc − 20		ns
th(RDH-CSiL)	Chip select hold time after read	0.5tc − 20		0.5tc − 20		ns
td(RDH-D)	Next write cycle data output delay time after read (Note 2)	tc − 15		tc − 15		ns
tw(BXWL)	Write output pulse width	(1 + W)tc − 15		2tc − 15		ns
tw(BXWH)	Write output high-level width (Note 1)	tc − 15		2tc − 15		ns
td(BXWH-RDH)	Read disable valid time after write (Note 2)	tc − 15		tc − 15		ns
td(A-BXWH)	Address valid time before write	tc − 30		2tc-30		ns
th(BXWH-A)	Address hold time after write (Note 3)	8		8		ns
td(BXWH-ALEL)	ALE completion delay time after write start		20			ns
td(ALEL-BXWH)	Write disable valid time after ALE completion			0.5tc − 20		ns
td(CSiL-BXWH)	Chip select valid time before write	0.5tc − 20		1.5tc − 20		ns
td(CSiL-BXWL)	Chip select output valid time before write completion	(1.5 + W)tc − 20		3.5tc − 20		ns
th(BXWH-CSiL)	Chip select hold time after write	0.5tc − 20		0.5tc − 20		ns
td(D-BXWL)	Data output valid time before write completion	(1 + W)tc − 20		2tc − 20		ns
th(BXWH-D)	Data hold time after write	0.5tc − 10		0.5tc − 10		ns
tpxz(BXWH-DZ)	Floating start delay time after write		0.5tc + 10		0.5tc + 10	ns

Notes 1: When the bus cycle just before this parameter is for the area where the recovery cycle insertion is selected, this parameter is extended by t_c (ns).

2: When accessing the area where the recovery cycle insertion is selected, this parameter is extended by t_c (ns).

3: When accessing the area where the recovery cycle insertion is selected, this parameter is extended by t_c (ns). However, except for the case at instruction prefetch.

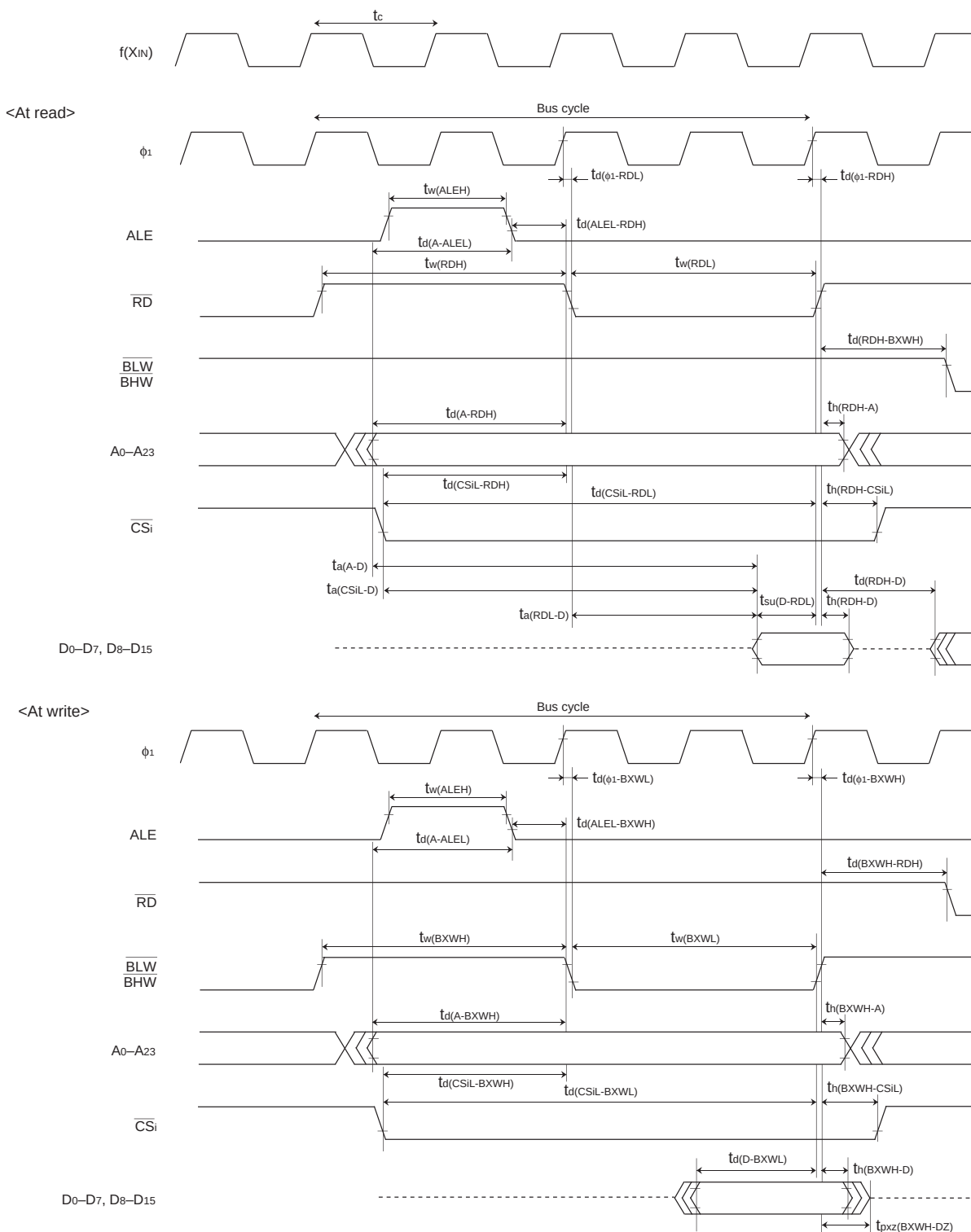
Normal access: 0/1/2 wait



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = -20$ to $85\text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 15\text{ pF}$ ($\overline{CSi}$)
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$ (except for $\overline{CSi}$)

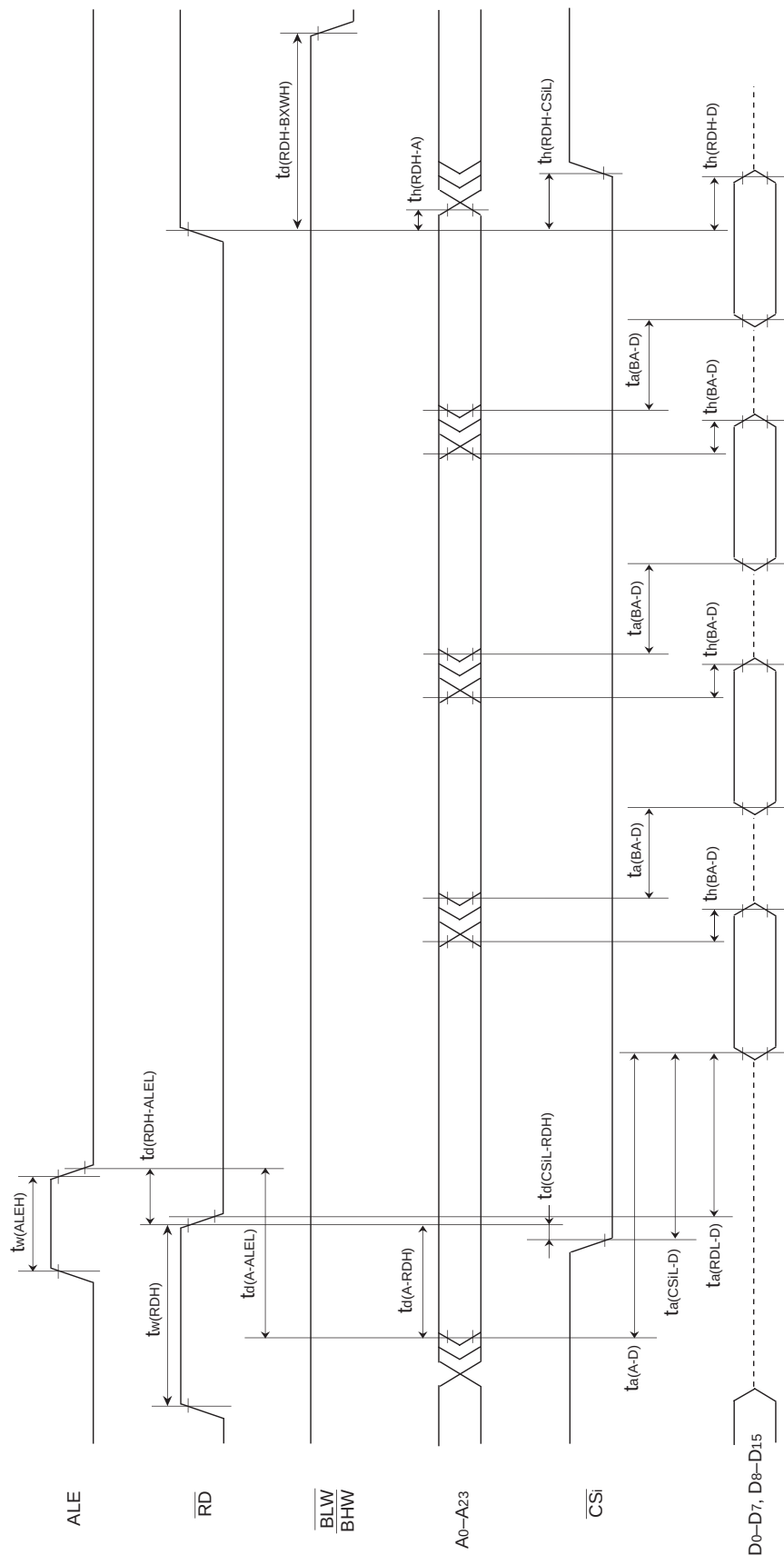
Normal access : ALE extension wait



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 15\text{ pF}$ ($\overline{CSi}$)
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$ (except for $\overline{CSi}$)

Burst ROM access : 0/1/2 wait at instruction prefetch



Test conditions

- $V_{CC} = 5 \text{ V} \pm 10 \%$, $T_a = -20 \text{ to } 85^\circ \text{C}$
- Input timing voltage : $V_{IL} = 0.8 \text{ V}$, $V_{IH} = 2.5 \text{ V}$
- Output timing voltage : $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$, $C_L = 15 \text{ pF}$ (CSi)
- Output timing voltage : $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$, $C_L = 50 \text{ pF}$ (except for CSi)

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

DRAM access

Timing Requirements ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }70\text{ }^{\circ}\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

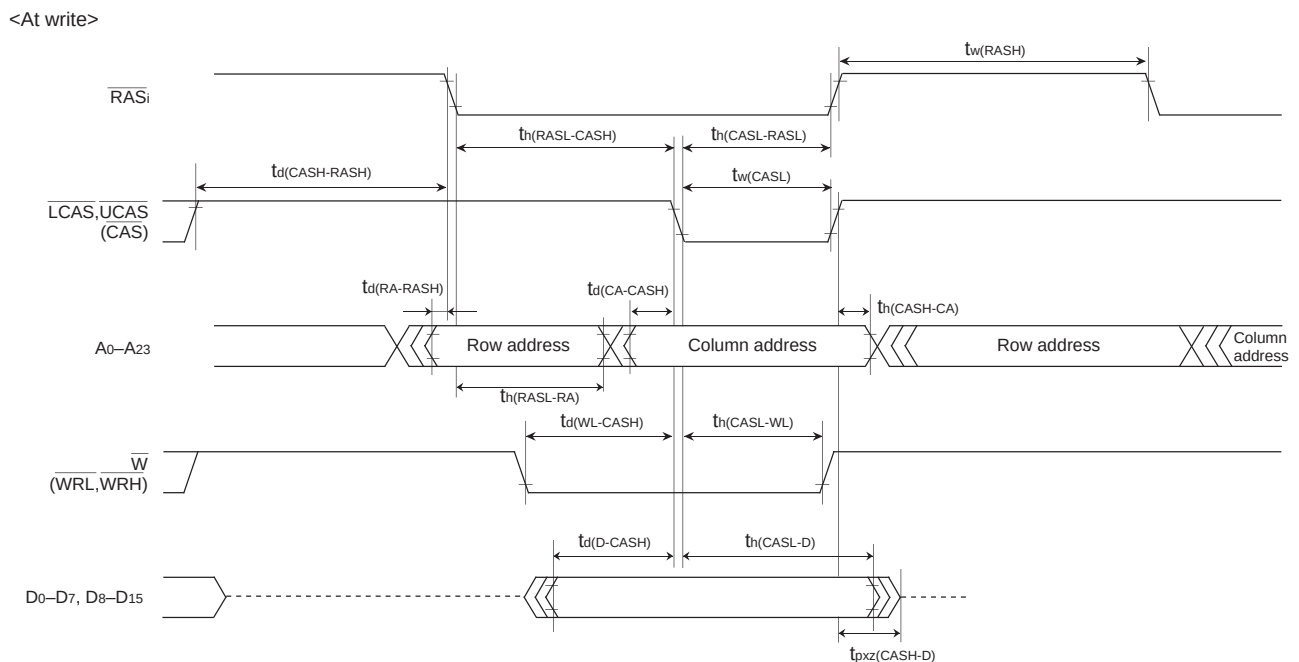
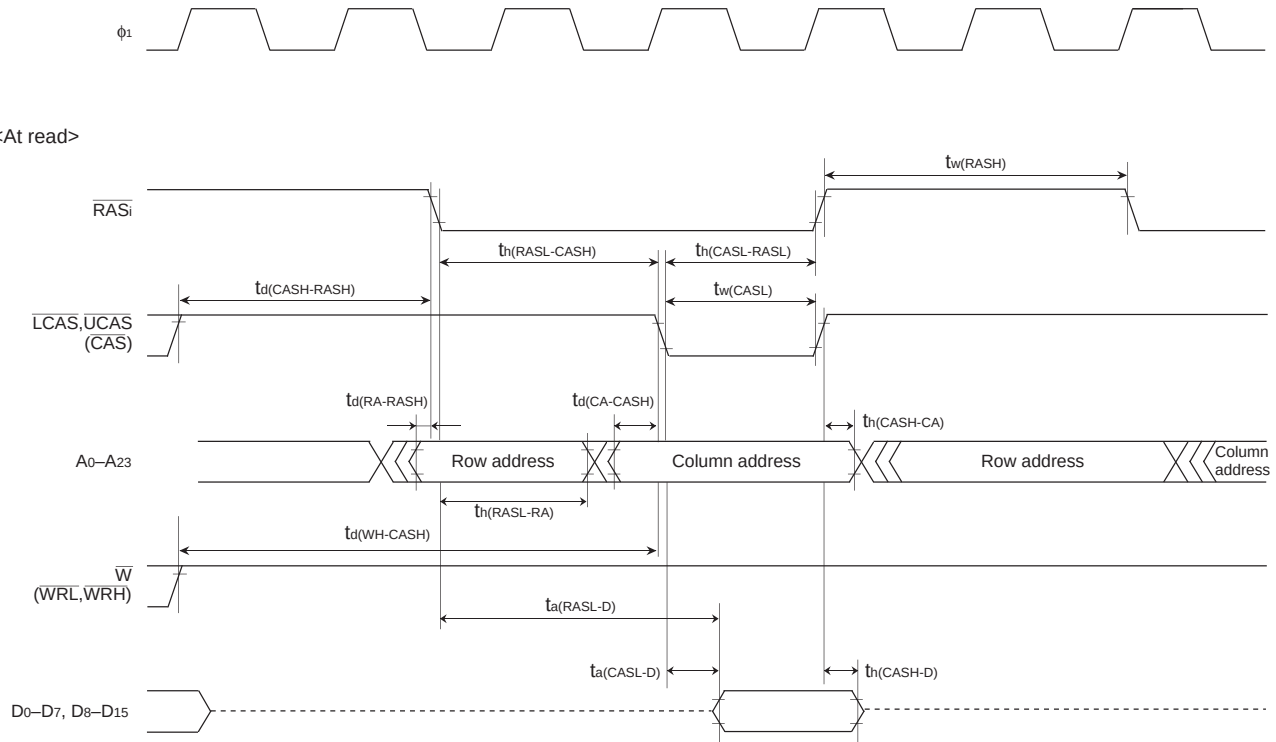
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_a(\text{RASL-D})$	$\overline{\text{RAS}}$ access time		$2.5t_c - 35$	ns
$t_a(\text{CASL-D})$	$\overline{\text{CAS}}$ access time		$t_c - 30$	ns
$t_h(\text{CASH-D})$	Data input hold time after $\overline{\text{CAS}}$	0		ns

Switching characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }70\text{ }^{\circ}\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(\text{RASH})$	$\overline{\text{RAS}}$ high-level pulse width	$1.5t_c - 20$		ns
$t_d(\text{CASH-RASH})$	$\overline{\text{CAS}}$ high-level valid time before $\overline{\text{RAS}}$	$1.5t_c - 20$		ns
$t_h(\text{RASL-CASH})$	$\overline{\text{CAS}}$ high-level hold time after $\overline{\text{RAS}}$'s low level	$1.5t_c - 20$		ns
$t_h(\text{CASL-RASL})$	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$'s low level	$t_c - 15$		ns
$t_w(\text{CASL})$	$\overline{\text{CAS}}$ low-level pulse width	$t_c - 15$		ns
$t_d(\text{RA-RASH})$	Row address valid time before $\overline{\text{RAS}}$	$0.5t_c - 25$		ns
$t_h(\text{RASL-RA})$	Row address hold time after $\overline{\text{RAS}}$'s low level	$t_c - 40$		ns
$t_d(\text{CA-CASH})$	Column address valid time before $\overline{\text{CAS}}$	$0.5t_c - 20$		ns
$t_h(\text{CASH-CA})$	Column address hold time after $\overline{\text{CAS}}$'s high level	0		ns
$t_d(\text{WH-CASH})$	$\overline{\text{W}}$ high-level valid time before $\overline{\text{CAS}}$	$3t_c - 15$		ns
$t_d(\text{WL-CASH})$	$\overline{\text{W}}$ low-level valid time before $\overline{\text{CAS}}$	$t_c - 15$		ns
$t_h(\text{CASL-WL})$	$\overline{\text{W}}$ hold time after $\overline{\text{CAS}}$'s low level	$t_c - 15$		ns
$t_d(\text{D-CASH})$	Data output valid time before $\overline{\text{CAS}}$	$t_c - 20$		ns
$t_h(\text{CASL-D})$	Data output hold time after $\overline{\text{CAS}}$'s low level	$1.5t_c - 15$		ns
$t_{pxz}(\text{CASH-D})$	Floating start delay time after $\overline{\text{CAS}}$	$0.5t_c + 10$		ns
$t_d(\text{CAF-CASH})$	Column address valid time before $\overline{\text{CAS}}$ (When fast page access ON is selected)	$t_c - 40$		ns
$t_d(\text{WFL-CASH})$	$\overline{\text{W}}$ low-level valid time before $\overline{\text{CAS}}$ (When fast page access ON is selected)	$0.5t_c - 20$		ns
$t_d(\text{DF-CASH})$	Data output valid time before $\overline{\text{CAS}}$ (When fast page access ON is selected)	$0.5t_c - 20$		ns
$t_{pxz}(\text{WH-D})$	Floating start delay time after write		$0.5t_c + 10$	ns

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

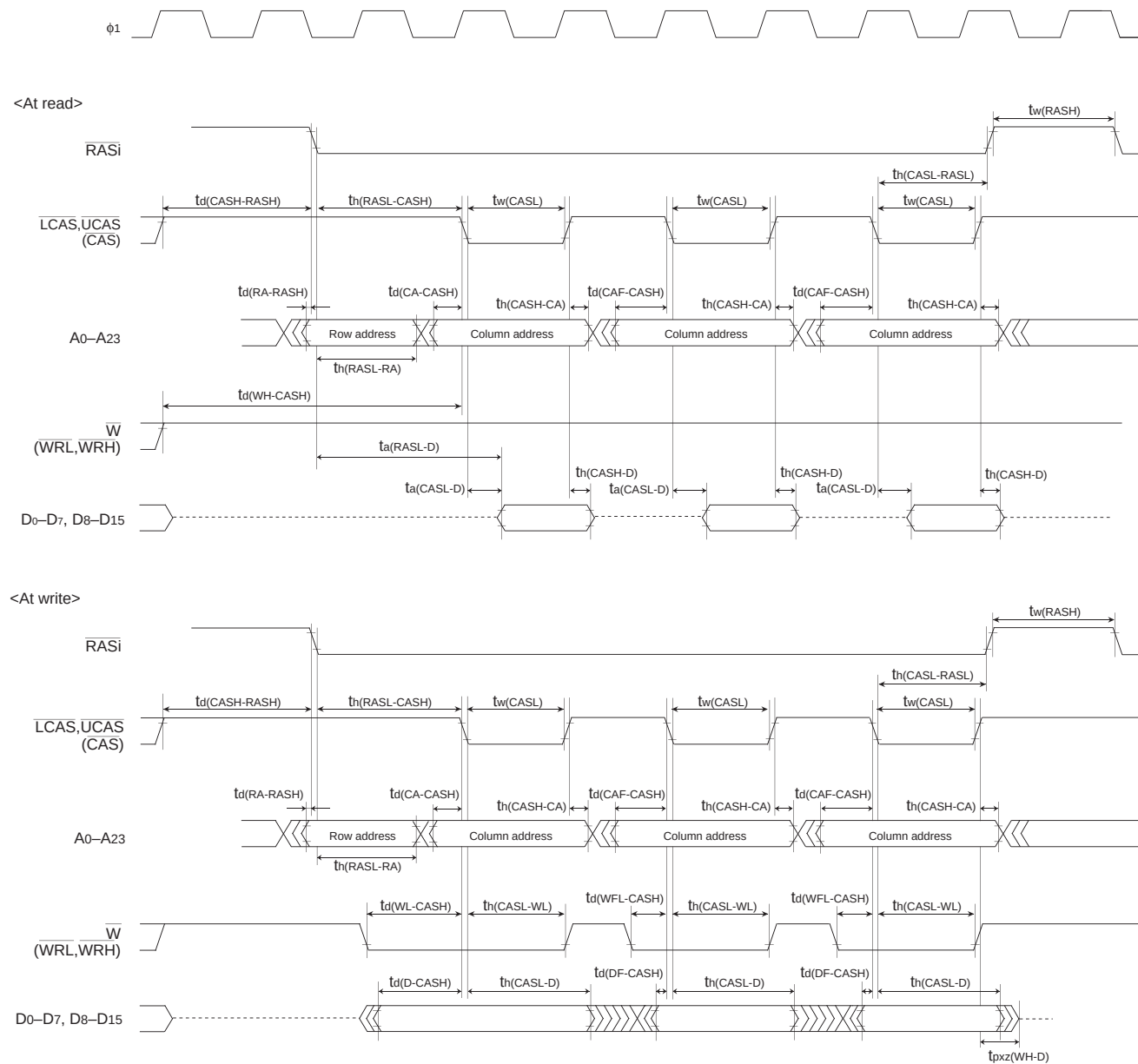
DRAM access : fast page access = OFF



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0\text{ to }70\text{ }^{\circ}\text{C}$
- Input timing voltage : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 15\text{ pF}$ ($\overline{\text{RAS}}_i$)
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$ (except for $\overline{\text{RAS}}_i$)

DRAM access : fast page access = ON



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0\text{ to }70\text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 15\text{ pF}$ ($\overline{\text{RASi}}$)
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$ (except for $\overline{\text{RASi}}$)

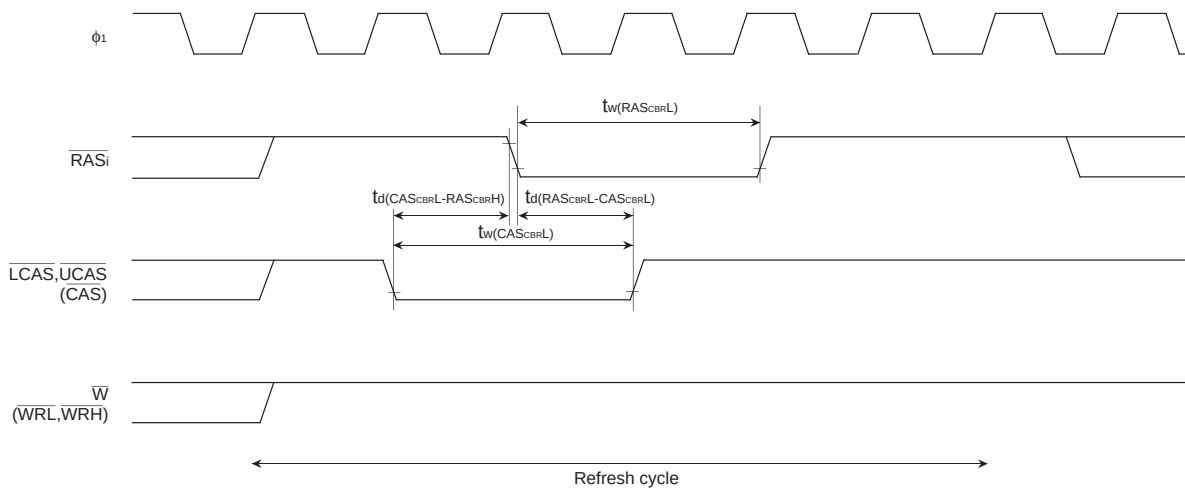
PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

DRAM refresh

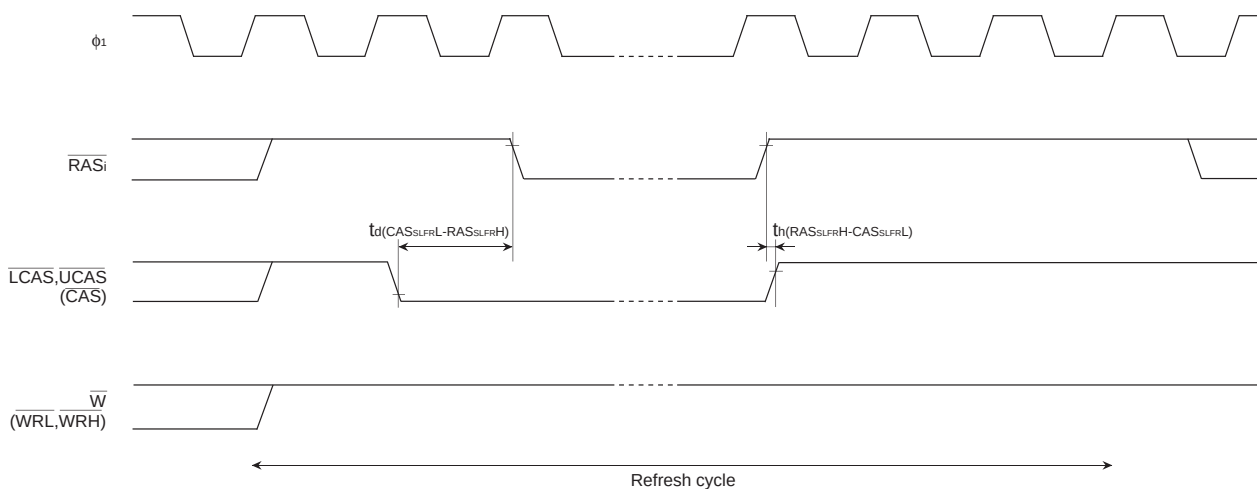
Switching characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }70\text{ }^{\circ}\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(\overline{\text{RAS}}_{CBRL})$	$\overline{\text{RAS}}$ low-level pulse width (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	$2t_c - 15$		ns
$t_w(\overline{\text{CAS}}_{CBRL})$	$\overline{\text{CAS}}$ low-level pulse width (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	$2t_c - 15$		ns
$t_d(\overline{\text{CAS}}_{CBRL}-\overline{\text{RAS}}_{CBRLH})$	$\overline{\text{RAS}}$ high-level valid time after $\overline{\text{CAS}}$'s low level start (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	$t_c - 15$		ns
$t_d(\overline{\text{RAS}}_{CBRL}-\overline{\text{CAS}}_{CBRL})$	$\overline{\text{CAS}}$ low-level valid time after $\overline{\text{RAS}}$'s low level start (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	$t_c - 15$		ns
$t_d(\overline{\text{CAS}}_{SLFRH}-\overline{\text{RAS}}_{SLFRH})$	$\overline{\text{RAS}}$ high-level valid time after $\overline{\text{CAS}}$'s low level start (At self refresh)	$t_c - 15$		ns
$t_h(\overline{\text{RAS}}_{SLFRH}-\overline{\text{CAS}}_{SLFRL})$	$\overline{\text{CAS}}$ low-level hold time after $\overline{\text{RAS}}$'s high level (At self refresh)	-15	15	ns

DRAM refresh : $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh



DRAM refresh : self refresh



Test conditions

- $V_{cc} = 5 \text{ V} \pm 10 \%$, $T_a = 0 \text{ to } 70^\circ\text{C}$
- Output timing voltage : $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$, $C_L = 15 \text{ pF}$ ($\overline{\text{RAS}}_i$)
- Output timing voltage : $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$, $C_L = 50 \text{ pF}$ (except for $\overline{\text{RAS}}_i$)

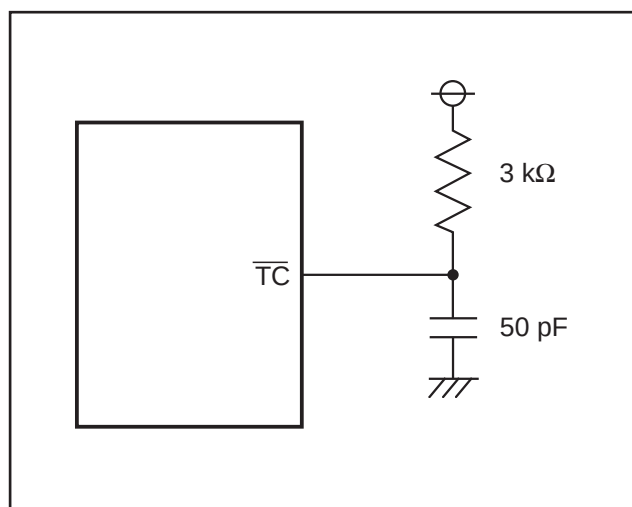
DMA transfer timing

Timing Requirements ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(TC_{INL}-\phi 1)$	$\overline{TC}$ input setup time	40		ns
$t_w(TC_{INL})$	$\overline{TC}$ input pulse width	$t_c + 20$		ns
$t_{su}(DRQL-\phi 1)$	$\overline{DMAREQ_i}$ input setup time	40		ns
$t_w(DRQL)$	$\overline{DMAREQ_i}$ input pulse width	t_c		ns

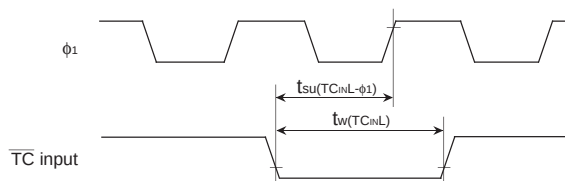
Switching characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(TCL)$	$\overline{TC}$ output pulse width	$t_c - 20$		ns
$t_d(RDH-TCL)$	$\overline{TC}$ output start delay time after read	$t_c - 15$		ns
$t_d(BXWH-TCL)$	$\overline{TC}$ output start delay time after write	$t_c - 15$		ns
$t_d(TCL-DMAACKL)$	DMAACK low-level output valid time after $\overline{TC}$ output start	$2.5t_c - 20$		ns

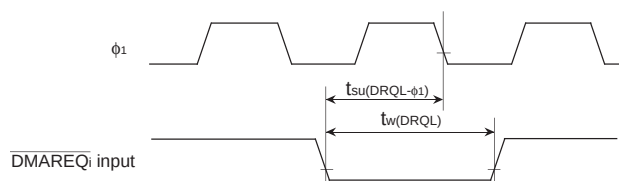


Test circuit for $\overline{TC}$ output

● $\overline{\text{TC}}$ input



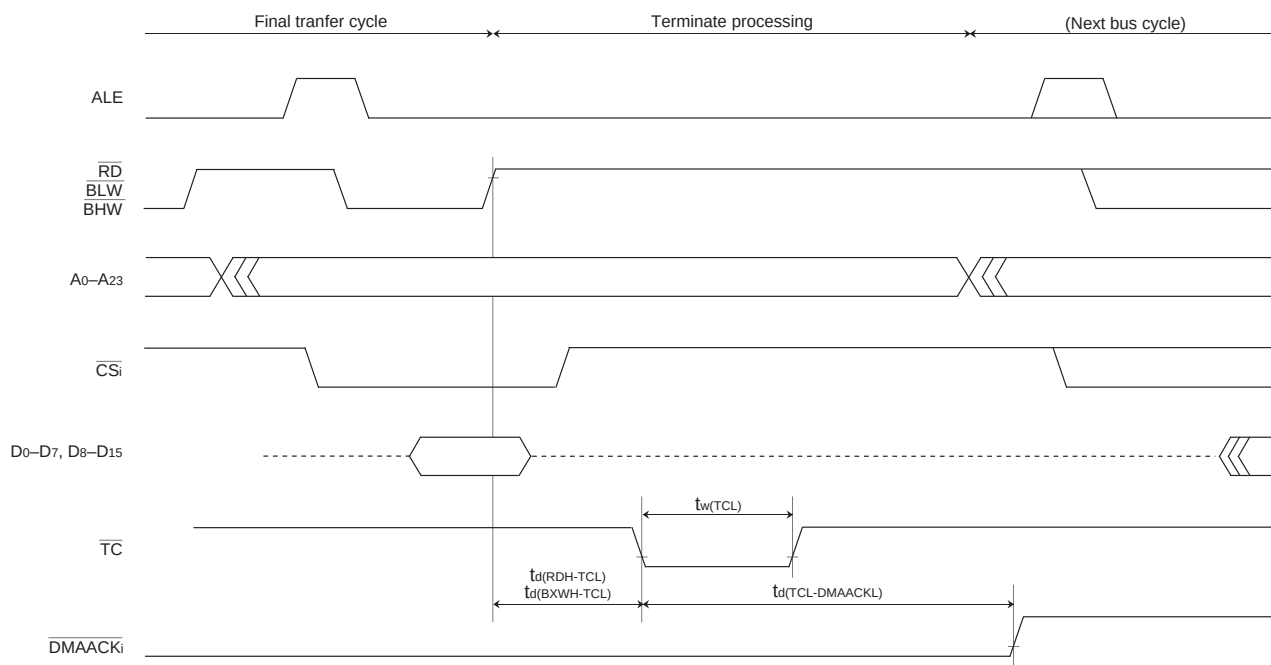
● $\overline{\text{DMAREQ}}_i$ input



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = -20$ to 85°C
- Input timing voltage : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$

● Transfer terminate timing



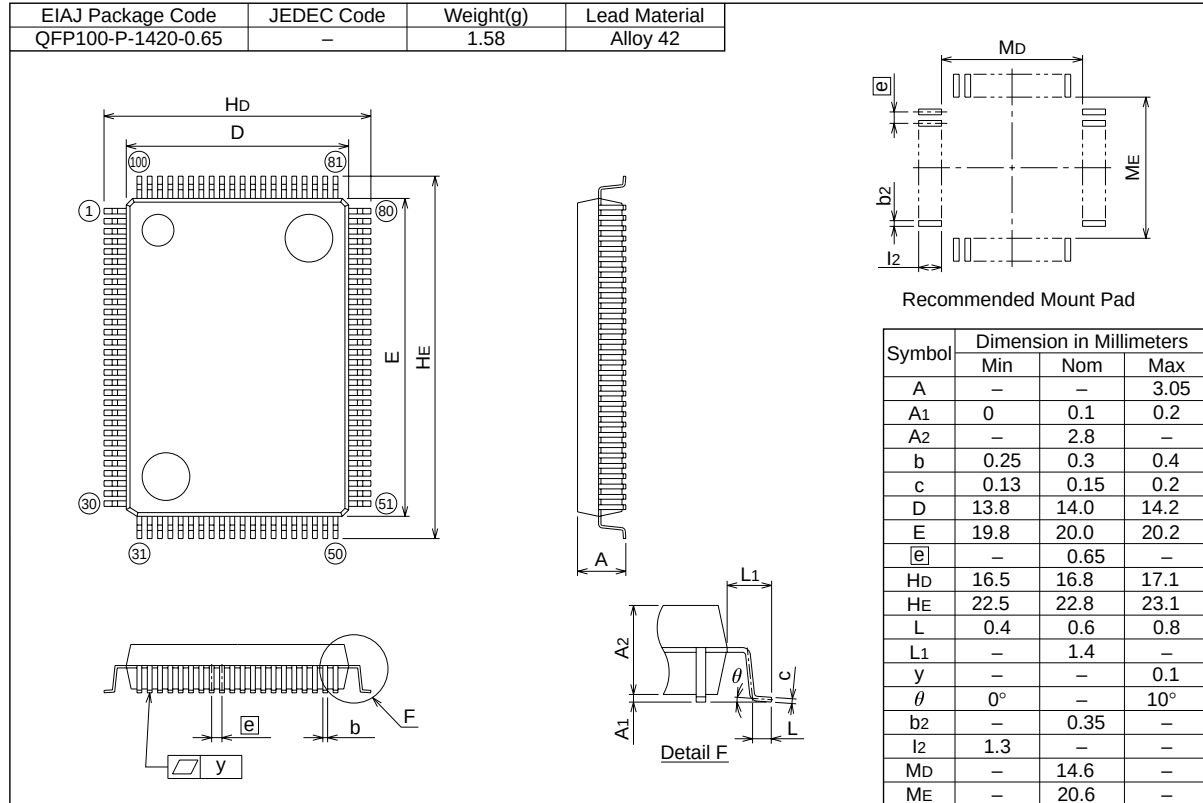
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = -20$ to 85°C
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$

PACKAGE OUTLINE

100P6S-A

Plastic 100pin 14X20mm body QFP



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- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

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