

20V P-Channel Enhancement-Mode MOSFET

$V_{DS} = -20V$

$R_{DS(ON)}, V_{GS}@-4.5V, I_{DS}@-4A = 60\ m\Omega$

$R_{DS(ON)}, V_{GS}@-2.5V, I_{DS}@-4A = 75\ m\Omega$

$R_{DS(ON)}, V_{GS}@-1.8V, I_{DS}@-2A = 85\ m\Omega$

Features

Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

we declare that the material of product

compliance with RoHS requirements.

S- Prefix for Automotive and Other Applications Requiring

Unique Site and Control Change Requirements; AEC-Q101

Qualified and PPAP Capable.

▼ Simple Drive Requirement

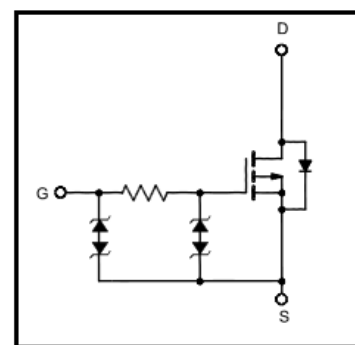
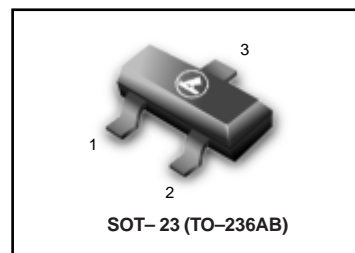
▼ Small Package Outline

▼ Surface Mount Device

Ordering Information

Device	Marking	Shipping
LP3415ELT1G S-LP3415ELT1G	P15	3000/Tape&Reel
LP3415ELT3G S-LP3415ELT3G	P15	10000/Tape&Reel

LP3415ELT1G
S-LP3415ELT1G



Maximum Ratings and Thermal Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	-20	V	
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current	I_D	-4	A	
Pulsed Drain Current 1)	I_{DM}	-30		
Maximum Power Dissipation	P_D	$T_A = 25^\circ C$	1	W
		$T_A = 75^\circ C$	0.6	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$	
Junction-to-Case Thermal Resistance	R_{qJC}	100	$^\circ C/W$	
Junction-to-Ambient Thermal Resistance (PCB mounted) 2)	R_{qJA}	150		

Note: 1. Repetitive Rating: Pulse width limited by the Maximum junction temperature

2. 1-in² 2oz Cu PCB board

3. Guaranteed by design; not subject to production testing

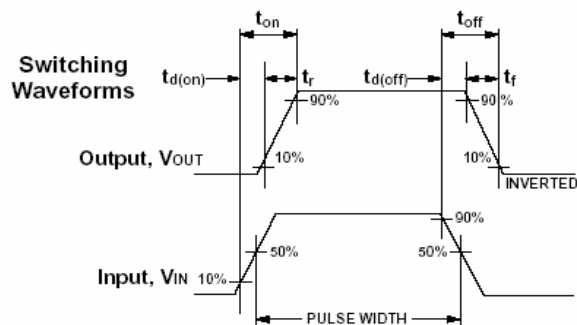
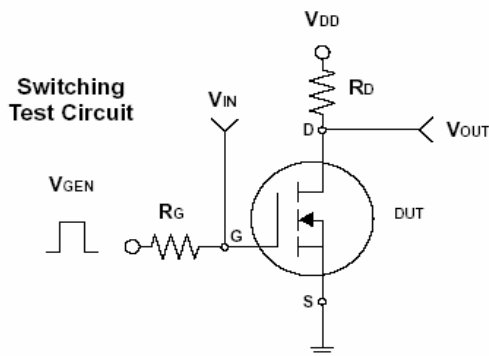
LP3415ELT1G , S-LP3415ELT1G

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -1.8V, I_D = -2A$			85.0	m Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -2.5V, I_D = -4A$			75.0	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -4A$			60.0	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.3		-1	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16V, V_{GS} = 0V$			-1	μA
Gate Body Leakage	I_{GSS}	$V_{GS} = \pm 8V, V_{DS} = 0V$			± 10	μA
Gate Resistance	R_g	$V_{DS} = 0V, f = 1.0MHz$		6.5		Ω
Dynamic³⁾						
Total Gate Charge	Q_g	$V_{DS} = -10V, I_D = -4A$ $V_{GS} = -4.5V$		4.59	5.97	nC
Gate-Source Charge	Q_{gs}			2.14	2.78	
Gate-Drain Charge	Q_{gd}			2.51	3.26	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10V, R_L = 2.5\Omega$ $I_D = -1A, V_{GEN} = -4.5V$ $R_G = 3\Omega$		965.2	1930.4	ns
Turn-On Rise Time	t_r			1604	3208	
Turn-Off Delay Time	$t_{d(off)}$			7716	15432	
Turn-Off Fall Time	t_f			3452	6904	
Input Capacitance	C_{ISS}	$V_{DS} = -10V, V_{GS} = 0V$ $f = 1.0 MHz$		36.45		pF
Output Capacitance	C_{OSS}			128.57		
Reverse Transfer Capacitance	C_{RSS}			15.17		
Source-Drain Diode						
Max. Diode Forward Current	I_S				-2.2	A
Diode Forward Voltage	V_{SD}	$I_S = -1A, V_{GS} = 0V$			-1	V

Note: Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

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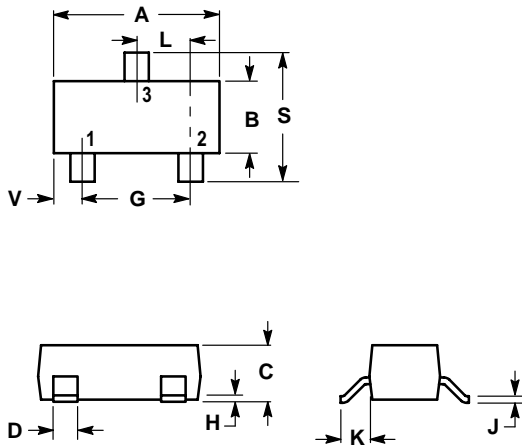


LP3415ELT1G , S-LP3415ELT1G

SOT-23

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

